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Low-Temperature Oxidation of Silicon Using Point-To-Plane Corona Discharge.

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LOW TEMPERATURE OXIDATION OF SILICON USING POINT-TO-PLANE CORONA DISCHARGE

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ABSTRACT

A technique for low temperature oxidation of silicon in dry oxygen ambient at temperatures between 25°C to 500°C using negative point-to-plane corona discharge is developed. The oxidation rate is a strong function of temperature and is found to increase significantly in comparison with the conventional thermal oxidation rate. For the thicker films, the refractive index of the grown oxide layer approaches the value obtained for high temperature thermally grown oxide. The effects of some independent process parameters such as time, temperature, and ion current on the oxidation of silicon are studied.

The electrical quality of the grown oxide film is investigated. The C-V characteristic curves of the MOS capacitors of the oxide grown by this technique show shifts in the flat-band voltage. The shift of flat-band voltage is found to be a function of oxidation temperature and the corona current during the oxidation process. The leakage current of the capacitor fabricated with the oxide grown by this method is not symmetric for applied dc negative and positive gate bias voltages. When the aluminum plate of the capacitor is biased negative with respect to the substrate, the measured value of the current is substantially higher than the measured current value under positive bias. The mechanism of the leakage current for the oxide grown at room temperature is studied. The interface trap

density spectrum in the range of $5x10^{10}$ to $5x10^{13}$ cm^{-2} $(eV)^{-1}$ is obtained for the oxide grown at 400°C for one hour with 1 cm electrode distance at 1 atm pressure in dry oxygen ambient. The oxide film grown by this method has a potential for application in device fabrication technology. The application of the Nicollian and Reisman oxidation model indicates that the oxidation process at a given temperature under corona discharge is more strongly surface reaction controlled than thermal oxidation of silicon. The observed high rate of oxidation of silicon by corona discharge in a dry oxygen ambient may be associated with stress relief and an increase in the viscous flow of the grown SiO_2 film during oxidation.

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

In silicon technology, high temperature processes are being substituted by lower temperature processes. Dopant incorporation processes conventionally achieved by thermal diffusion at 900 - 1200°C are now being replaced by ion-implantation and low temperature annealing.[1] Plasma-enhanced chemical vapor deposition (PECVD) around 300 - 400°C or photo-excited CVD at below 300°C are being examined to substitute for CVD. Oxidation of silicon which is one of the most important high temperature processing steps in fabrication of integrated circuits is carried out at a temperature around 1000°C for gate insulator material. There have been significant efforts to develop low temperature oxidation techniques such as high pressure oxidation (700 - 1000°C), plasma oxidation, and photo-assisted oxidation. Each of these techniques offers its own advantages and has its own limitations. As a result, conventional high temperature oxidation of silicon continues to remain the most commonly used oxidation technique for formation of MOS gate dielectric material.

Reducing the oxidation temperature has the following advantages: 1) reduction in lateral as well as vertical movement of dopant atoms, 2)

reduction in oxidation induced defects, 3) reduction in wafer warpage, 4) reduction in diffusion of heavy metals, and 5) increase in processing flexibility such as post-metalization oxidation.[2–6] Low temperature oxidation is particularly important for the development of multilayer three dimensional circuits since in this case fabrication of upper layer devices needs to be carried out without significantly affecting the device structures in the lower layers. Novel approaches to oxidation may be desirable for future development of high density, high speed VLSI circuits. These novel techniques must be capable of forming thin, non-porous SiO_2 films of good electrical quality at low-growth temperatures.

1.2 Objectives

The silicon dioxide film formation is an important step in IC fabrication. The SiO_2 films are used for many different purposes such as MOS gate oxides, multi-layer isolations, spacer oxides, field oxides, and passivation layers. The high temperature oxidation produces excellent quality oxide films, but as mentioned earlier, it has disadvantages such as redistribution of impurities. There are some alternatives to produce oxide films with lower quality at low temperature which have been briefly reviewed in the subsequent sections. These lower quality oxide films are mainly used for multi-layer isolation, field oxides, and passivation layers in IC fabrication.

The objective of this work is to investigate negative point-to-plane corona discharge oxidation of silicon at low temperatures in the range of 25°C to 500°C. The effects of some of the oxidation process parameters such as temperature and corona current density on the grown oxide films are studied for the possible application of this technique to VLSI fabrication technology. The effect of negative point-to-plane corona discharge on the rate of oxidation of silicon is examined. Also, some of the electrical properties of the oxide grown by this technique are investigated.

1.3 Oxidation Techniques for Silicon

There are many different techniques for oxidation of silicon. The oxide film obtained by each technique has its own application niche in an IC fabrication process. Oxides with superior electrical quality are produced by a high temperature thermal oxidation of silicon in dry oxygen for MOS structures. These oxides must have good interface properties as well as other chemical and electrical properties. The oxide insulating film is also used for field oxide and for passivation protective coating. Currently, SiO_2 is being used as an interlayer dielectric film to isolate the first level metal interconnect from the second layer metal interconnect in a multilevel metalization scheme. The interface property of films for interlayer isolation, field oxide and passivation coating is not of much concern as it is for the gate oxide film, but a low temperature oxide formation is

desired. For example, excessive time at high temperature during interlayer dielectric formation could cause excessive hillock formation in the underlying metalization level.[7] These hillocks could produce inter-metal shorts if they become exposed during dielectric resist etchback planarization or during the via etch. If the inter-metal short is not produced, it may cause sufficient dielectric thinning to cause leakage or breakdown during the operation of the IC. When the space between the metal lines decreases for submicron IC technology, the voids in the dielectric between closely spaced Al lines of the first level metal could cause poor step coverage for the second metal layer. This could lead to low yield or reliability problems. Various oxidation techniques are briefly reviewed in the following sections.

1.3.1 Thermal Oxidation of Silicon

Thermal oxidation of silicon at high temperature is the oxidation technique which is currently used in industry to produce very high quality MOS gate oxides. Thermal oxidation of silicon, which is carried out at 1000°C to 1200°C, is a high-temperature step in comparison with the temperatures of several other steps present in the VLSI processing. In the last twenty years or so, the oxidation rate and the chemical and the electrical quality of the resultant Si–SiO_2 interface has probably been studied more extensively than any other interface. However, more work is needed to

obtain a better understanding of oxidation mechanism of extremely thin gate oxides. The MOS gate oxide thickness is scaled to smaller values to meet the requirements of submicron line width design rules and, hence, will remain an area of contemporary interest for some time to come. The thermal oxidation setup and apparatus is very simple, but it requires a clean room and a contamination free furnace. The disadvantages of conventional thermal oxidation are problems such as redistribution of impurity, wafer warpage, and defects associated with a high temperature process. There has been considerable work done to lower the oxidation temperature as an alternative for conventional thermal oxidation as described in the next section.

1.3.2 Low Temperature Oxidation Techniques for Silicon

Over the past few years, there has been significant effort to develop techniques to produce SiO_2 films at a lower temperature than the temperature of conventional thermal oxidation. Important among these low temperature oxidation techniques are photo-assisted oxidation, high pressure oxidation, plasma enhanced chemical vapor deposition (CVD) and plasma oxidation. Each of these techniques is briefly reviewed here.

1.3.2.1 Photo-Assisted Oxidation

In the past few years, photo-assisted oxidation of silicon and gallium arsenide has been investigated by several workers and enhancement in the oxidation rate has been reported. The sources of optical excitation used have been visible-light lasers or ultraviolet light.[8–13]

During the early stages of Si oxidation when the grown oxide layer is thinner than approximately 30 nm, the oxidation is a reaction control process, and the oxidation rate can be enhanced by optical excitation. One can argue that the optical beam can generate electron-hole pairs by breaking Si-Si bonds at the Si–SiO_2 interface and hence enhance the oxidation rate. If the grown oxide layer is thicker than about 100 nm, the rate of oxidation is limited by the diffusion of oxidizing species through the oxide layer and hence, oxidation becomes a diffusion control process. At this stage of oxidation, optical excitation alone would not be as effective.

The effect of the optical beam during oxidation is two fold. One is a simple heating effect and the second is a photonic effect.[11] Young and Tiller have shown that in their experiments, the photonic mechanism was the dominant mechanism in the oxidation rate enhancement of silicon. The oxide growth using pulsed excimer laser at the wavelength of 193 nm (ArF) and 248 nm (KrF) showed a dramatic rate enhancement at 193 nm wavelength.[13] At relatively low laser pulse intensity (0.05-0.40 J/cm^2), the

substrate heated to less than 500°C and cooled within 100 ns at both wavelengths.[13] Thus, the observed 10 times higher rate at the shorter 193 nm wavelength with respect to the longer 248 nm wavelength is attributed to photonic effect such as photo-dissociation of O_2 to O atoms having a high degree of reactivity.

One of the advantages of photo-assisted oxidation is its ability to be extremely localized in a well defined area of the surface. The disadvantage of the photo-assisted oxidation is the difficulties associated with non-conformity of the optical beam or pulse which can result in non-uniform oxide film on the wafer. This problem may be resolved by using a large area uniform beam from a synchrotron radiation source.

1.3.2.2 High Pressure Oxidation

High pressure (25-500 atm) oxidation of silicon was first performed at Bell Laboratories around 1960. The selectivity of this oxidation method has been tested by carrying the oxidation of silicon samples at 90 atmosphere pressure and 700 °C using Si_3N_4 as a mask which opened new possibilities of growing SiO_2 films at low temperature for VLSI fabrication. The rate of oxidation of 5.4 nm/min at 60 atmosphere pressure and 675 °C for (111) silicon was reported.[14] This method has been used in industry since the 70's. The oxidation temperature is typically around 800°C and

the pressure is typically around 10 atm. There has been commercial high pressure oxidation equipment available since 1977 such as GaSonics HiPOX unit capable of handling large number of wafers from 10 atm to 25 atm between 600°C to 1000°C.[15–16] The quality of the oxide grown by this method is comparable with the quality of oxide grown by the conventional high temperature oxidation, although increases in electron trapping due to neutral traps in the former have been reported.[17] This technique suffers from the safety problems associated with the operation at a high pressure.

1.3.2.3 Atmospheric and Low Pressure Thermal CVD

In this process, all of the deposition species are brought into the reactor from the outside, and the reaction is promoted by thermal energy only. For silicon dioxide dielectric film formation, the reactant gases are typically SiH_4 and O_2 with nitrogen as a carrier gas. The deposition rate is about 100 nm/min at 200-500°C temperature for the atmospheric pressure CVD process. There are three types of reactors in common use, namely, horizontal reactors, vertical reactors and barrel reactors. At higher temperatures, the rate of deposition is mass-transport limited and, hence, is proportional to the diffusivity of the gas molecule and the gradient of gas phase concentration. As the temperature decreases, the surface reaction rate decreases rapidly because it is an activated process, and the process

becomes surface-reaction controlled. The rate of deposition is a strong function of temperature at low processing temperatures. Therefore, it is essential to have a good control of the process temperature. Radio-frequency induction heating is used to heat the substrate. If the wafers are placed in the furnace vertically to increase the wafer capacity, uniform deposition cannot be obtained in the mass-transport-limited operation with narrow spaces between wafers. Uniformity is obtained by using lower temperatures and low pressures, hence, low pressure chemical vapor deposition (LPCVD) is often employed.[18–20] Low pressure CVD has several advantages over the atmospheric pressure CVD including an increase in the wafer throughput, reduction in reactant gases needed for deposition, and improved film uniformity from one wafer to the next. However, the low-pressure CVD has a slower deposition rate of 10-15 nm/min versus 100 nm/min for film processing with the atmospheric pressure process. The operating pressure of LPCVD for SiO_2 processing is about 0.7 torr and the operating temperature is typically 450°C. The LPCVD process operates in the surface reaction control regime making the deposition rate a strong function of temperature and, therefore, difficult to control.

1.3.2.4 Plasma-Enhanced CVD

The metallurgical considerations, such as hillock formation in the first metal level and microcracks or thinning in the second metal level, which

result in poor metal coverage require the dielectric SiO_2 film to be processed by plasma enhanced chemical vapor deposition (PECVD). Dielectric films deposited by PECVD are preferred over LPCVD in consideration of electromigration reliability problems and step coverage when multilevel interconnect metal lines are used.

Plasma-enhanced CVD is becoming increasingly important in integrated circuit fabrication. Silicon oxide, silicon nitride and silicon films can be deposited by this method. In this process, a plasma is used to couple electrical energy into the gas and promote the chemical reactions and, hence, decrease the temperature of the operation. The plasma is an almost-neutral collection of molecules and excited radicals and some charged particles. Both neutral radicals and ionized species are created by the energetic, high temperature electrons impacting on the molecules. Different types of discharges have been used for processing of devices.[21] Glow discharge can be produced by application of a dc or a low frequency voltage across electrodes inside of the discharge tube, or by application of a high frequency, such as radio or microwave frequencies at low pressures external to the discharge tube. dc parallel plates and point-to-plane corona discharges have so far not been of much practical interest in the IC fabrication processes.

The effects of plasma source frequency and reactor pressure on the quality of the oxide produced by PECVD have been reported.[22] The

amount of ion bombardment on the film changes as the excitation frequency varies. In dc excitation and low pressure plasma, the sample surface is bombarded with higher energy ions and hence, it affects the quality of the deposited film differently than the higher pressure and higher excitation frequency plasma. In a dc excited plasma, a dc voltage is applied across two parallel conducting plate electrodes. The plasma glow region is distinctive from the dark sheath region near the electrodes. Since the glowing plasma region is a very good conductor, most of the applied voltage across the parallel plates will be dropped in the plasma sheath regions. The electric field inside of the glow region is small and the voltage inside of this region is almost constant. The plasma has slightly positive potential. The electrons of the glowing region are attracted towards the anode while the positive ions are attracted toward the cathode. Secondary electrons will be created during the bombardment of the cathode. As the frequency of the plasma source is increased to less than 500 HZ, both the ions and the electrons respond to the variation of electric field. However, as the frequency increases above the "ion transition frequency," the differences in the effective masses of electrons and ions become obvious as the ions tend to move slower than the electrons in the time varying electric field. At a frequency of about 450 kHz, it will take several rf cycles for ions to reach the cathode, hence the average energy of the ions during the bombardment of the cathode will be reduced. This will affect

the quality of the oxide during deposition. The efficiency of electron generation is higher for high frequency plasma sources than for the lower frequency plasma sources, but a low frequency plasma source yields a lower wet etch ratio and more compressive oxides. Therefore, a combination of low and high frequency plasma sources is used. A carrier waveform with a frequency of 13.56 MHz and 200 volts peak-to-peak voltage and a 450 kHz, 800 volts peak-to-peak modulating waveform were used by Hey et al.[22] However, the sidewall oxides and flat surface oxides will have different etch rates. The oxides on the horizontal surfaces have lower etch rates than the oxides on vertical surfaces. Also, a denser oxide film is produced when a lower frequency signal is applied across the electrodes and when the process is carried out at a lower pressure. This is a possible indication of ion bombardment affecting the quality of the film.

The most desirable type of deposition is the process which results in an end product of thin film with stochiometrically correct or chemically stable structure. Lucovsky et al. have discussed two approaches for silane-based PECVD of silicon oxide films.[23–25] One is the direct PECVD in which all gas phase reactants are simultaneously excited by the plasma and the substrate is located directly in the plasma, and the other is a remote PECVD in which one of the reacting gases is plasma excited and the substrate is located outside the plasma. The authors reported stoichiometric, hydrogen-free silicon oxide films were obtained at

relatively low substrate temperatures of 100 to 300°C by this remote PECVD technique.[23–25]

1.3.2.5 Plasma Oxidation of Silicon

Plasma oxidation of silicon differs from plasma enhanced CVD in that in the former case the reactant gas is either oxygen or steam which reacts with silicon substrate and, hence, it is essentially a process of oxide growth. In plasma enhanced CVD, there are usually several gas reactant molecules present and the oxide film is deposited on the substrate, and thus it is a deposition process. Plasma oxidation growth is currently not employed by industry but use of the plasma enhanced CVD is quite widespread. Most of the workers have studied the plasma oxidation process for the purposes of determining the oxidizing species involved in thermal and plasma oxidation and for studying oxidation mechanism.[26–29] Ligonza observed a nonparabolic oxidation rate in an oxygen plasma excited by microwaves without the application of an external dc voltage between the electrodes.[26] For a given temperature and a given discharge condition, no further increase was observed over periods of many hours after the film thickness had reached its asymptotic value. However, if a dc voltage in the range of 30 to 90V was applied between the electrodes, the oxide film was seen to grow on the anode side with a parabolic rate with

no limiting final value. Ray and Reisman studied the formation of SiO_2 on silicon in a rf generated oxygen plasma in the pressure range of 10 mTorr and below.[27] The rate of oxidation was found to be temperature independent in the 600 to 800°C range at 4.5 kW rf plasma power. The properties of the oxide formed at 600°C and above were reported to be somewhat poorer than thermal oxides grown in the 1000-1100°C range. The oxides had higher fixed charge and interface trap state densities while their refractive indices were seen to be the same as that of thermal oxides. However, the oxidation mechanism was found to be more like a deposition rather than growth. The possibility of the deposition of SiO_2 from the SiO sputtered from the wall of the reaction chamber was verified by an experiment.[27] This experiment was done by partially masking the surface of the wafer with a 400 nm thick Al film and then exposing the wafer to the plasma. SEM showed that SiO_2 formed on both the exposed Si surface and also on the Al film. The results of the plasma oxidation experiment reported by Ligonza suggested involvement of oxygen negative ions, O^-, in the oxidation of a silicon sample when dc voltage was applied between the electrodes since no limiting final values of oxide thickness were measured in that case.[26] The work of Ray and Reisman indicated the plasma deposition process instead of the growth process when no dc voltage is applied between the electrodes.[27] As a result, the electrical quality of the oxides grown in the oxygen plasma have not been investigated.

In summary, there are many different techniques to form SiO_2 films, but the oxide film grown by high-temperature conventional thermal oxidation is commonly used for MOS gate oxide. However, other methods to produce oxide are suitable for various application in IC fabrication which requires lower quality oxides. The electrical quality of the oxides grown by the plasma oxidation have not been reported. Plasma oxidation growth and point-to-plane corona discharge oxidation, which is also a plasma oxidation growth process, have been mostly used for investigation of specifying the oxidizing species involved in the oxidation technique. The study of oxidation of silicon using point-to-plane corona discharge at low temperature is not found in available literature. The development of a technique for low temperature oxidation of silicon using point-to-plane corona discharge is desirable for possible application in VLSI device fabrication.

1.4 Brief Preview of the Current Work

The point-to-plane corona discharge in an oxygen ambient at 700°C to 1000°C has been studied to resolve some of the controversial arguments about the oxidizing species involved in conventional high temperature thermal oxidation of silicon.[30–31] The authors concluded their work by identifying neutral oxygen molecules as the oxidizing species and not the positive or the negative charged oxygen ions during thermal high temperature oxidation of silicon. This result strictly applies to oxides thicker than

about 30 nm and is based on a thermodynamic argument which states that it is energetically unfavorable to form interstitial negative oxygen ions by transport of electrons and holes from SiO_2 layer to the SiO_2/gas interface. Recently, it is reported that the oxide films which are grown at temperatures below 900°C in dry oxygen with point-to-plane corona discharge technique are more conformal (uniform) around both concave and convex surfaces than those for thermally grown oxides.[32] The two-dimensional effects in silicon oxidation become extremely important as the IC device geometries shrink.[33–37] There is a potential for application of corona discharge on silicon structures such as oxidation layers for trenched capacitors for high density submicron IC technology.

In this work, some of the effects of the negative point-to-plane corona discharge oxidation of silicon at low temperatures 25°C to 500°C are investigated. In Chapter 2, the corona discharge generation is discussed and the design of furnaces for corona discharge oxidation is given. In Chapter 3, some of the effects of negative point-to-plane corona discharge on oxidation of silicon samples in dry ambient at low temperatures 25°C to 500°C are studied. The effects of negative point-to-plane corona discharge on silicon oxidation rate are considered. The refractive index and electrical properties of the oxide films grown by this method are also examined. The interface trap density values for the silicon samples which are oxidized at 400°C are obtained. In Chapter 4, the mechanism of

silicon oxidation at low temperature using point-to-plane corona discharge is examined. Chapter 5 gives the conclusions and the recommendations for future work.

CHAPTER 2

EXPERIMENTAL APPARATUS FOR PROCESSING WITH CORONA DISCHARGE

2.1 Introduction

The effects of corona discharge on the oxidation of silicon at low temperatures in dry oxygen ambient were first examined with a design of an initial simple furnace. Later on, two different furnaces were designed to carry out this work. One was designed with a stainless steel wall to study the rate of oxidation, and the other with an electronic grade quartz to study both the rate of oxidation and the quality of the grown oxides. In this chapter, the corona discharge generation is briefly described. The oxidation furnace design which is based on the constraints imposed by the corona discharge generation in dry oxygen ambient is explained. The design of both the stainless steel and the quartz furnace are described. The characteristics of the oxidation furnace made with electronic grade quartz is investigated. A comparison between the theoretical and practical corona discharge current versus applied voltage data at room temperature and at atmospheric pressure for 2 cm electrode gap is provided.

2.2 Corona Discharge Generation

Corona discharge has been studied by many workers.[38–40] Recently, rod to plane voltage/current corona discharge characteristics have been studied by McLean and Ansari.[40] The shape of current density has been experimentally verified to closely follow the Warburg's law. The Warburg's law is given by the relationship[38]

$$J(\theta) = J(0) \cos^{m}\theta \tag{2.1}$$

where J(0) is the current density directly below the needle point, θ is the angle between the perpendicular line from needle point and a line from the needle point to the point under consideration on the collecting plane as shown in Figure 2.1. The parameter m depends on the point to collecting plane gap distance, the applied voltage and the diameter of the needle point. In a simplified consideration, point to plane corona discharge ionization at low current is assumed to be confined to a small region around the needle point as shown in Figure 2.1. This means that the electric field is high enough to sustain ionization in the ionization volume around the needle point only. The drift region is assumed to be unperturbed at low current corona discharge and the electric field distribution is Laplacian. As the corona discharge current increases, the space charge will perturb the Laplacian field distribution. The current will now be space charge limited. The saturation current density, J(0), is then given by[40]

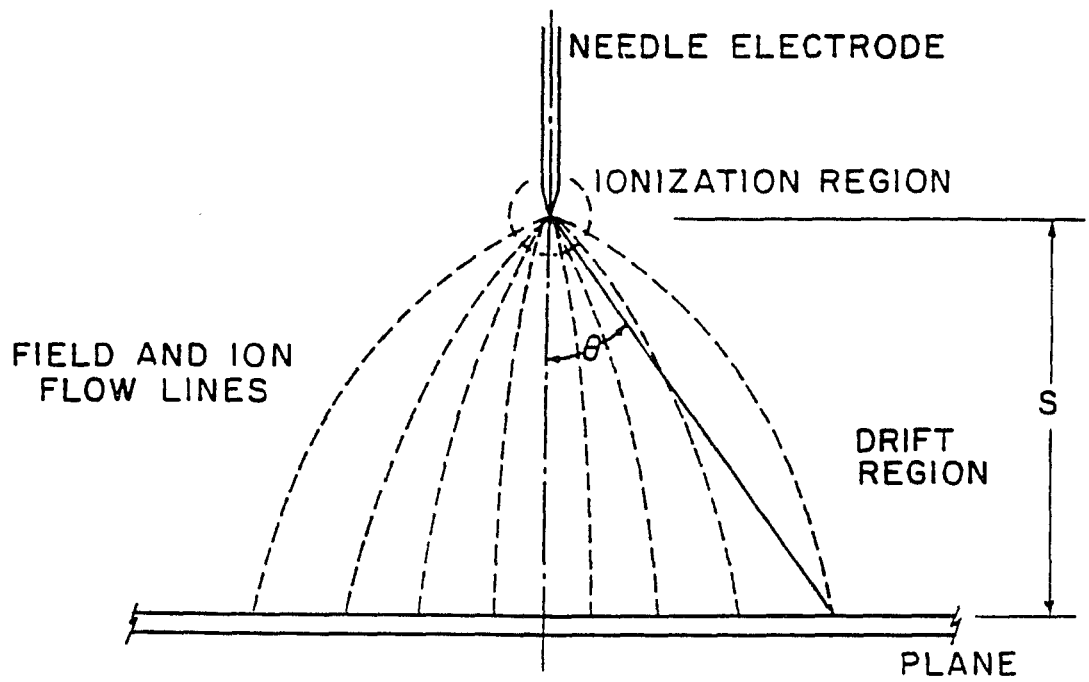

Figure 2.1 Point to plane corona discharge ionization regions.

$$J(0) = \varepsilon_0 \mu \frac{(V - V_d)^2}{(S - y)^3} \tag{2.2}$$

where ε_0, μ, V_d and y are respectively the permittivity of free space, ion mobility, the voltage required to establish the onset of corona discharge and the average length of corona ionization region. Here, S is the perpendicular distance from the needle point to the electrode plane. The current-voltage characteristic is obtained by using the Warburg's law as follows[40]:

$$I = K_a S^2 J(0) \tag{2.3}$$

where $K_a = \frac{2\pi}{(m-2)}(1 - \cos^{m-2}\theta_c)$ and θ_c is the cut-off angle defined as the angle between a line from the needle point electrode perpendicular to the plane electrode located underneath the point and the line from the needle point to a point located on the plane where current density becomes negligibly small. Here J(0) is the value of the corona current density as described before, and I is the corona discharge current. The corona current I is a function of pressure in the chamber and the applied voltage between the electrodes.

2.3 Oxidation Furnace Design

Oxidation furnaces were designed for the oxidation of silicon with

point to plane corona discharge in a dry oxygen ambient. Several important constraints in the design of these furnaces have been considered. One of these constraints is the oxidation of the electrode during oxidation. The corona discharge oxidation in pure oxygen ambient creates a highly oxidizing environment. This oxidizes not only the silicon sample but most other surrounding metals readily. It is desirable that the electrode does not oxidize during the oxidation cycle. After a period of exposure to the corona-discharge, the current will diminish if the electrode oxidizes. Another important constraint is the cleanliness present in the oxidation chamber. Outgassing from the furnace components particularly at temperatures higher than the room temperature will introduce contaminants into the system. If the furnace is used for atomic hydrogen annealing, it is desirable to operate under reduced chamber pressure of a four torr for safety purposes. Also it is necessary to decrease the pressure of the furnace lower than one atm at low temperatures for obtaining suitable values of corona-discharge ion current.

During oxidation, the sample should rest upon the substrate-holder and make an electrical contact to the substrate-holder which also acts as the bottom electrode. Initially, a high purity dense block of graphite with a smooth surface was used as the substrate-holder. The outer surface of the graphite block was found to oxidize in a few hours of exposure to the corona-discharge at 500 °C in a pure oxygen ambient. Hence, the graphite

block could not be used as an effective conductive electrode.

As a second choice, a block of molybdenum with a thin layer of molybdenum disilicide on the outer surface was used. The molybdenum block was heated by two 400 watt cylindrical heaters embedded into the block. Figure 2.2 shows the furnace with molybdenum substrate holder. The stainless steel wall surfaces of the furnace were cooled to 8°C by circulating chilled water. The molybdenum substrate holder block was found to remain conductive upon many hours of exposure to the corona-discharge at 500°C in pure oxygen ambient. However, exposure to the ambient air moisture seemed to degrade its conductivity. The next choice for the substrate holder material was a platinum foil of high purity mounted on a quartz disk. The electrical conductivity of the platinum foil remained unchanged after many hours of operation at low and high temperature corona-discharge oxidation.

For examining the electrical quality of the grown oxide films by this technique, a second furnace was designed from electronic grade quartz. Figure 2.3 shows the general view of this oxidation furnace. A platinum needle was used here as the top electrode. The needle was made by shaping a 1.0 mm diameter platinum wire. The diameter of the needle point was measured to be 0.1 mm. The platinum wire electrode was made from 99.9985% pure material. The needle was welded to a 0.25 mm diameter platinum wire. The platinum wire was passed through an inside quartz

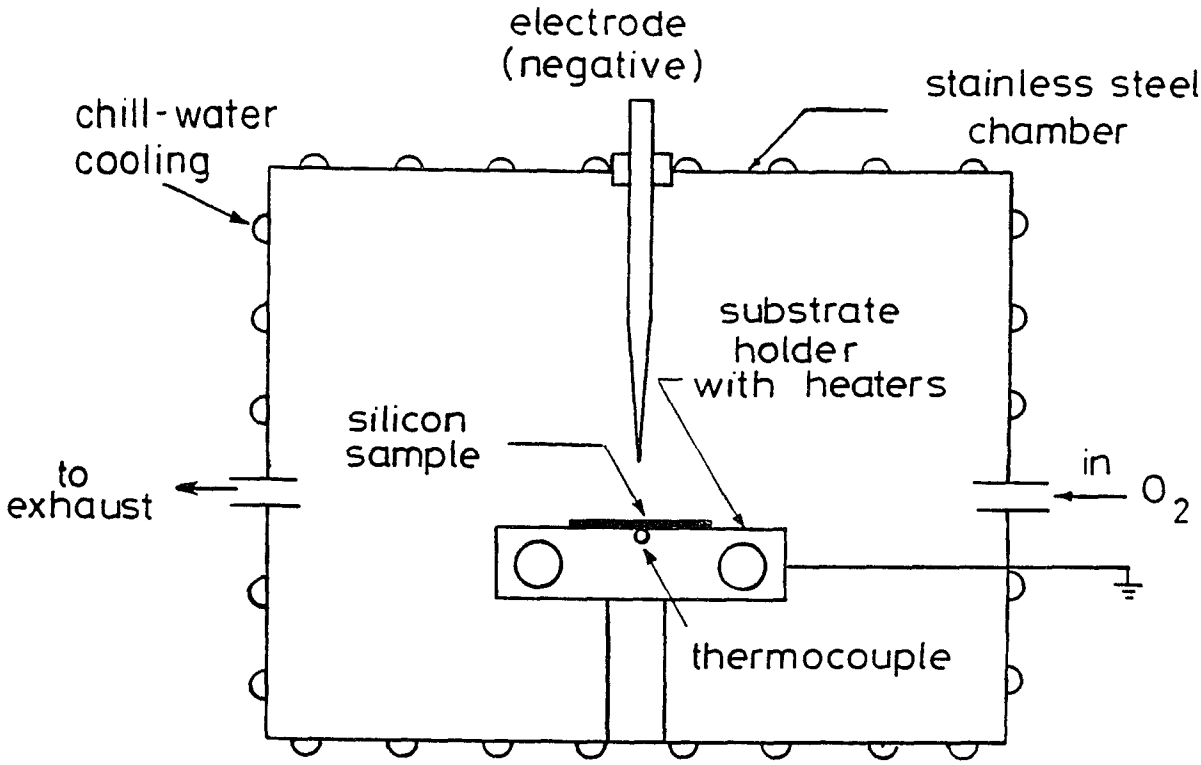

Figure 2.2 Stainless steel wall chamber with molybdenum substrate holder.

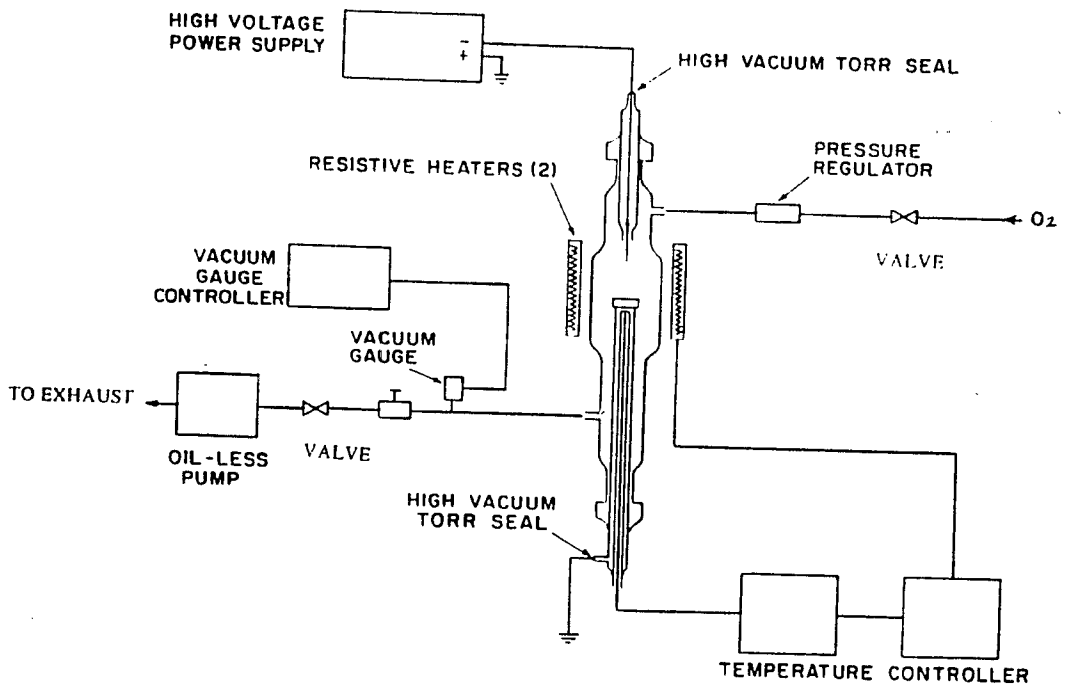

Figure 2.3 Experimental setup with the quartz oxidation chamber.

tube which extended to the outside of the top of the furnace and was connected to the high voltage power supply terminal. The substrate holder comprised of 99.998% pure platinum foil mounted on top of a quartz disk. The quartz disk is the top portion of the quartz tube which extended out of the bottom of the chamber. There is another quartz tube located inside of this quartz tube and was used for thermocouple wire leads. This inner quartz tube completely isolated the thermocouple wires from the furnace chamber environment, thereby eliminating contamination of the furnace chamber due to outgassing of the thermocouple wires. The thermocouple tip touches the bottom surface of the quartz disk on which the platinum foil resides. The thermocouple was, hence, located close to the sample during the oxidation for temperature measurements. The wire that connected the substrate platinum foil to the the high voltage power supply terminal passed through the quartz tube as illustrated in Figure 2.4. The outer quartz tube had a larger diameter in the center and was heated with the help of two semi-cylindrical resistive heaters as shown in Figure 2.3. In this design, the heaters were located outside the oxidation furnace to minimize the contamination due to the heater elements. The semi-cylindrical heaters can raise the temperature of the interior of the chamber to 1000°C. The uniformly heated section of the chamber extends from 2 inches above to 2 inches below the center of the chamber. The oxidizing gas flows from the top of the furnace to the bottom. The gas tube

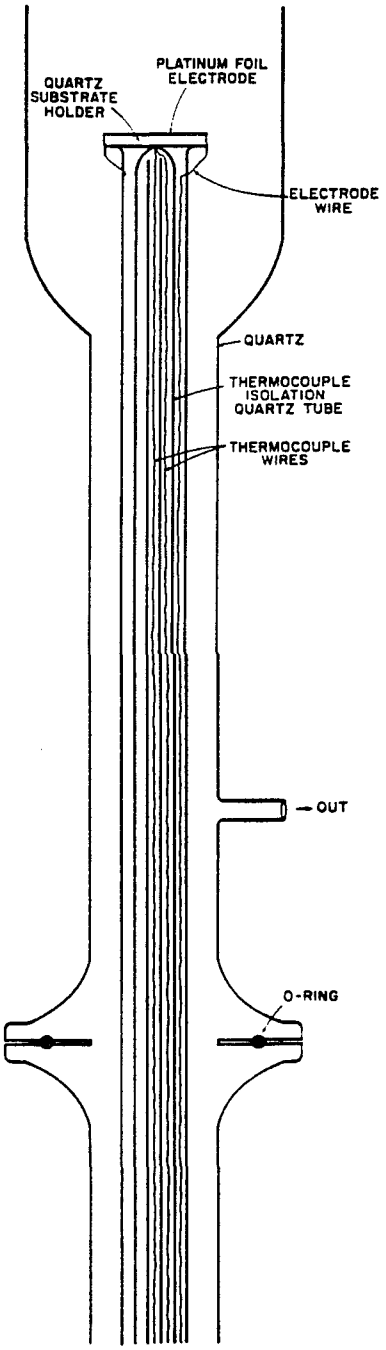

Figure 2.4 Substrate holder as the bottom electrode with the thermocouple assembly and an o-ring arrangement for loading and unloading the sample.

connections to the inlet and outlet of the quartz chamber which are located away from the hot zone of the furnace stays near room temperature during the operation. The quartz disk has grooves cut along the edges to reduce the stagnant layer during oxidation. The needle electrode position and the sample holder position can be changed with respect to each other. As a result, the gap between the needle electrode point and the substrate holder can be changed with respect to the center of the tube. Necessary guides have been designed to make the needle stay on top of the center of the substrate holder. The chamber length of 12 inches is long enough to keep the ends cool with moderate ventilation when the furnace is operating at high temperatures. The details of the furnace structure are shown in Figure 2.4 to Figure 2.7. The overall length of the furnace is 3 feet.

The loading of the sample is done easily by placing the sample on top of the platinum foil mounted on top of the quartz disk assembly as shown in Figure 2.4 and moved up to the desired position. Clamps are used to press the o-ring seals at the bottom. The furnace can be evacuated to less than a four torr pressure.

This furnace is designed for oxidation of silicon at temperatures from 25°C to 500°C. However, it can also be used for low temperature atomic hydrogen annealing of grown oxide films. Atomic hydrogen annealing has been found to be very effective in elimination of $Si–SiO_2$ interface traps by using a high voltage discharge via a Pt wire projection into the quartz

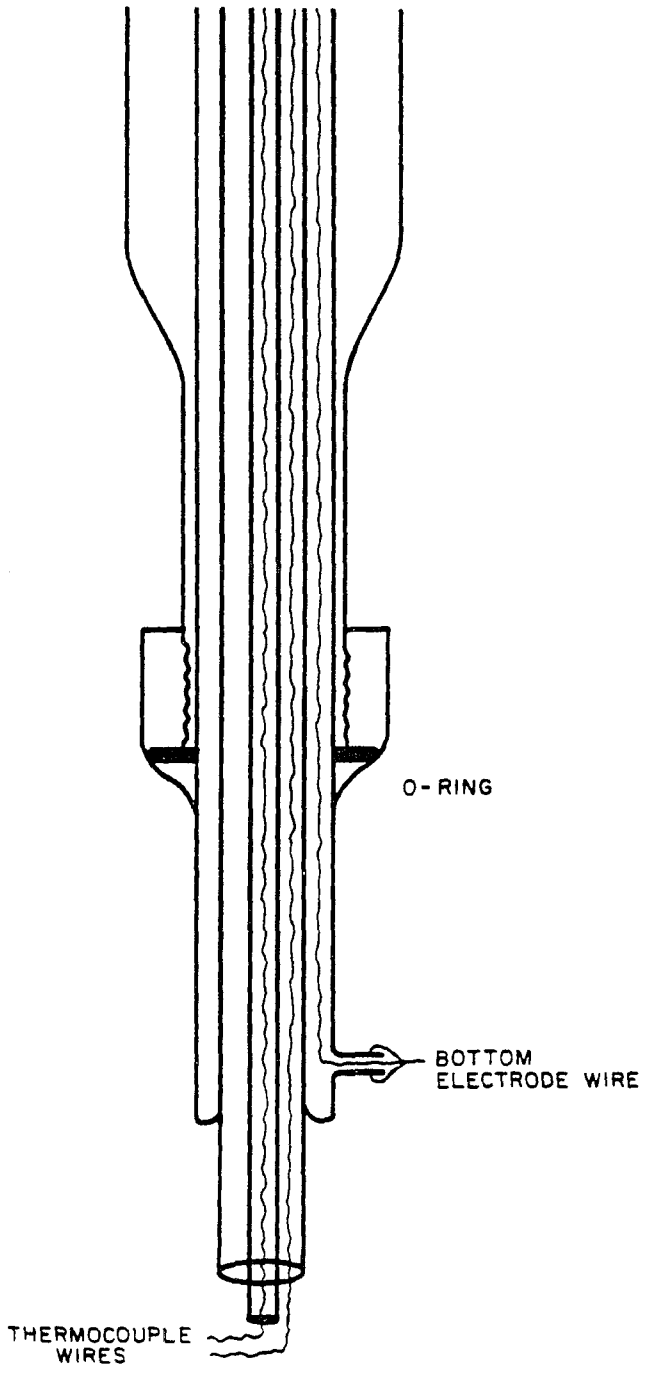

Figure 2.5 Detailed diagram of the bottom of the furnace.

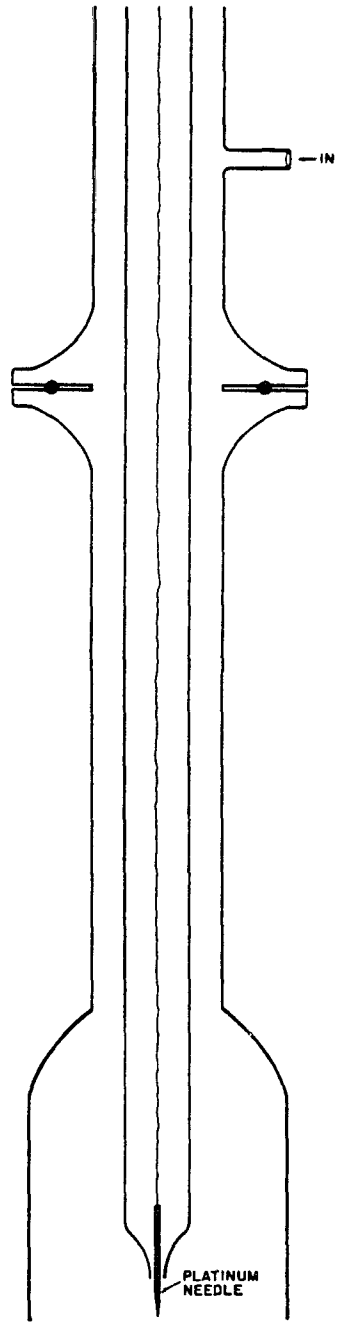

Figure 2.6 Platinum needle electrode assembly.

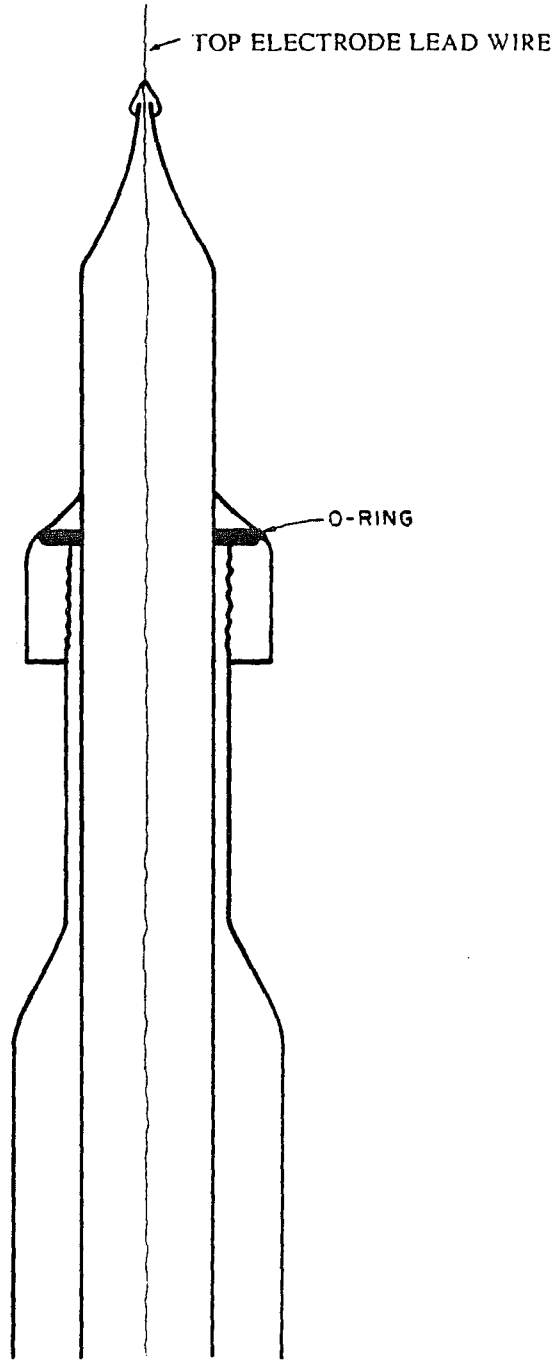

Figure 2.7 Details of the top electrode wire and o-ring assembly for needle to plane electrode gap distance adjustment

annealing chamber. The reduction of the interface trap density in atomic Hydrogen is observed at temperatures as low as room temperature.[41]

2.4 System Description

The reacting gas is made to flow from the gas tank through a stainless steel tube to a flow-meter located close to the quartz furnace of Figure 2.3. Tygon tube with wall thickness of 1/16 inch is used to connect the flow-meter to the furnace inlet. It is assumed that air moisture diffusing through this short piece of tygon tubing is not significant to have any effect on the oxidation rate. Prior to the oxidation process, the furnace with all the tubing is evacuated to a few torr, and consequently filled by dry oxygen. The gas outlet from the furnace is connected to a three way stainless steel valve by a thick-wall tygon tube. The chamber can be pumped to the desired pressure by a Cole Parmer oil-less vacuum pump Model J-7056-27. The chamber pressure is measured by a 275 series Granville-Phillips convectron gauge as shown in Figure 2.3. Two semi-cylindrical resistive heaters from Watlow Inc. are used to heat the furnace center zone. Each heater is rated at 275 watt maximum power. The two heaters together can raise the temperature of a 2 inch diameter, 4 inch long cylindrical cavity to approximately 1100°C. The exterior surfaces of the heaters facing the room ambient are vacuum insulated from the interior. The temperature of the cavity between the heater and the chamber is controlled within ± 3°C by a Eurotherm programmable type 818 controller

and Eurotherm model 831 SCR power supply assembly. A chromel-alumel type K thermocouple is used in this system. Even though the thermocouple is located close to the sample, its response is slow to the changes of the chamber temperature as it is isolated by the quartz tube envelope from the chamber. However, this delay in response does not create any problem in controlling the chamber temperature within ± 1°C for temperatures 500°C and higher. For controlling furnace temperatures in the range of 25°C and higher another chromel-alumel type K thermocouple is used. This thermocouple measures the temperature of the heater cavity wall directly. By controlling the temperature of the heater cavity, the temperature of the furnace interior can be monitored within ±2°C accuracy. Without the second thermocouple to control the temperature of the heater cavity directly, the controller will not be able to detect the changes in temperature fast enough by the first thermocouple located inside the furnace to react properly. The point to plane corona discharge is established by applying high voltage between the needle point and the substrate holder surface. The variable high voltage power supply, Gamma High Voltage Model RR30-2R/M207, used in this system can supply voltage in the range of 0-30 kV was modified to measure current also in the range of 0.1 μA to 30 mA. The polarity of the output voltage is reversible and the power supply can be used as a constant voltage or as a constant current source. The power supply regulation is 0.005% and the ripple is rated at

0.02%.

2.5 Furnace Characteristics

The properties of the built furnace were first examined. As mentioned in Section 2.2, the corona current is a function of pressure and applied voltage between the electrodes. This dependency is illustrated in Figure 2.8 for the quartz furnace with a 2 cm electrode gap and operating at room temperature. The corona current values for different pressures are the same for the applied voltages less than a threshold voltage. The value of the threshold voltage changes as the temperature of the chamber is varied. The effect of the chamber temperature on the corona current versus the applied voltage at one atm pressure for the same furnace is illustrated in Figure 2.9. The corona current at a given applied voltage beyond the threshold value is seen to increase with temperature and with reduction in chamber pressure.

The current/voltage characteristic for the corona discharge generator of the quartz furnace is shown in Figure 2.10. The needle point size is 0.1 mm and the measurement is performed at 1 atm pressure and room temperature. The distance between needle point and the bottom plate electrodes is 2 cm. Experimentally, the values of V_d and y in equation 2.2 are determined. The average length of the ionization region y can be obtained by measuring the ionization glowing region along the perpendicular line between the point of the needle to the collecting plate. The ionization

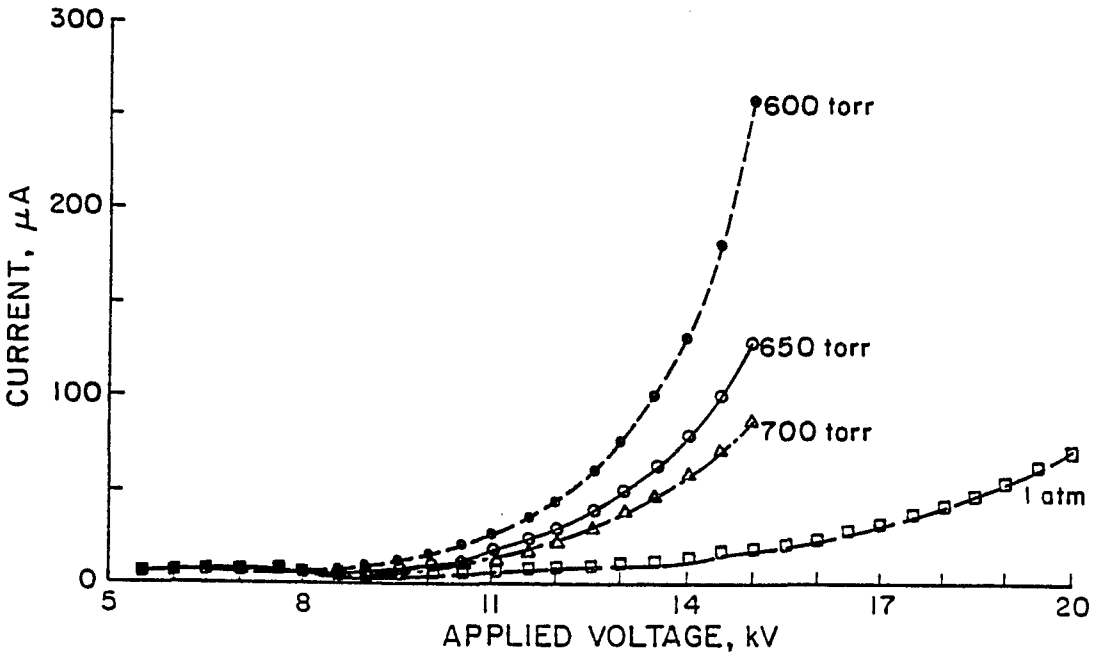

Figure 2.8 Plot of room temperatuare corona current vs applied voltage for different chamber pressures for a 2 cm electrode gap.

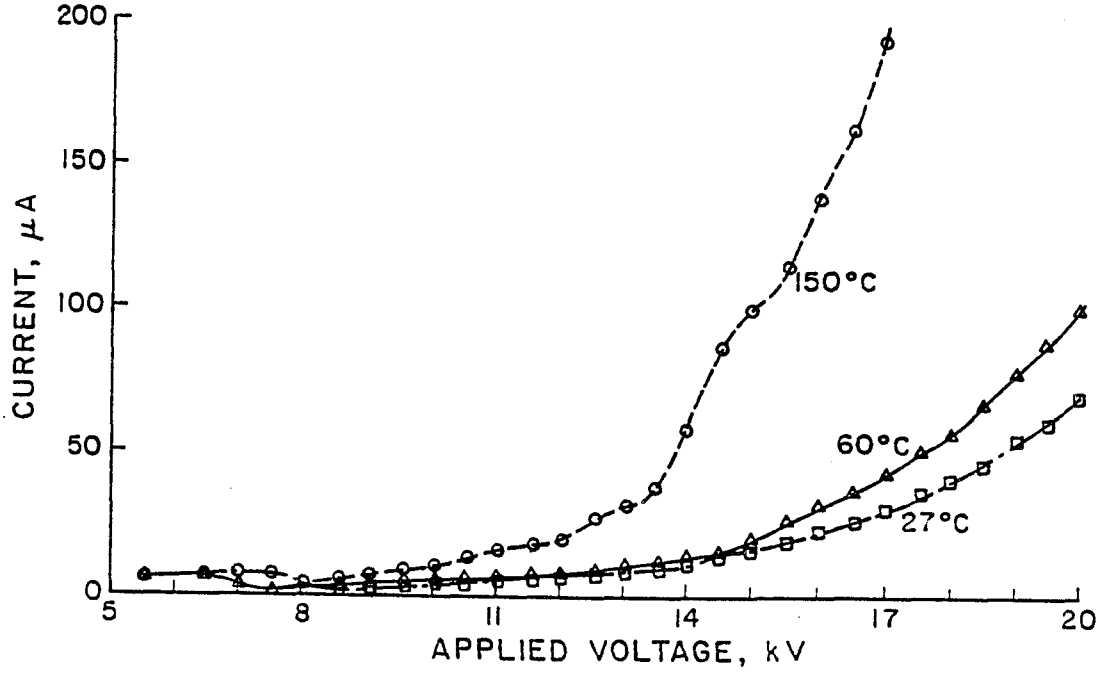

Figure 2.9 Plot of corona current vs applied voltage for different chamber temperatures for a 2 cm electrode gap and 1 atm pressure.

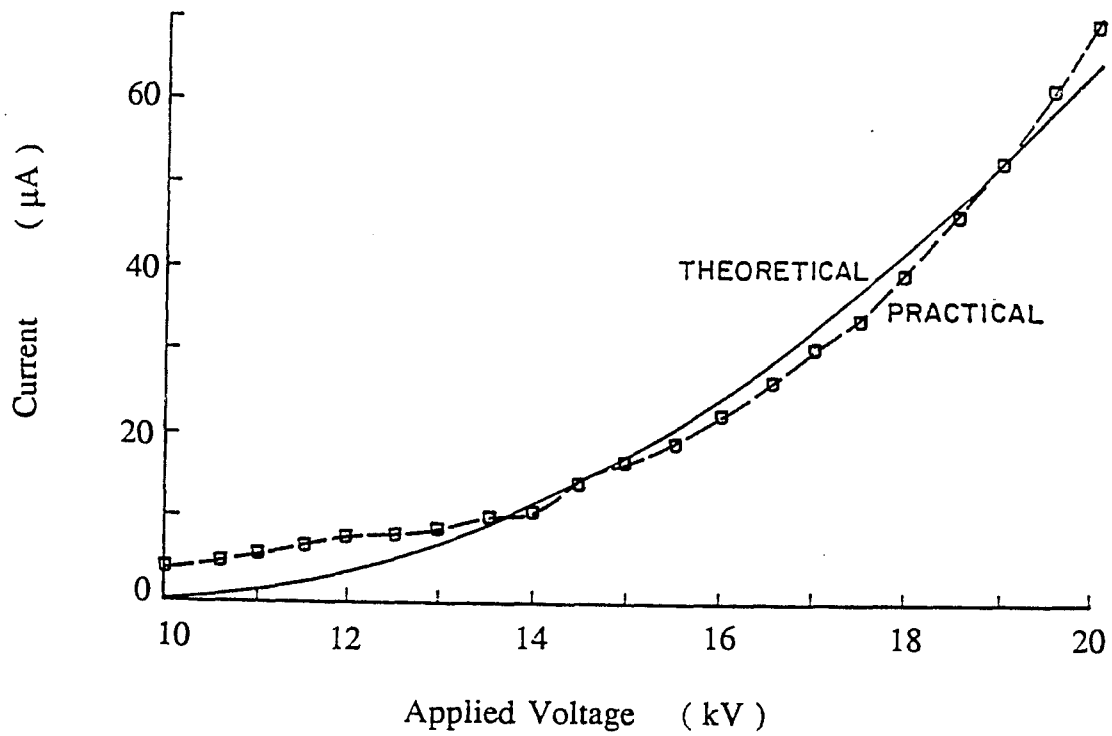

Figure 2.10 Theoretical and practical corona current vs applied voltage at room temperature and at atmospheric pressure for 2 cm electrode gap.

region is confined around the needle point and therefore y is very small in comparison with S the distance between the needle point and the collecting plate. The value of y for this furnace is measured to be 2 mm for 1 atm pressure and room temperature. The error in measurement cannot significantly affect the theoretical calculations, since y is much smaller than the value of S of 2 cm. The voltage to establish the onset of corona discharge, V_d, can be measured simply by increasing the applied voltage between the electrodes from zero until a rise in the corona current is detected. The value of V_d depends on the pressure and the temperature of the chamber and can also be determined from the curves shown in Figure 2.8 and 2.9. For this system, θ_c with 2 cm gap distance and 1 cm^2 plate area is calculated. The theoretical current as obtained from equation 2.3 is also drawn in Figure 2.10 for comparison with the practical current/voltage characteristic curve. For different gap sizes and different diameter of the needle tip the values of m will change. The value of m used in Figure 2.10 is 2.92. At higher temperatures, the values of V_d, y and μ changes and the current/voltage characteristic changes as can be seen from Figure 2.9.

In summary, two furnaces were designed and built to study the effects of point to plane corona discharge on oxidation of silicon in dry oxygen ambient at low temperatures. The stainless furnace was primarily used to study the rate of oxidation of silicon and the quartz furnace was used to

study the rate of oxidation of silicon and the quality of the oxide grown by this method. The corona generation was stable during the oxidation of silicon within the range of processing parameters such as temperature, pressure, and ion current values which were determined by studying the characteristics of the furnace. The measured corona current pressure for 2 cm electrode gap at room temperature and its corresponding calculated theoretical values were found to be in agreement.

The quartz furnace was also tested for corona generation in the hydrogen ambient for atomic hydrogen annealing purposes of SiO_2 films. To establish a corona current in the hydrogen ambient required lower voltage applied between the electrodes than the voltage necessary in the pure oxygen ambient.

CHAPTER 3

EXPERIMENTAL RESULTS

3.1 Introduction

In this chapter, results of negative point-to-plane corona discharge on oxidation of silicon samples in a dry ambient atmosphere at low temperatures in the range of 25°C to 500°C are given. First, the effect of negative point-to-plane corona discharge on silicon oxidation rate is considered. Second, the physical and electrical properties of the oxide films grown by this method are examined. The purpose of this study is to investigate these effects for developing a new technique for low temperature oxidation of silicon.

3.2 Effect of Corona-Discharge on Si Oxidation Rate

Series of experiments were performed to determine the effects of oxidation time, temperature, corona discharge current density, and substrate resistivity on the silicon oxidation rate using point-to-plane corona discharge in dry oxygen ambient. After oxidation of each sample with this method, the thickness and refractive index of the oxide films were measured using an ellipsometer.

For this purpose, a special stainless steel furnace as detailed in chapter 2 was utilized. The experimental set-up is shown in Figure 2.2. The stainless steel walls of the furnace were maintained near 8°C during the oxidation process by circulating chilled-water in the stainless steel tubing which was welded and epoxied to the outer surface of the furnace. The cooling arrangement was found to function satisfactorily even for runs involving many hours of oxidation at 500°C. Keeping the furnace wall at a low temperature minimizes the chance of the contaminants from the wall reaching the sample during the oxidation process which otherwise could affect the quality of the grown oxide film or may change the rate of oxidation. The gap between the needle point of the top electrode and the substrate holder bottom electrode was adjusted to 2 cm. The needle point of the stainless steel top electrode was measured to be 0.1 mm. The needle point was shaped from a 0.25 inch diameter stainless steel rod by precise machining. After proper adjustment of the gap distance between the electrodes, the top needle electrode is clamped in position by tightening the swagelok feed through mount. The latter is mounted on a ceramic insulator. The distance between the stainless steel electrode and the furnace wall was kept at least 2.5 cm. No leakage or sparking between the ceramic insulator and the furnace was observed.

The power supply used for this set of experiments had an output voltage of 13 kV. This inverter power supply had a 12 V dc input and its 13

kV dc output had 500 V peak to peak ripple voltage. The input voltage was supplied by dry batteries to isolate the high voltage power supply from the ac line for safety purposes. However, after a few hours of operation the battery output was found to decay with time, and hence, the high voltage output from the power supply decreased to about 9 to 10 kV. This change in output voltage decreased the corona current and affected the oxidation rate. A 12 V dc regulator was next connected to three 12 V batteries connected in series to maintain the high voltage constant for long periods of time during oxidation. After each oxidation process, the batteries were recharged. During oxidation of each wafer, a 13 kV dc signal was applied across the 2 cm gap between the needle point of the top electrode and the substrate holder bottom electrode. The substrate holder is grounded with the needle point maintained at -13.0 kV with respect to ground. The connection between the substrate holder and the wall of the furnace, which is grounded externally, is made by a thin platinum wire. Special 30 kV high voltage wires were used outside of the furnace for safety. The silicon wafer resided on the substrate holder and became a part of the back electrical contact. It is essential that the substrate holder remained a good electrical conductor in this highly oxidizing environment at temperatures between 25° C and 500° C. A molybdenum block with a thin layer of molybdenum disilicide on the outer surface was found to be appropriate as a substrate holder for many hours of oxidation though this

layer was found to eventually degrade on exposure to humid air. The molybdenum block was heated by two 400 W cylindrical heaters embedded into the block. Oxygen gas flow was regulated by a flowmeter. The chamber pressure was controlled by a convectron gauge installed at the outlet of the chamber.

The results of the work carried out on p-type (100) oriented silicon wafers with 0.1 Ω-cm resistivity are reported here. Prior to oxidation, each wafer was cleaned by heating in trichloroethylene, acetone and deionized (DI) water baths. In order to obtain a clean surface, the silicon wafers were soaked in 80°C nitric acid for 20 minutes, rinsed with DI water followed by dipping in a 10% hydrofluoric acid solution for one minute to strip out the oxide layer. Each wafer was then rinsed with DI water and dried with nitrogen gas and placed in a Hummer IV sputter coater using argon gas. The back surface of each wafer was coated with a thin layer of either platinum or gold. The purpose of this thin coating was to prevent oxidation of the back surface of each sample and also to provide a uniform conducting plane at the bottom electrode during the corona-assisted oxidation. For room or low temperature oxidation work, this back metal layer is not likely to pose a significant contamination problem. In all of these steps, special care was implemented to have a minimum amount of native oxide resulting from exposure to ambient air. Prior to the actual oxidation, about 1 to 1.5 nm of oxide was measured by an ellipsometer.

The oxidation of each wafer was carried out by applying a 13 kV dc signal across a 2 cm gap between the needle point top electrode and the substrate. The maximum oxide thickness obtained after one hour of oxidation as a function of substrate temperature is shown in Figure 3.1. The oxide thickness values of 6 nm and lower were determined using an ellipsometer and the appropriate look-up tables, since nomogram cannot be used for determining very thin oxide thicknesses. High purity MOS grade dry oxygen was used as the gas ambient and the corona current was 17 μA.

It is clear from Figure 3.1 that the rate of oxidation by this technique is a function of substrate temperature for a constant corona current. As seen from the furnace characteristics depicted in Figure 2.8 at a constant value of the applied voltage, the corona current increases with decreasing chamber pressure at a constant temperature. Also, from Figure 2.9, at a constant pressure the corona current increases with increasing temperature for a given applied voltage. Depending on the needle shape and the applied voltage, the current may decrease to the point of flickering and finally cease to exist as the chamber temperature is reduced. In order to maintain a constant ion beam current of 17 μA during oxidation, the pressure in the oxidation chamber was adjusted as the substrate temperature was varied as illustrated in Figure 3.2. As an indication of enhancement of the rate of oxide growth, the 23 nm thick oxide film grown in one hour by this method at 472°C would have required about 58 hours by dry

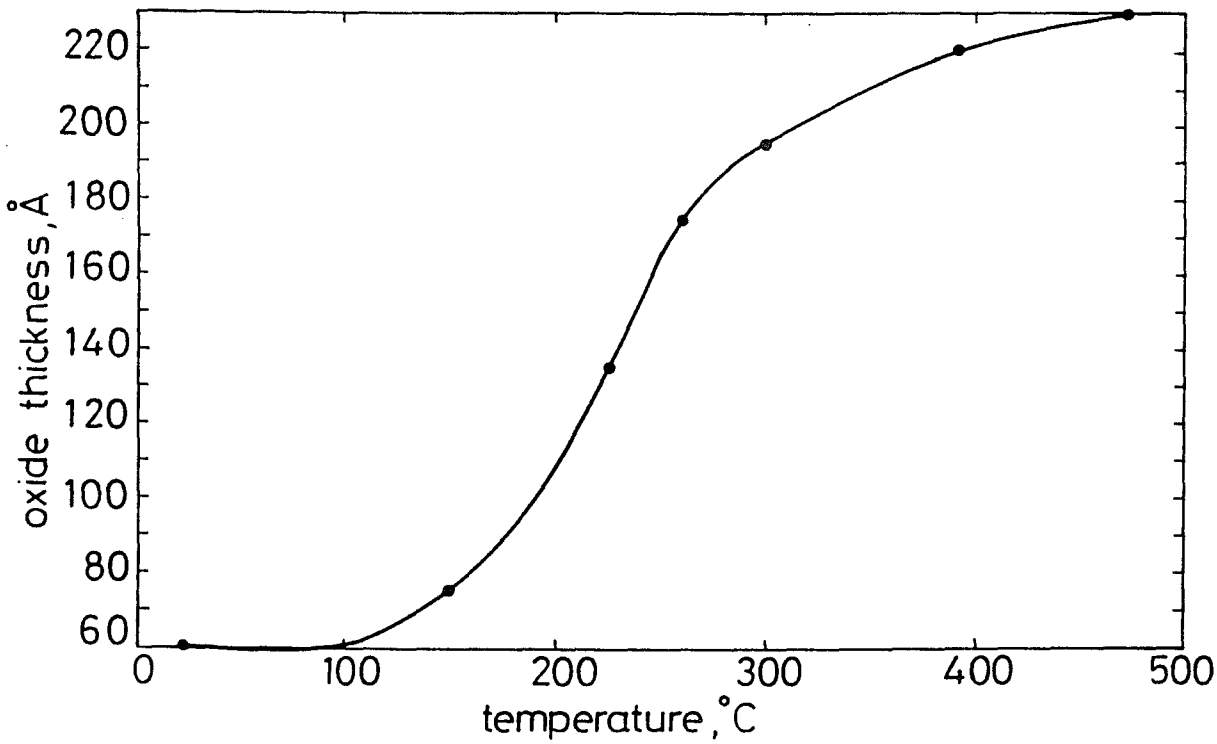

Figure 3.1 Thickness of grown oxide as a function of substrate temperature for one hour growth time at 17 μA current.

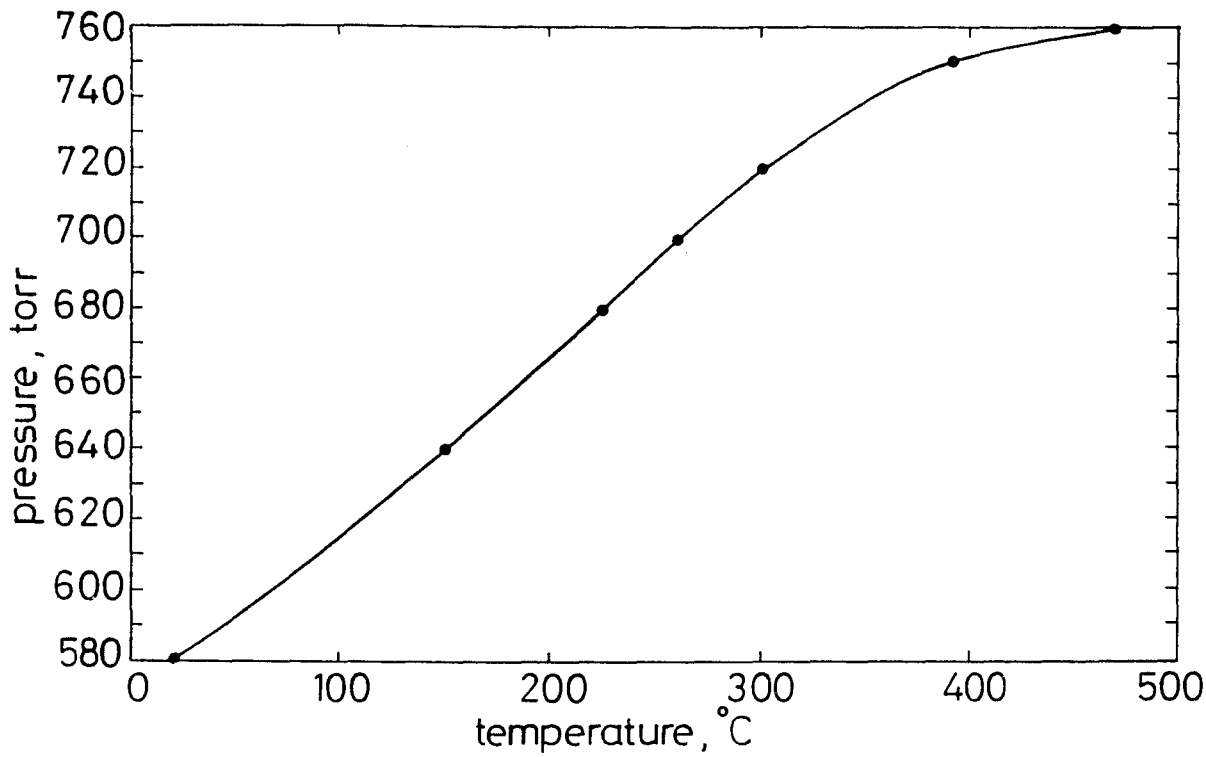

Figure 3.2 Growth pressure as a function of substrate temperature for a constant current of 17 μA.

thermal oxidation technique at 700° C. The oxide thickness and the refractive index of the samples grown at 472° C for different oxidation times, as measured by the ellipsometer, are shown in Figure 3.3. As the thickness of the oxide increases, its refractive index becomes closer to the value 1.46 obtained for the high-temperature thermally grown oxides. The uniformity of a 12 nm thick oxide film obtained in this work was seen to be within ±20 % across a 2.5 cm diameter wafer. The oxide thickness has its maximum value right below the upper needle electrode, and it decreases towards the edges of the wafer. The uniformity of the grown film depends on the ionic current density distribution. The current density distribution is related to the gap distance between the needle point and the collecting electrode plane and also depends on the needle shape and its point diameter for a given pressure and temperature.

The rate of corona oxidation of silicon samples were also examined for oxides grown in the quartz furnace of Figure 2.3. The thickness of each wafer was measured with Microsense 6033T manufactured by ADE Corporation and the resistivity of each wafer was measured with a Four Point Probe model FPP-100 from Veeco Instruments Inc.. The resistivity of these wafers was measured to be 30 Ω–cm. In this experiment the silicon wafers were cut to a 1 cm by 1 cm square dices by using a wafer scriber Model 2800 from Semiconductor Equipment Corp. to fit on the substrate holder. The gap distance between the needle point electrode and

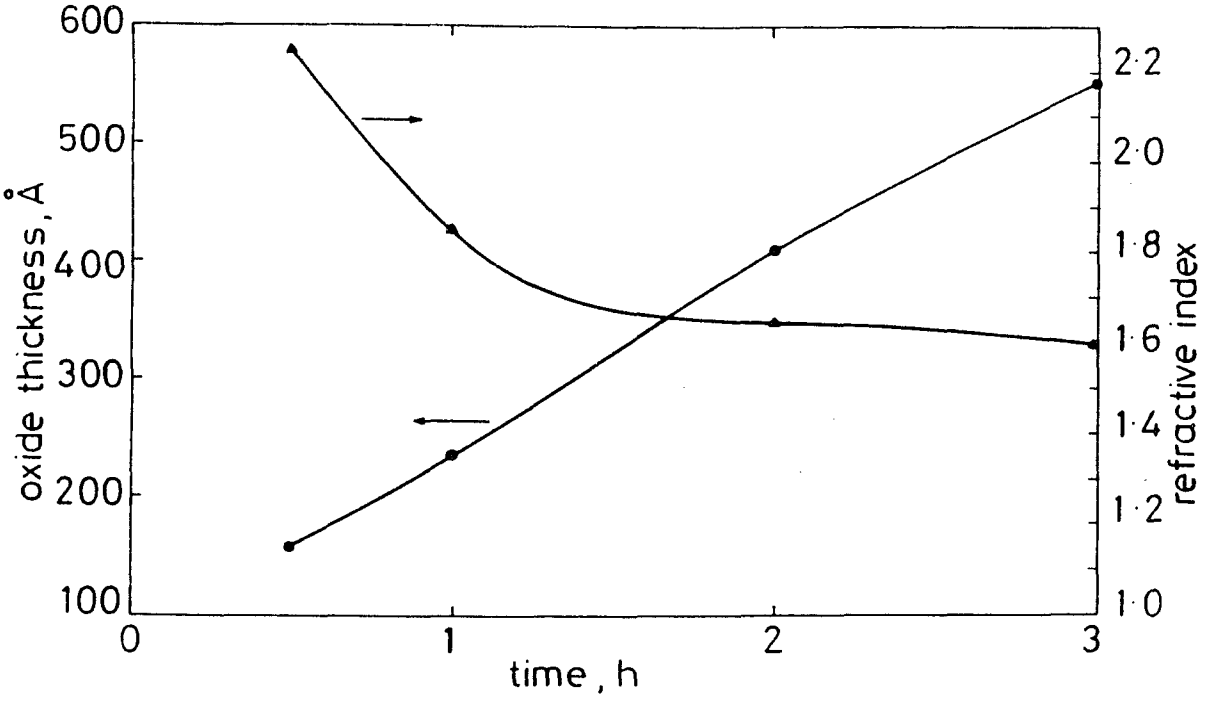

Figure 3.3 Oxide thickness and refractive index as a function of oxidation time for substrate temperature of 472 °C.

the substrate holder as the second electrode in this case was adjusted to 1 cm. These samples were cleaned prior to oxidation by the same procedure described earlier. The temperature of oxidation was varied from 25 to 500°C in this study. The corona current of 17 μA and 1 atm pressure were used. As the current and the pressure were kept constant, the applied voltage across the electrodes changed automatically in the 3.5 kV to 8.5 kV range by the power supply as the oxidation temperature was varied from 25°C to 500°C. This effect is shown in Figure 3.4. The grown oxide thicknesses and their refractive indices as a function of temperature of oxidation are shown in Figure 3.5. The corona oxidation of several silicon samples with different resistivity values from 0.1 Ω–cm to 50 Ω–cm were also carried out in a similar fashion. However, resistivity of the starting material was found to have no significant effect on the rate of oxidation of these samples.

As the temperature of oxidation was increased from 25 to 500°C, two important effects were observed. First, the rate of oxidation was seen to be significantly higher than the conventional thermal oxidation rate for silicon. This effect is shown in Figures 3.1 and 3.5. The oxide thickness was measured with an ellipsometer. As illustrated in Figure 3.5, approximately 100 nm of oxide film is grown in one hour at the oxidation temperature of 400°C and 12 nm oxide thickness is measured at 100°C. The oxidation rate is seen to decrease for oxidation temperatures higher than 500°C.

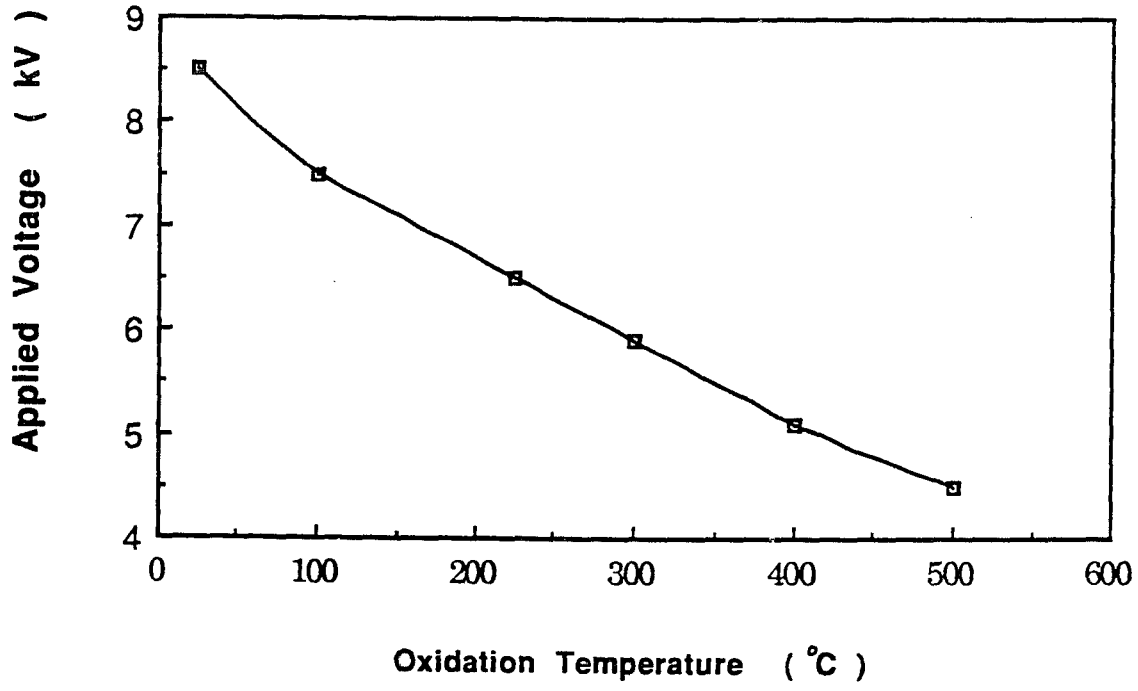

Figure 3.4 Plot of applied voltage between the electrodes vs the oxidation temperature for gap distance of 1 cm during the corona oxidation at one atmosphere pressure.

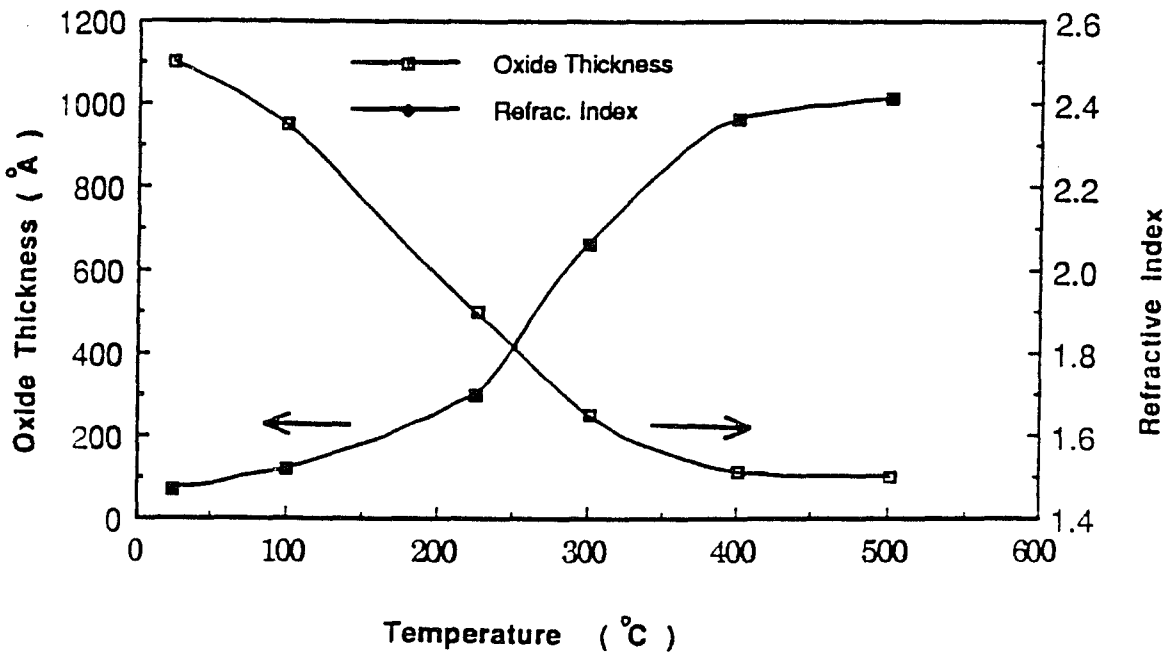

Figure 3.5 Oxide thickness and refractive index as function of oxidation temperature for oxidation time of one hour for 1 atm pressure and 17 μA corona current.

However, the rate of oxidation using point-to-plane corona discharge at a given temperature is always significantly higher than the rate of oxidation by conventional thermal oxidation at the same temperature. Second, the refractive index of the grown oxide by this method improves at the higher growth temperatures and for the thicker grown oxide films. As seen from both Figure 3.1 and Figure 3.5, the rate of oxidation of this process is a strong function of temperature. The oxidation rate first increases and then decreases with the oxidation temperature. The latter experimental observation may support the concept of ionic oxygen as a dominant oxidation species in the low-temperature oxidation of silicon. The temperature of transition from a dominant ionic to a molecular species is estimated to be around 500° C at oxygen pressure of 1 atmosphere.[42] However, Modlin and Tiller report this transition temperature as high as 850°C.[30–31] At temperatures higher than 850°C, the dominant oxidation species are oxygen molecules. At temperatures between 600°C and 850°C both ionic and neutral species are important, but for temperature lower than approximately 600°C only ionic species are important since the diffusion coefficient of the neutral oxygen is very small.

In summary, the rate of silicon oxidation using a point-to-plane corona-discharge in dry oxygen ambient at temperatures less than 500° C is found to increase significantly in comparison with conventional thermal oxidation process. This enhancement suggests the involvement of charge

species in thin film low-temperature oxidation of silicon as dominant oxidation species. The refractive index of the oxide grown by this technique approaches the value obtained from high temperature thermally grown oxide as the thickness of the film increases.

3.3 Electrical Quality of the Grown Oxide

As a first attempt to investigate the quality of the grown oxides, the electrical quality of the SiO_2 film grown on silicon with the stainless steel furnace as described in section 3.2 was examined. The capacitance-voltage (C-V) curves of the oxide grown in this furnace at temperatures higher than the room temperature showed no distinct accumulation and inversion regions. The walls of the furnace were kept cool during oxidation by circulating chilled-water. However, the contamination from the stainless steel heaters inside the oven for the oxide films grown at temperatures higher than room temperature is a distinct possibility in this growth set up. The electrical quality of the oxide grown at room temperature is examined first. These oxides films should have minimal contamination from the furnace walls and the substrate heaters. Also, at higher growth temperatures, some contamination from Au or Pt back layer may be present. However, at these low temperatures of less than 500 °C and atmospheric pressure oxidation, this possibility seems to be small. The films grown in the quartz furnace will be used to study the electrical qual-

ity of the oxide grown at temperatures higher than the room temperature. The measured data were obtained by using software which is written to link a personal computer Zenith-100 to HP 4275A multi-frequency LCR meter via an IEEE communication bus. The condition of measurements such as dc bias voltages, ac signal frequency, and the time sequences between each dc biasing step could be varied by using another software program. For C-V measurements, biasing dc voltage steps were changed every 250 msec. A 50 mV small signal ac was superimposed on the dc bias. For each data point on the C-V curve, the measurement was repeated 10 times and then averaged.

3.3.1 The Electrical Quality of the Oxide Grown at Room Temperature

The electrical quality of the oxides grown at room temperature on silicon wafers using negative point-to-plane corona discharge in dry oxygen ambient is examined here. These oxides were grown in the stainless steel chamber. The silicon samples were 11.3 mil thick p-type with boron doping of 3.2×10^{14} cm^{-3}. For 17 μA corona discharge current, the pressure of the oxidation reactor was adjusted to approximately 600 torr. After one hour of oxidation of the samples at 25°C in dry oxygen ambient by this technique, 7.5 nm of oxide thickness was obtained as measured by an ellipsometer. Aluminum was evaporated on the grown oxide as the

gate electrode for the MOS capacitors. The aluminum evaporated area of each capacitor was 4.56×10^{-3} cm^2. A HP 4275A multi-frequency LCR meter is used for the capacitance/conductance vs voltage measurement at different frequencies of 2 MHz, 1 MHz, 400 KHz, 200 KHz and 100 KHz.

The C-V curves are shown in Figure 3.6. The value of the capacitance in accumulation region was seen to decrease as the frequency of the ac signal was increased. Series resistance can cause significant reduction in the capacitance values in accumulation region especially at high frequencies. Also, a high value of series resistance will mask off the interfacial properties which can be extracted from the C-V characteristic curves. The capacitance shown in Figure 3.6 has series resistance. There are various sources for series resistance such as the probe contact resistance to the top capacitor plate, the top plate and back contact resistances, a dirt film between the pedestal and the back contact of the sample, the resistance of the quasi-neutral bulk silicon and extremely nonuniform doping in silicon underneath the oxide.[43] The series resistance is determined by biasing the MOS capacitor in strong accumulation region. In this region, the equivalent circuit of the MOS capacitor is simplified to contain only the series resistance R_s and the oxide capacitance C_{ox}. From simple RC circuit analysis, the values for R_s and C_{ox} in terms of the measured parallel capacitance and conductance values of C_m, and G_m in strong accumulation

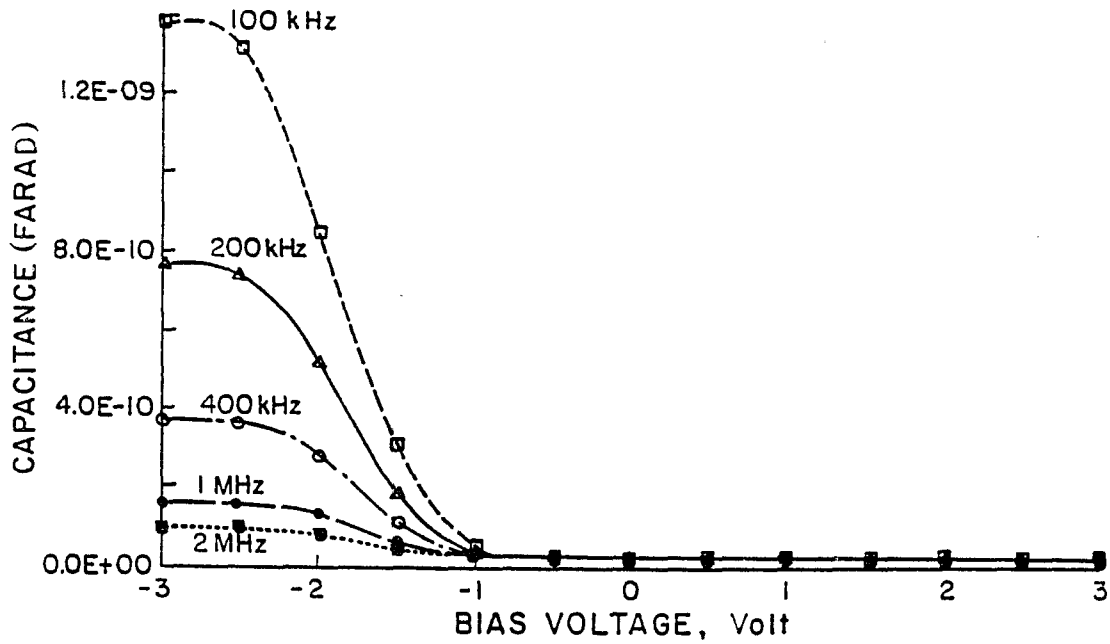

Figure 3.6 Capacitance as function of dc bias voltage for different values of signal frequency.

region of angular frequency of ω can be written as:

$$C_{ox} = C_m + \frac{G_m^2}{\omega^2 C_m} \text{ , and } R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2}. \quad (3.1)$$

Higher values of R_s and ω imply a lower value for oxide accumulation capacitance, C_{ox}. The series resistance, R_s, of this sample is calculated to be 377 Ω which is rather high. This high value for the series resistance on these samples is attributed mostly to the back contact and the bulk resistance. The back contact resistance can be reduced further by improving fabrication steps. The bulk resistance can be reduced by reducing the substrate thickness by a lapping process. The effect of series resistance can be taken into account on the capacitance value for each value of the applied bias voltage. The following equations can be used to obtain the corrected capacitance C_c and equivalent parallel conductance G_c under all bias situations:[43]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{a^2 + \omega^2 C_m^2} \quad (3.2)$$

and

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2) a}{a^2 + \omega^2 C_m^2} \quad (3.3)$$

where $a = G_m - (G_m^2 + \omega^2 C_m^2) R_s$ and where C_m and G_m are the parallel capacitance and the parallel conductance values measured across the MOS capacitor terminals. After the effect of series resistance is taken into

account, the corrected capacitance C_c in the accumulation region will be the same as the oxide capacitance C_{ox}.

Figure 3.7 shows the normalized capacitance value C_c/C_{ox} plotted as a function of the biasing voltage. As seen from this figure, a flat-band voltage shift of about 1.5 volts is obtained for these oxide films grown at 25°C. The transition between accumulation to strong inversion is well defined in the C-V characteristic curves of these samples processed at room temperature. The normalized capacitance value C_c/C_{ox} goes above 1.0 at -3 volt bias voltage because in these measurements the capacitances measured around this point increased slightly before it dropped to its final value as shown in Figure 3.6. The amount of this increase is higher at lower measurement frequency. This effect is somewhat exaggerated since a third order polynomial approximation is used between the data points in these plots. The source of this increase may be an artifact of the measurement system used. In Figure 3.7, ideal C-V characteristic curve is also shown for comparison. The ideal C-V curve is obtained numerically by a computer program which is based on the equations given in the Appendix.

The shift in the flat-band voltage shown in Figure 3.7 corresponds to a presence of positive charges at the oxide-silicon interface. A bias stress test for detecting the presence of mobile ions was also performed. The samples were stressed by applying an electric field of approximately 0.5

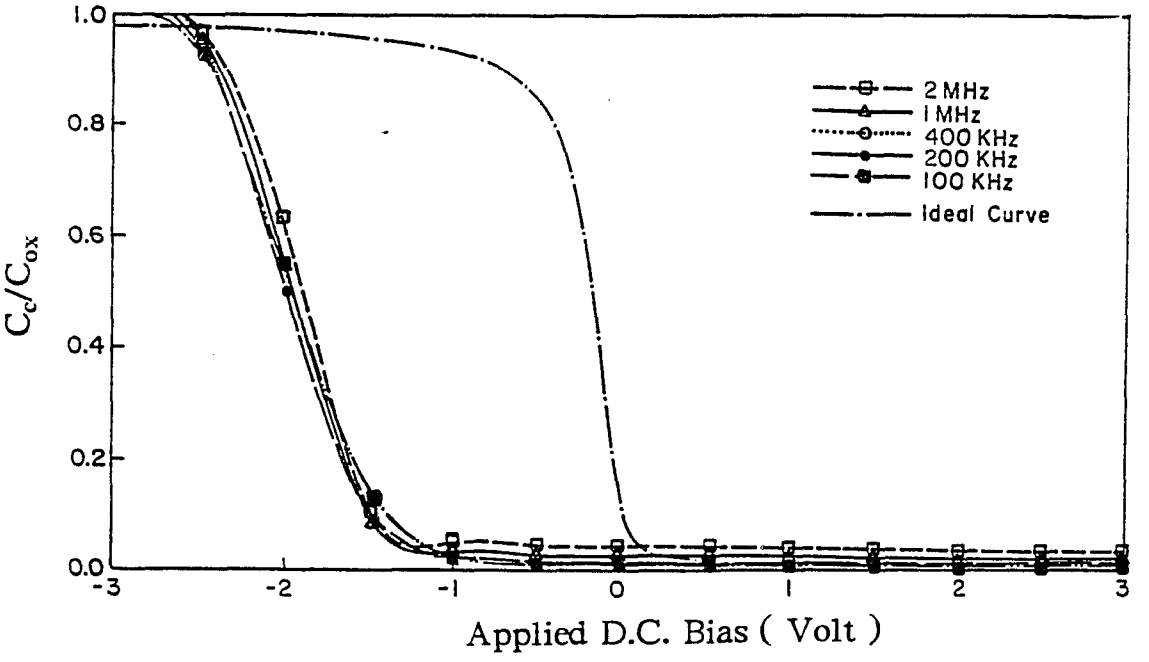

Figure 3.7 C_C / C_{ox} ratio at 2 MHz, 1 MHz, 400 kHz, 200 kHz and 100 kHz for a 7.5 nm oxide grown at 25 °C. The ideal curve is shown for comparison.

MV/cm magnitude in both the positive and the negative bias directions across the MOS capacitor plates at 150°C for an interval of 25 minutes. The result of this stress test on some samples indicated the existence of mobile charges in the oxide. However, for other samples under study, the high frequency C-V characteristic curve shifted towards left during both the positive and negative polarity of applied stress as shown in Figure 3.8. The shift in the C-V characteristic curves towards left in both cases of stress tests indicates injection of oxide charges along with ionic motion instability in these structures.

The dc I-V characteristic curve of a MOS structure measured at room temperature is shown in Figure 3.9. When the aluminum plate of the capacitor was biased negative with respect to the substrate, the measured value of the current was substantially higher than the measured current value under positive bias. This difference in the measured current can be attributed to the presence of positive charges in the oxide film. If positive charges are present in the oxide near the oxide-semiconductor interface, the effective field that appears across the oxide film is higher under negative gate bias than the case when there is no charge present in the oxide. This results in the higher current with negative gate bias.

Temperature dependency of the current density through the oxide was also examined. In order to obtain the actual oxide current density as a function of the voltage across the oxide, the effect of flat-band voltage

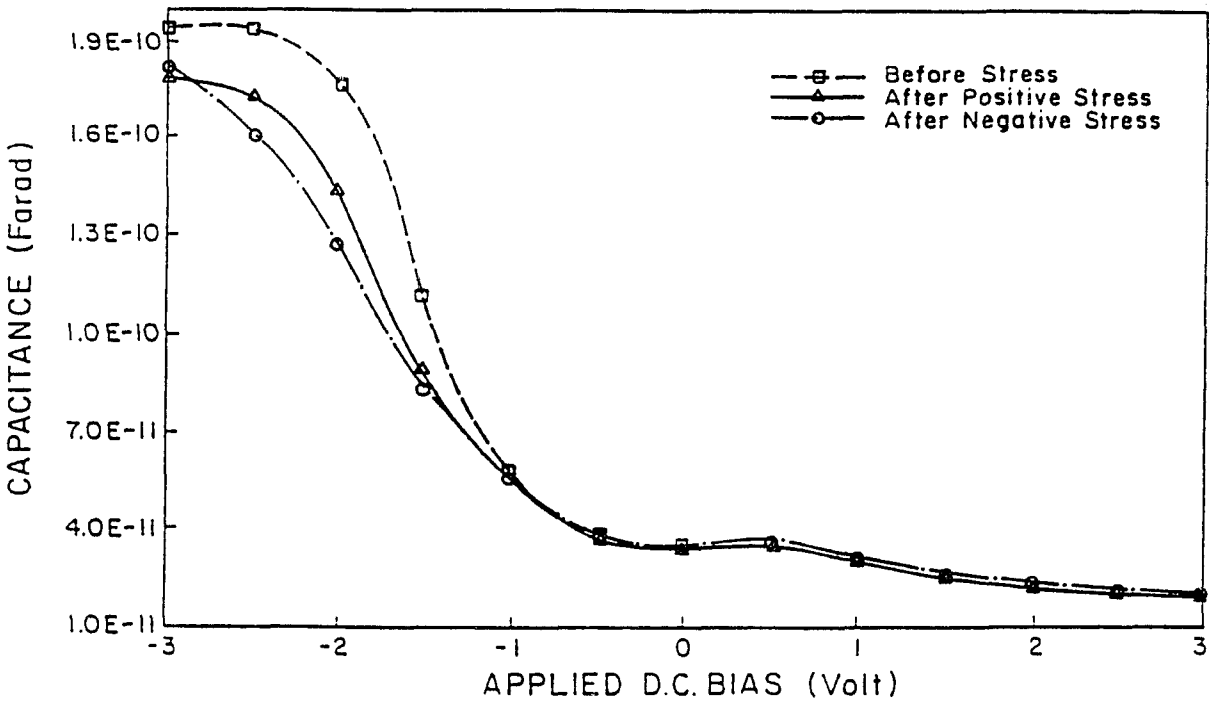

Figure 3.8 C-V curve shift after positive and negative bias temperature stresses.

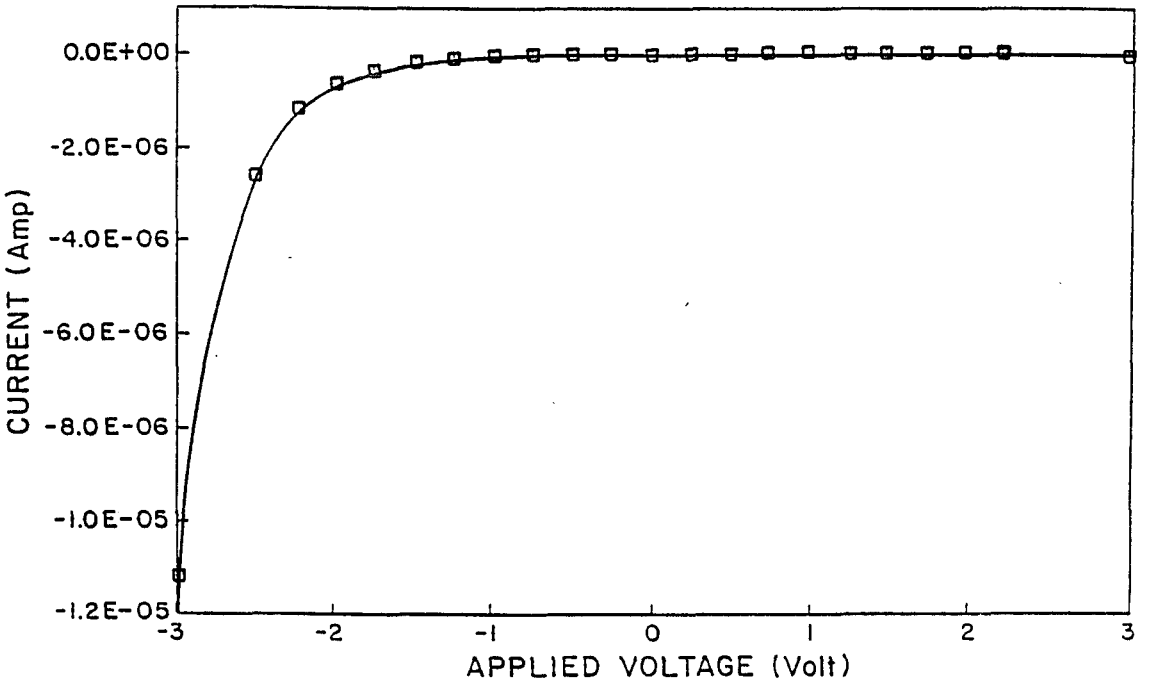

Figure 3.9 Current vs applied gate voltage at room temperature on an MOS structure with 7.5 nm oxide grown at 25°C. The device area is 4.56 x 10^{-3} cm^2.

shift and the surface potential at different temperatures need to be considered. In this calculation, it is assumed that the flat-band voltage value will not significantly change in the temperature range used. This assumption is verified by comparing the C-V characteristic curves measured at 100 °C and room temperature which are shown in Figure 3.10. There is a dip in the C-V characteristic curve of the sample under test at 100°C for dc bias voltages in the -2 to -3 V range. This effect can be attributed to excessive leakage current at this higher measurement temperature. The surface potential of the MOS capacitor at different temperatures was calculated. The logarithm of the device current density j in amperes versus the square root of the voltage in volts appearing across the oxide for several temperatures is shown in Figure 3.11. In this semi-logarithm graph at higher values of the voltages, the current density curves are approximately linear with respect to the square root of the oxide voltages at different temperatures. This indicates the emission process is either Schottky emission or Frenkel-Poole emission. A plot of $\ln(\frac{j}{T^2})$ versus $\frac{1}{T}$ does not yield appropriate linear relationship for Schottky emission. Hence, for these voltages, the field-enhanced thermal excitation of trapped electrons to the conduction band can be taken to be the dominant current transport mechanism. The major component of charge transport through the oxide shows a behavior similar to the Frenkel-Poole emission mechanism. At

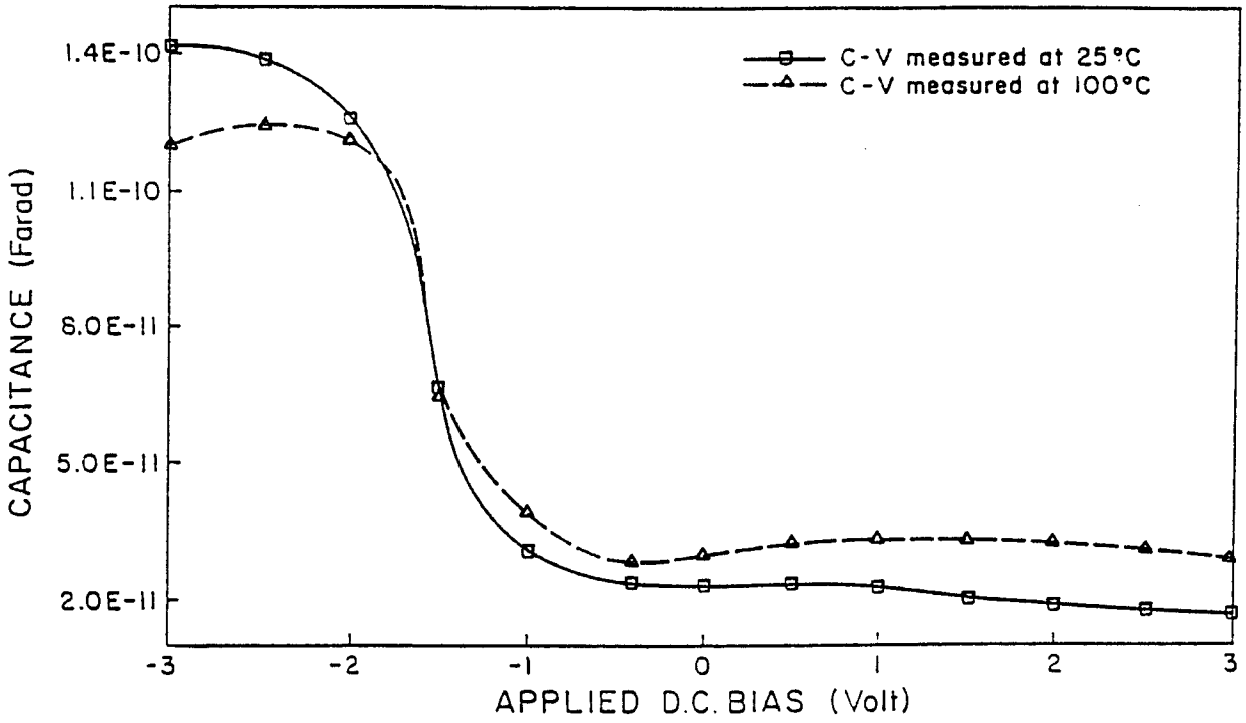

Figure 3.10 Plot of C-V curves measured at room temperature and at 100°C.

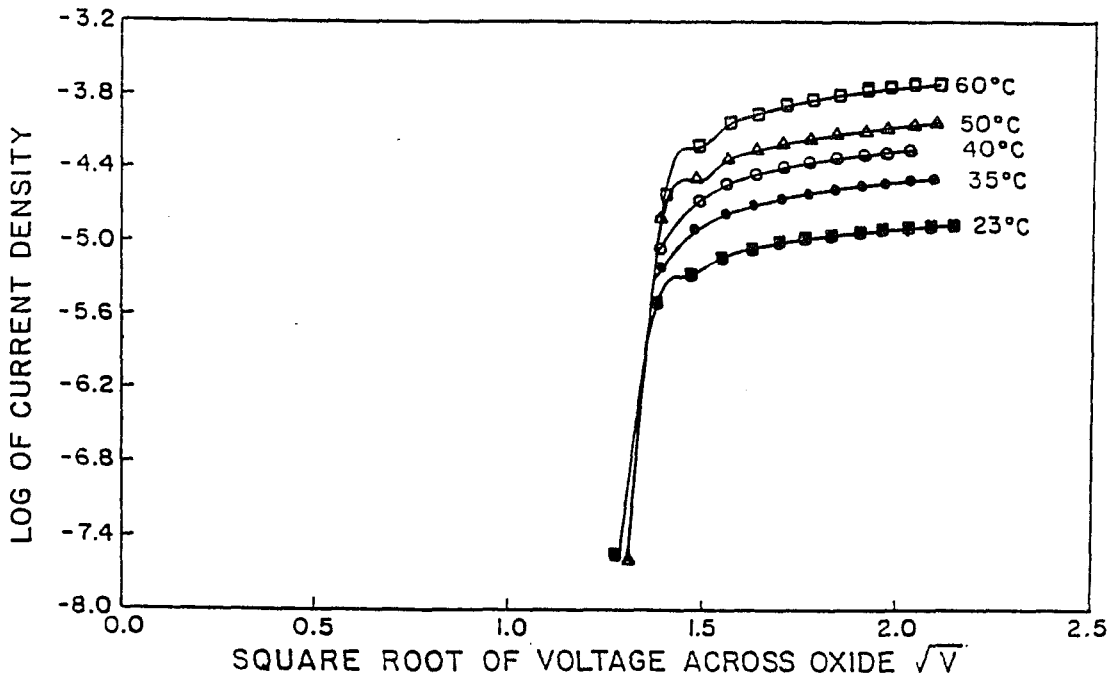

Figure 3.11 Plot of log(j) vs $\sqrt{V}$ measured at 23, 35, 40, 50, and 60°C temperature for MOS structure with 7.5 nm oxide. Aluminum plate is positive with respect to the substrate.

lower oxide voltages, these curves are almost temperature independent and have the strongest dependence on the applied voltage. This is characteristic of tunneling. The latter is caused by field ionization of trapped electrons into the conduction band and the former by electrons tunneling between the metal and the insulator conduction band.[44–46] The leakage current through the oxide is substantially higher when the aluminum plate is biased negative with respect to the substrate than when the aluminum plate is biased positive with respect to the substrate. The logarithm of the current density as a function of the square root of the voltage across the oxide for applied negative gate voltages is plotted in Figure 3.12. From this figure, it appears that for negative gate voltages, the tunneling process is dominant since the current density is not dependent strongly on temperature and is a strong function of the voltage appearing across the oxide.

3.3.2 The Effect of Current Density During Oxidation

A (100) silicon sample was oxidized at room temperature in a quartz furnace and atmospheric pressure in dry oxygen ambient by applying corona-discharge current of 15 μA for two hours. The needle to bottom electrode gap distance was 1 cm. Oxide film thickness of 10 nm was measured with an ellipsometer at the center of the sample where the ionic current density was the highest. The C-V curves of capacitors located at different areas of the sample were measured for comparison. Since, the 1

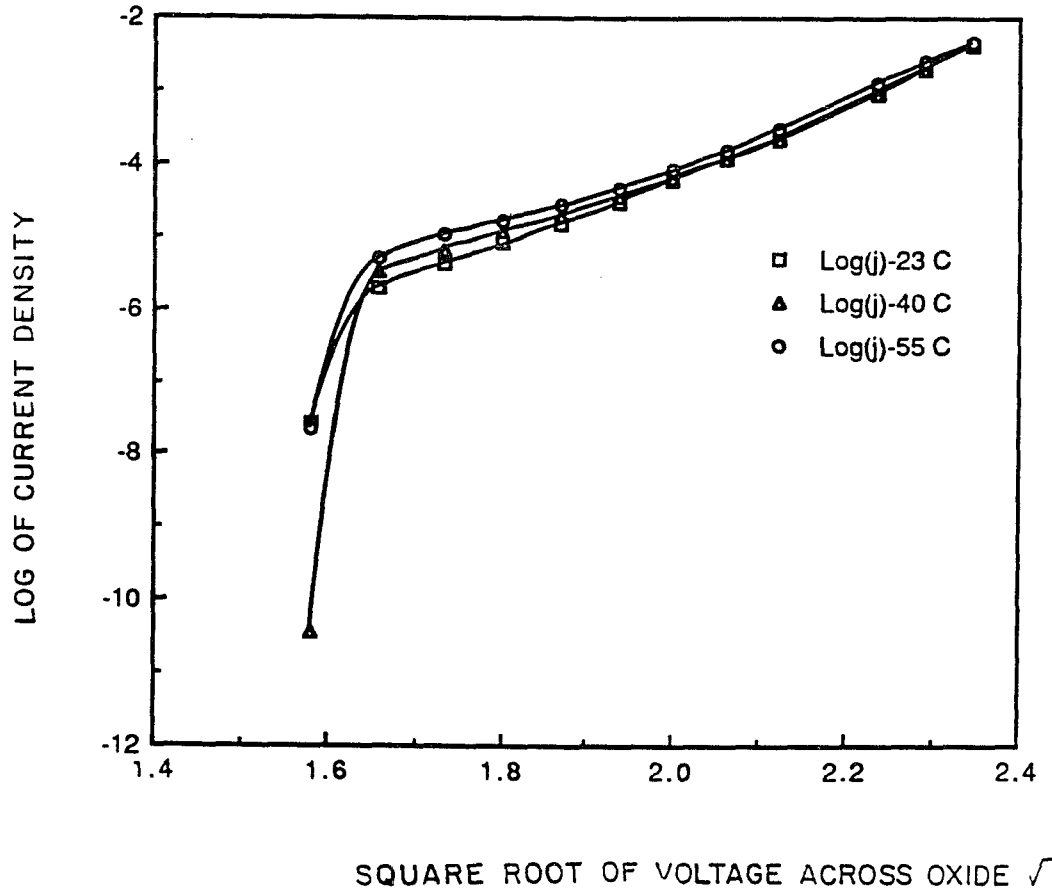

Figure 3.12 Plot of log(j) vs $\sqrt{V}$ measured at 23, 40, and 55°C temperature for MOS structure with 7.5 nm oxide. Aluminum gate is negative with respect to the substrate.

cm electrode distance is relatively small, the variation of the oxide thickness across the sample can be observed from the measured values of capacitances in accumulation. As shown in Figure 3.13, the capacitor #3, which is located near the center of the sample had the smallest value for accumulation capacitance while capacitor #4 located at the sample edge had the highest value. Sample #2, located in the middle, has an intermediary value for the accumulation capacitance. Also, it was observed that the capacitor leakage current decreased as its location was removed farther from the center of the sample. As seen from Figure 3.14, capacitor #4 had the lowest leakage current under accumulation while capacitor #3 had the highest magnitude for the leakage current. As seen from Figure 3.13, the shift in the flat-band value decreases with decreasing corona-discharge current density. This can be seen from comparing Figures 3.15 and Figure 3.16. Capacitor #4, in Figure 3.16, which is closer to the sample edge has a somewhat smaller negative shift in its flat-band voltage than the capacitor #2 in Figure 3.15, which is closer to the center of the sample. The current density of the ion beam generated during corona oxidation decreases for the locations away from the sample center which is positioned right under the needle point. Therefore, as the corona-discharge current density decreases the rate of oxidation decreases but the electrical quality of the grown oxide improves. This effect can also be seen from Figure 3.17 where two other samples are oxidized with two different

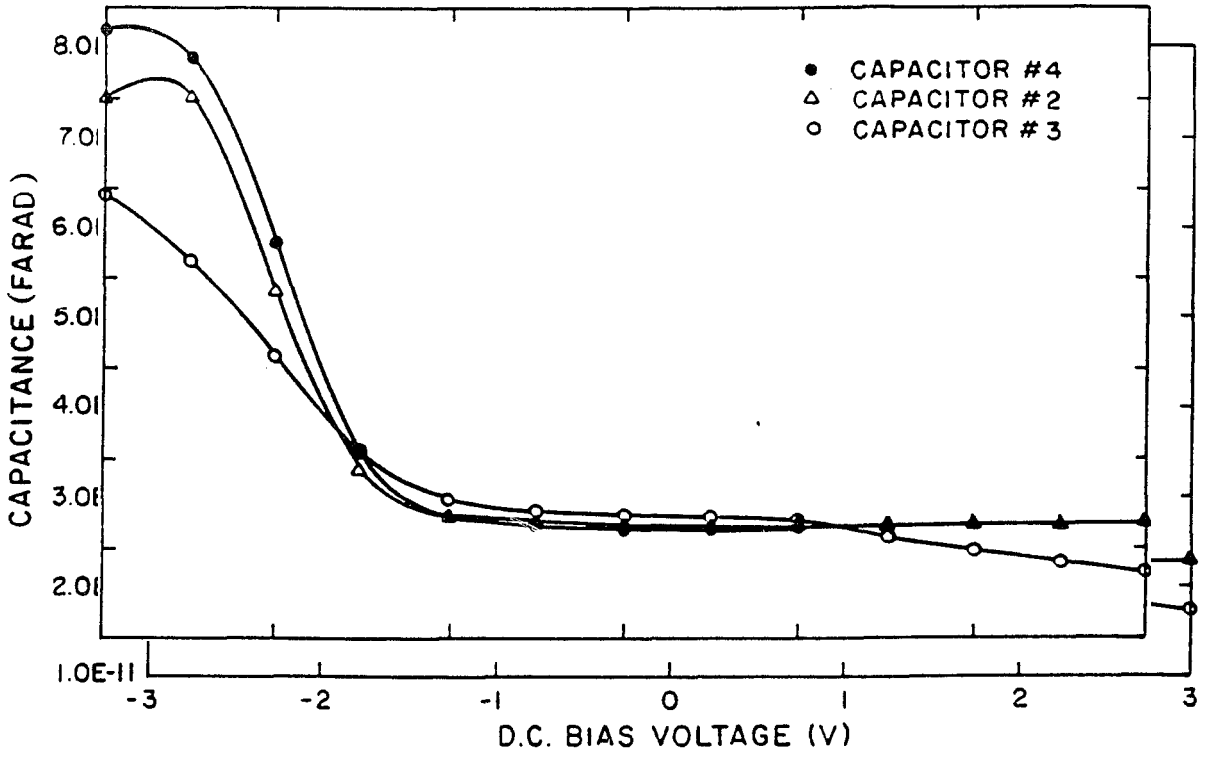

Figure 3.13 C-V characteristic curves for capacitors #3, #2 and #4 located from the center of the sample towards the edge. The measurement frequency is 1 MHz.

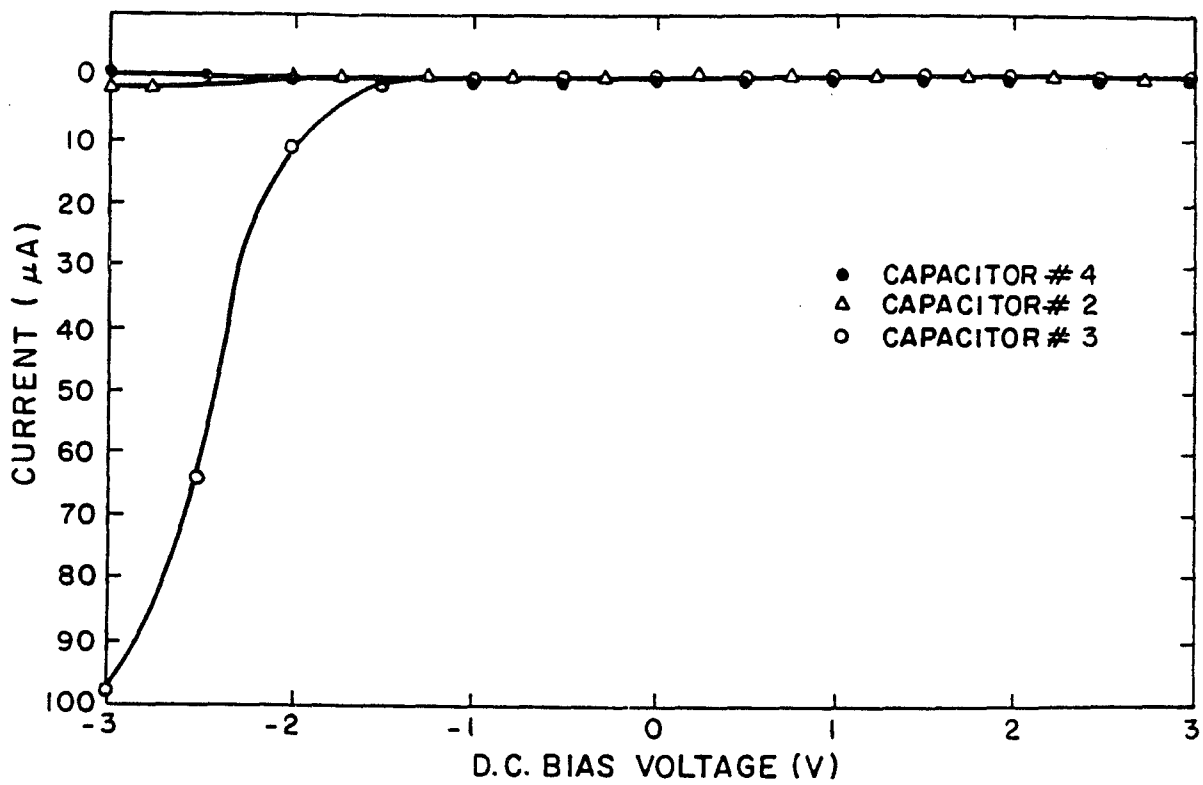

Figure 3.14 I-V characteristic curves for capacitors #3, #2 and #4 located from the center of the sample towards the edge.

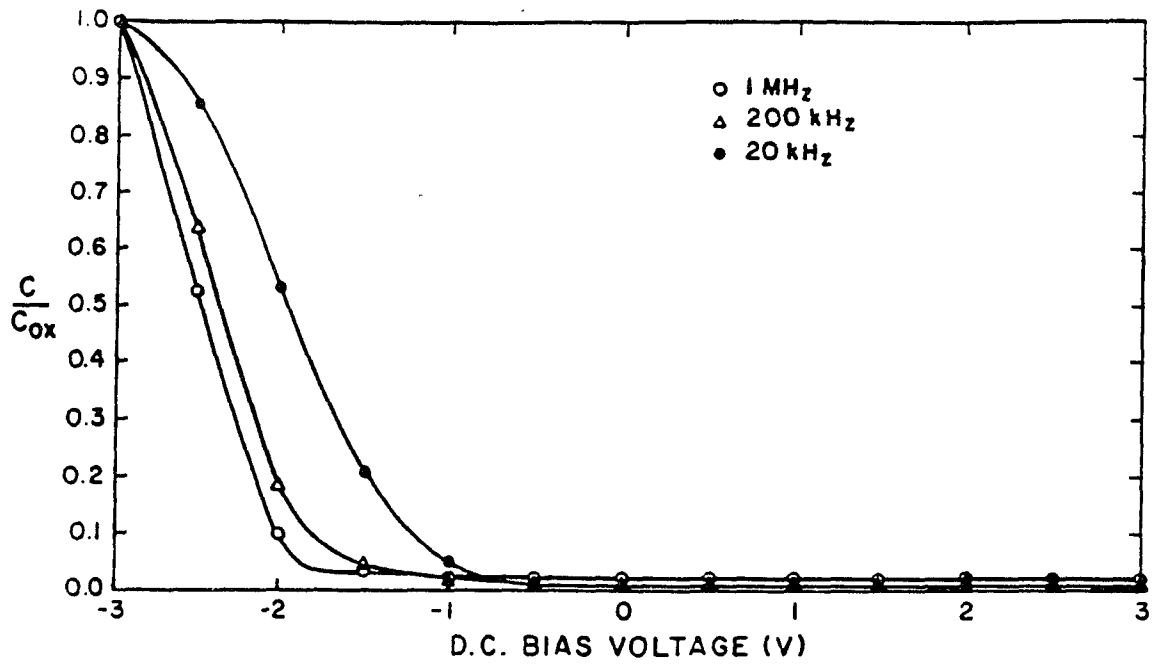

Figure 3.15 C/C_{ox} ratio at 1 MHz, 200 kHz and 20 kHz for capacitor #2.

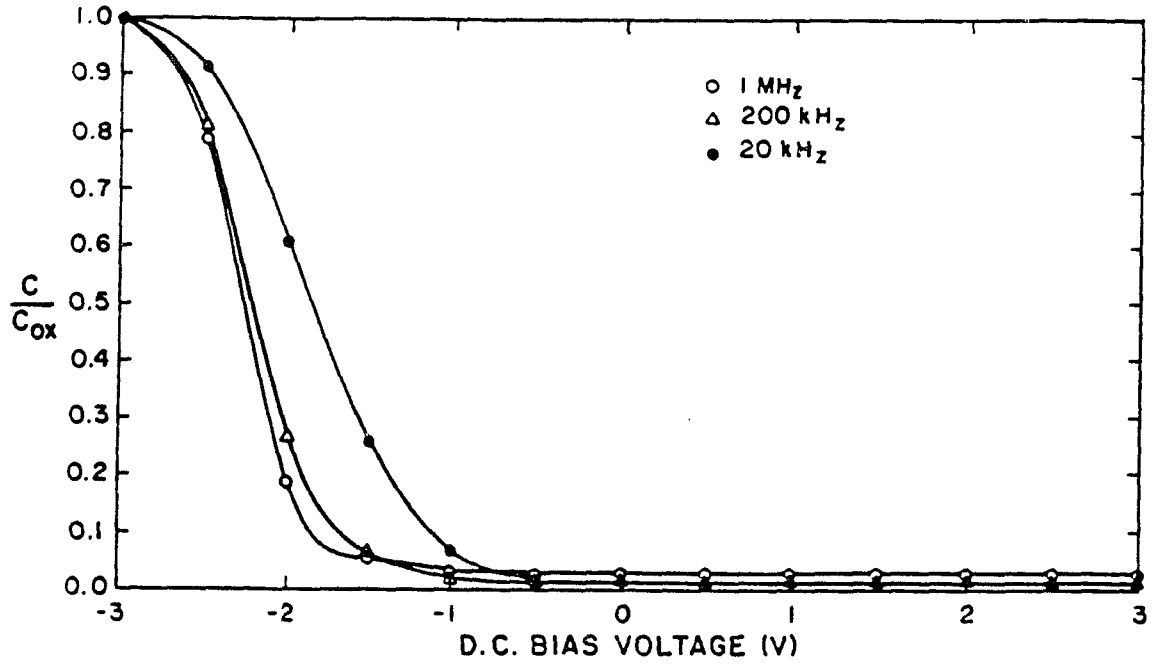

Figure 3.16 C/C_{ox} ratio at 1 MHz, 200 kHz and 20 kHz of capacitor #4.

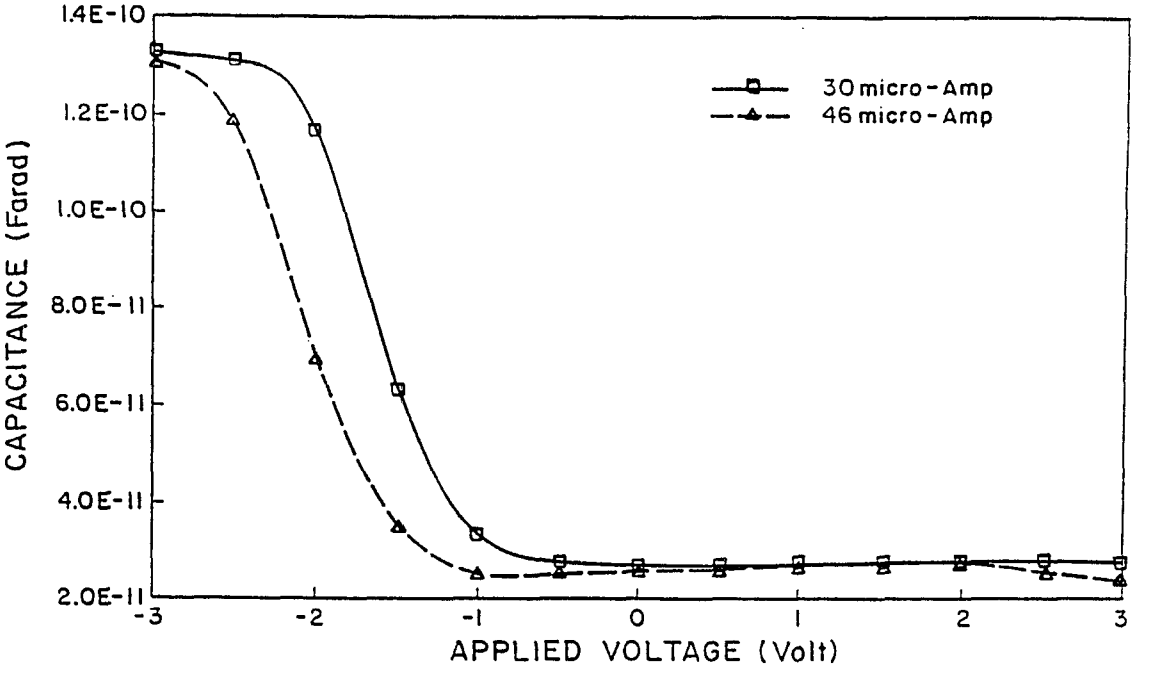

Figure 3.17 Shift in the value of the flat-band voltage shown on the C-V curves measured at 1 MHz frequency signal for two different values of corona-discharge current.

corona current densities. The corona oxidation of these two samples are carried out for one hour at room temperature with atmospheric pressure and 1 cm gap between the electrodes in the quartz furnace. Both these samples were located at the center of their respective substrates. The oxide grown with 30 μA corona-discharge current has less shift in the flat-band voltage than the oxide grown with 46 μA corona discharge current during the oxidation process.

3.3.3 The Electrical Quality of the Oxide Grown at Temperatures Higher than Room Temperature

In this section the electrical quality of the oxides grown at temperatures higher than room temperature using negative point-to-plane corona-discharge are examined. The samples are oxidized for one hour in dry oxygen with substrate at different temperatures in the quartz furnace. The corona discharge current was kept constant at 17 μA for all the samples studied here. The oxidation pressure was 1 atm. The applied voltage was automatically adjusted to have a constant discharge current at each oxidation temperature. The applied voltage between the top electrode and the bottom electrode for 1 cm gap is a function of oxidation temperature as shown in Figure 3.4. As the temperature of the oxidation chamber increases, the generation of electrons from the needle point in the ionization region increases along with an increase in the ion mobility in the drift

region. Hence, the voltage necessary to maintain a given corona current decreases. The grown oxide thicknesses and their refractive indices as a function of temperature of oxidation are shown on Figure 3.5. The thickness of oxide grown in 1 hour increases as the corona oxidation temperature increases and begins to level off at about 500 °C. Also, from Figures 3.1 and 3.5, it can be seen that the amount of oxide grown in 1 hour with 1 cm electrode gap is about four times the amount of oxide grown with 2 cm electrode gap at 400°C oxidation temperature. The flat-band voltages of the MOS samples showed a tendency to move towards more positive voltage values as the oxidation temperature was increased. This effect is shown in Figure 3.18. However, within a small range of temperature change this effect may not be obvious due to variation of current density seen by different samples located in a different area of the wafer. Figure 3.18 also shows stretchout and deformation of the C-V curve, particularly at higher growth temperatures. There are several techniques to study interface trap behavior that cause stretchout of the high frequency C-V curves. Among them, the conduction method is perhaps the most accurate. However, the high frequency capacitance method is convenient since it does not require low frequency measurements which is very sensitive to noise.

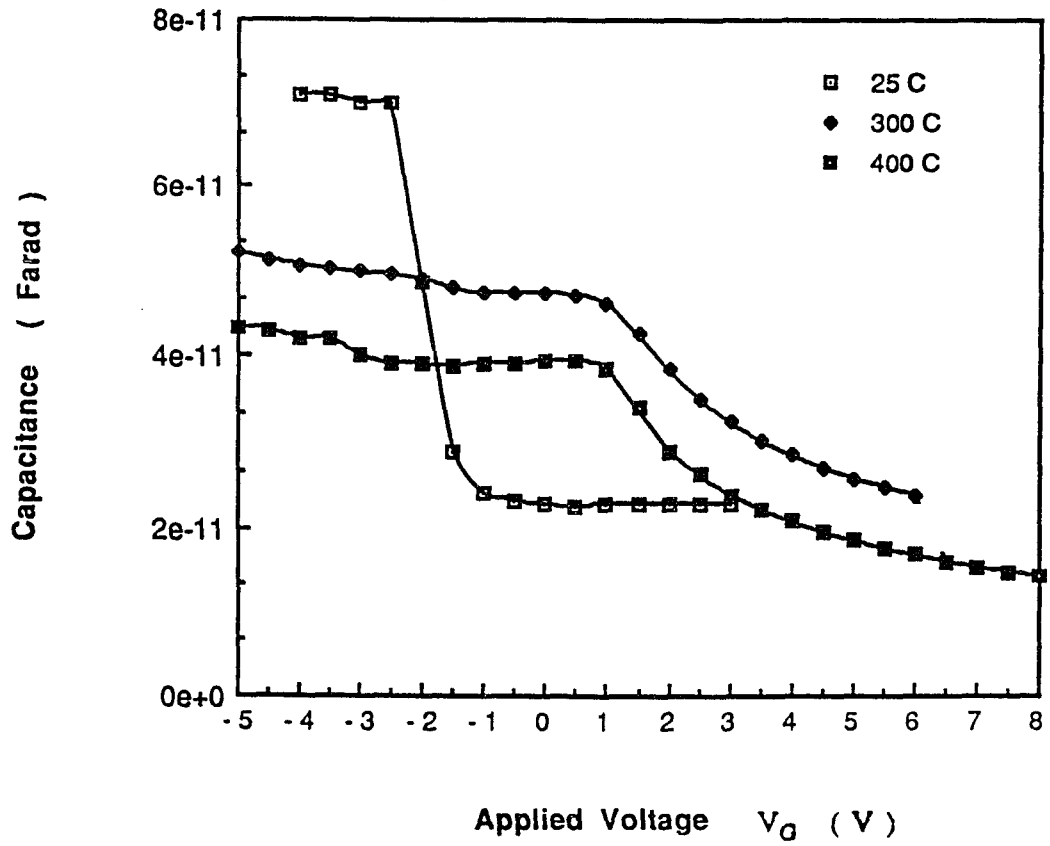

Figure 3.18 C-V characteristics of oxides grown at 25, 300, and 400°C with corona discharge gap of 1 cm and 17 μA current in dry oxygen ambient and at 1 atm pressure.

3.3.4 Study of Interface Trap Properties with Capacitance Technique

Interface traps are defects which are located at the Si-SiO_2 interface. Each interface trap may have one or more energy levels within the silicon bandgap. These defects can interact with silicon bands by emitting and capturing electrons and holes. Interface traps can be acceptor or donor type. The interface trap charge depends on its occupancy. A donor type interface trap is positive when it is empty and neutral when it is filled. An acceptor type interface trap is negative when it is filled and neutral when it is empty. The occupancy of the interface traps changes with the applied dc gate bias voltage. Therefore, the amount of band bending will be influenced by the presence of interface trap charges which is a function of applied gate voltage. The net effect of this is to stretchout the C-V curve. Also, interface traps can respond to the ac measurement signal applied on the gate if the frequency of the ac signal is not too high. If interface traps respond to the ac signal, there will be a contribution of interface traps to the measured value of the capacitance. However, at sufficiently high frequencies, there is no capacitance contribution to C-V curves from interface traps and only the stretchout effect will be present.

Figure 3.19 shows the high frequency C-V curve for a capacitor fabricated with oxide grown at 400 °C for an hour with corona-discharge in comparison with an ideal capacitor having the same oxide thickness, substrate doping and having no interface trap. The valve of the oxide

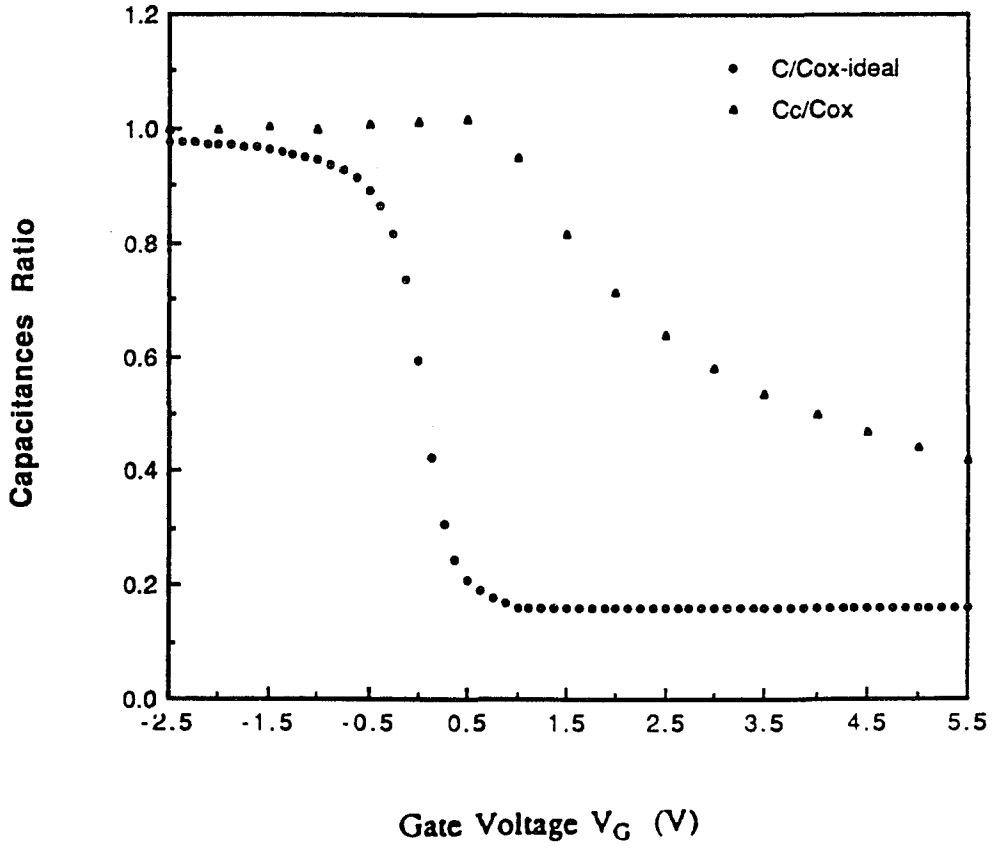

Figure 3.19 C_c/C_{ox} ratio vs gate voltage for a capacitor with oxide grown at 400°C for 1 hour with 1 cm electrode distance in dry oxygen ambient (t_{ox} = 96.2 nm, p-type doping 3.2 x 10^{14} cm^{-3}). The C/C_{ox} curve for an ideal capacitor is also shown for comparison.

thickness t_{ox} was measured to be 96.2 nm for this sample. By " high frequency " it is meant a frequency sufficiently high so that neither minority carriers nor interface traps can follow the ac gate voltage. Minority carrier density do not respond to frequencies higher than 1 kHz at room temperature. Interface traps generally will not respond to frequencies much higher than 100 kHz. The high frequency C-V curve shown on Figure 3.19 is at 1 MHz. At this frequency neither the minority carriers nor the interface traps are expected to respond to the ac high frequency signal. So, there is no capacitance contribution due to interface traps. However, interface traps will respond to the changes in the dc bias voltage. Hence, interface trap occupancy status will be changed, thereby having an effect on the band bending.

A quantitative treatment of C-V stretchout effect is given by Nicollian.[43] From Gauss's law

$$C_{ox}\,(V_G - \psi_s) = -\,Q_{it}(\psi_s) - Q_s(\psi_s) \tag{3.4}$$

where C_{ox} is the oxide capacitance per unit area, V_G is the dc gate bias, ψ_s is the potential drop in Si and is proportional to band bending at the surface, Q_{it} is the interface trap charge per unit area, and Q_s is the charge in silicon per unit area. Differentiating Equation 3.4 with respect to the surface potential ψ_s yields

$$C_{ox}dV_G = [C_{ox} + C_{it}(\psi_s) + C_s(\psi_s)]d\psi_s \tag{3.5}$$

where $C_{it}(\psi_s) \equiv -\frac{dQ_{it}}{d\psi_s}$ is interface trap capacitance per unit area and $C_s(\psi_s) \equiv -\frac{dQ_s}{d\psi_s}$ is silicon depletion capacitance per unit area. Equation 3.5 illustrates the stretchout effect. If $C_{it}(\psi_s)$ is present, a small change in the applied gate voltage dV_G will result in a smaller amount of change in the band bending represented by $d\psi_s$ than when $C_{it}(\psi_s) = 0$. For a change in the applied gate voltage dV_G, there will be a change in the total charge per unit area dQ_T. If the frequency is low enough that the interface traps can maintain equilibrium with the ac signal, the total low frequency capacitance will be given by

$$C_{LF} = \frac{dQ_T}{dV_G} = \frac{(C_{it} + C_s(\psi_s))C_{ox}}{C_{ox} + C_{it}(\psi_s) + C_s(\psi_s)} \tag{3.6}$$

where $Q_T = -(Q_{it} + Q_s)$.

As the frequency of measurement signal increases, the interface trap will not respond to the higher signal frequencies and C_{it} will approach zero. The high frequency MOS capacitance will, hence, be

$$C_{HF}(\psi_s) = \frac{C_s(\psi_s)C_{ox}}{C_{ox} + C_s(\psi_s)}. \tag{3.7}$$

From the above equation it is obvious that for a given ψ_s, the high frequency capacitance and the ideal capacitance with no interface trap will be the same. However, the gate voltages corresponding to ψ_s will be

different for each case. Therefore, ψ_s versus V_G curve can be constructed from the C_{HF}/C_{ox} versus ψ_s curve of ideal capacitor without interface traps and C_{HF}/C_{ox} versus V_G of the capacitor with interface traps. These curves are shown in Figures 3.20, 3.21, and 3.22 respectively. Since any smooth continuous function can be represented by a polynomial expression, the ψ_s versus V_G behavior obtained here is curve fitted with a fifth order polynomial as shown in Figure 3.22. This polynomial is differentiated with respect to V_G. The interface trap capacitance $C_{it}(\psi_s)$ versus total band bending at the surface ψ_s curve is obtained by using equation 3.5 which can be written as follows:

$$C_{it}(\psi_s) = C_{ox}[(d\psi_s/dV_G)^{-1} - 1] - C_s(\psi_s). \tag{3.8}$$

The relation between interface trap density spectrum D_{it} and interface capacitance is given by

$$C_{it}(\psi_s) = qD_{it}(\phi_s) \tag{3.9}$$

where $\phi_s = (\phi_B + \psi_s)$ and $\phi_B = (kT/q)\ln Na/n_i$ is the bulk potential.[43] Here n_i is the intrinsic concentration, Na is the acceptor concentration in p-type silicon, k is the Boltzmann constant, T is the temperature in degree Kelvin and q is the magnitude of electron charge. Figure 3.23 shows the interface trap density spectrum versus surface potential for the capacitor fabricated with oxide grown at 400 °C in dry oxygen ambient with 1 cm electrode distance. The measured interface trap density spectrum values lie in the

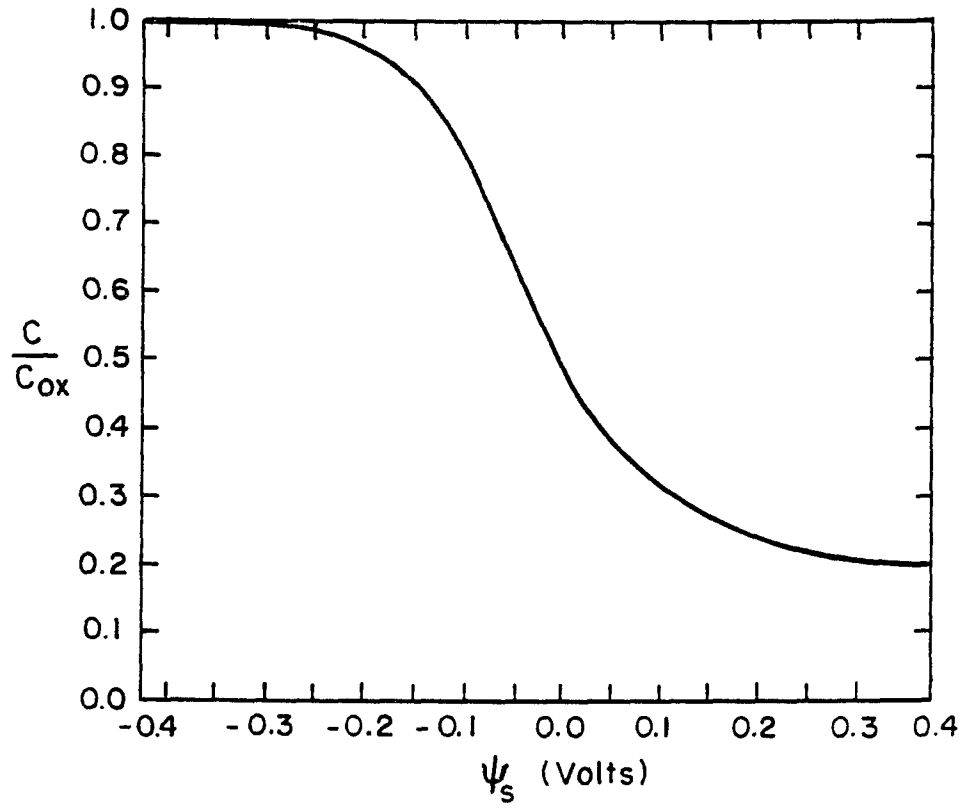

Figure 3.20 C/C_{ox} versus barrier height for an ideal capacitor with t_{ox} = 69.2 nm and p-type doping of 3.2×10^{14} cm^{-3}.

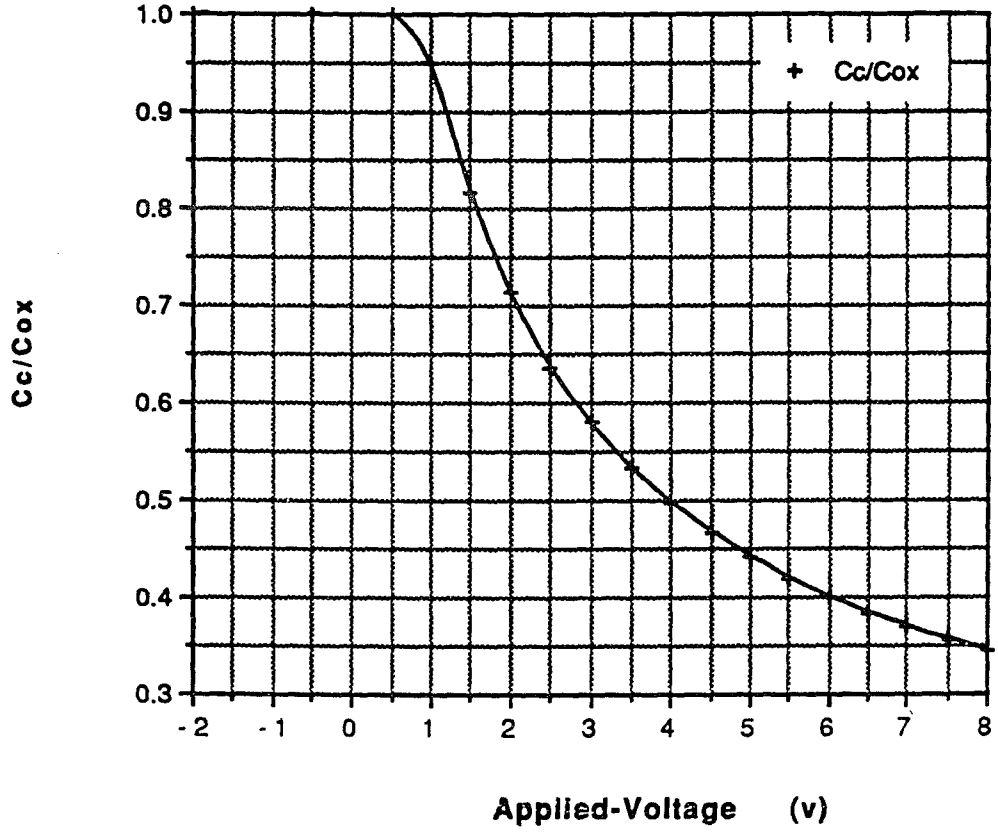

Figure 3.21 Corrected capacitance over oxide capacitance ratio versus gate voltage for a capacitor with oxide grown at 400°C for 1 hour in corona discharge with t_{ox} = 96.2 nm and p-type doping 3.2 x $10^{14.}$ cm^{-3}.

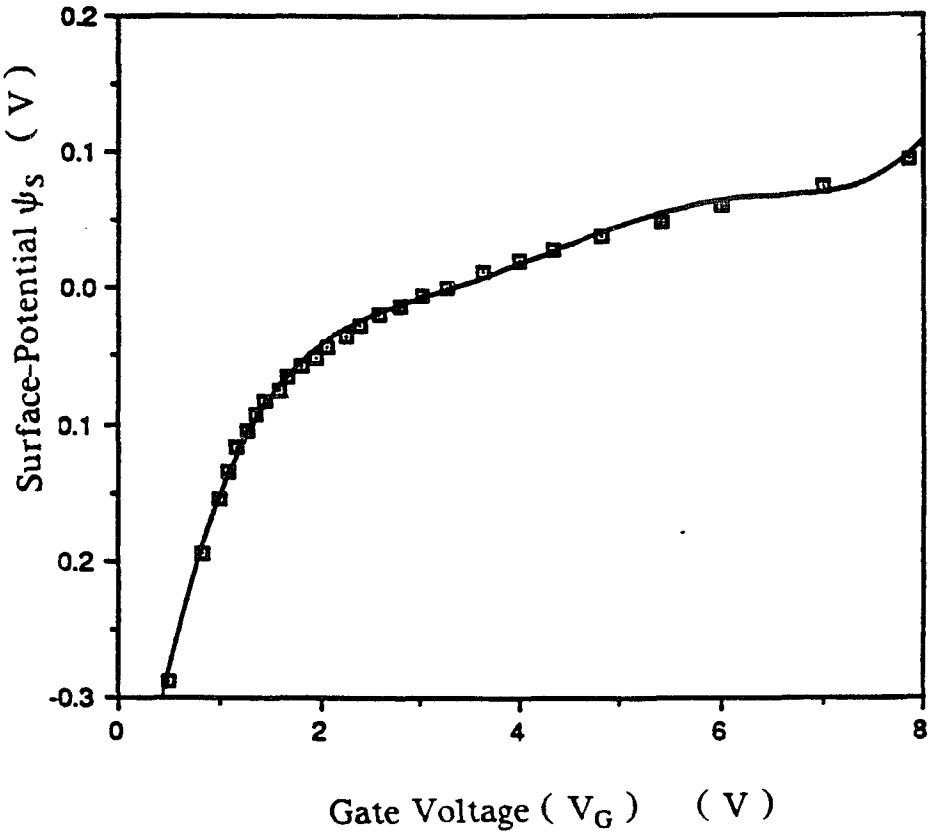

Figure 3.22 Surface potential versus gate voltage curve obtained from the curves shown on Figure 3.20 and 3.21. The data points are curve-fitted by a 5th order polynomial.

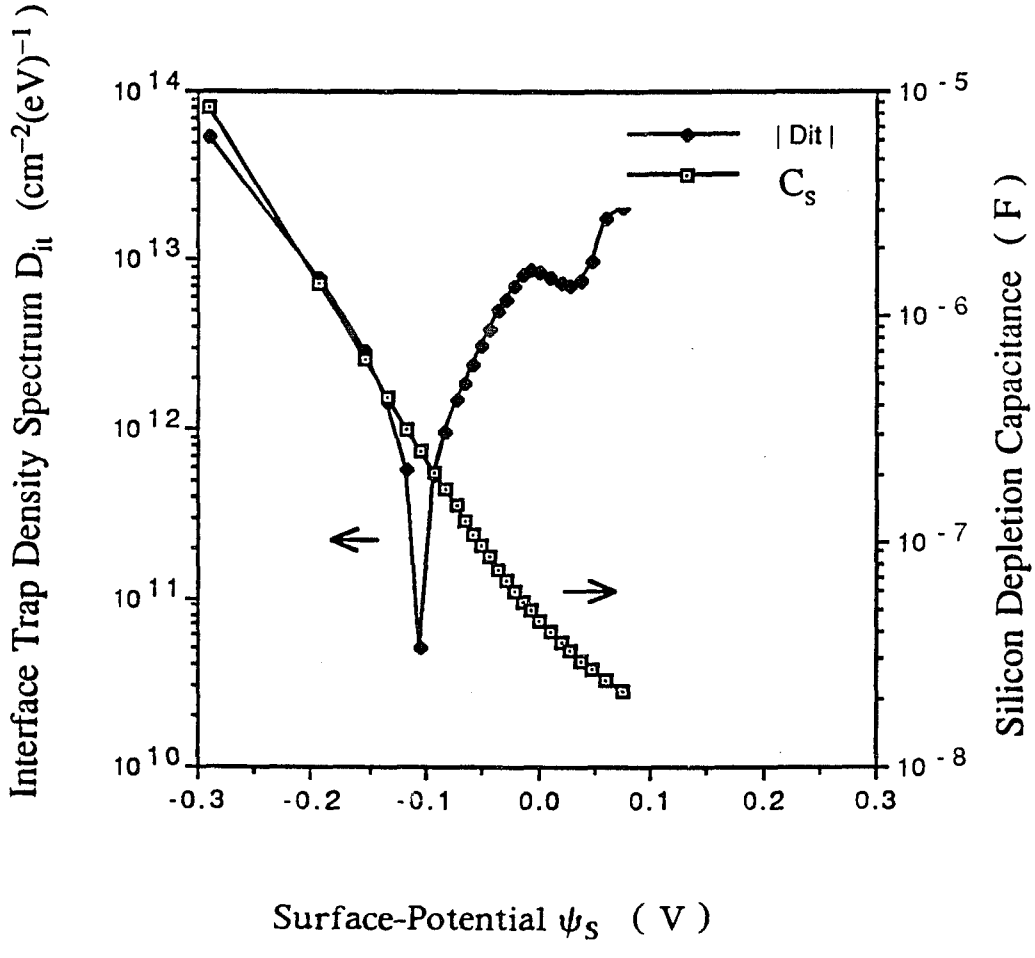

Figure 3.23 Interface trap density spectrum and silicon capacitance versus surface potential ψ_s for the capacitor with oxide grown at 400°C for 1 hour with 1 cm electrode distance.

range of $5x10^{10}$ to $5x10^{13}$ $cm^{-2}(eV)^{-1}$. The interface trap density N_{ss} is calculated. The obtained value of N_{ss} equal to $3.34x10^{13}$ cm^{-2} is higher than the values reported for the oxides grown by high temperature conventional thermal oxidation. At each gate bias the position of Fermi level with respect to the majority carrier band edge at the silicon surface can be determined. For the p-type substrate and non-degenerate material the acceptors introduce an energy level 0.05 (eV) above the top of the valence band. The intrinsic energy level is parallel to valence band everywhere. The intrinsic energy level is approximately $E_g/2$ above the top of the valence band edge where E_g is the semiconductor band gap. At the silicon surface, the intrinsic level bends by the value $q\psi_s$. In the bulk, the Fermi level lies below the intrinsic level by $q\ \phi_B$. At room temperature, ϕ_B = 0.259 V is calculated from doping concentration. Therefore, the location of interface trap energy level E_T located at the Fermi level ($E_F = E_T$) can be determined for each value of ψ_s from the following equation:

$$\frac{E_T - E_V}{q} = \frac{E_g}{2q} + \psi_s - \phi_B. \qquad (3.10)$$

The variation of ψ_s versus the gate voltage is shown in Figure 3.22. The interface trap density spectrum versus the trap level location from the top of the valence band at the silicon surface for capacitor with oxide grown with corona discharge at 400°C for an hour with electrode distance at 1 cm is shown in Figure 3.24.

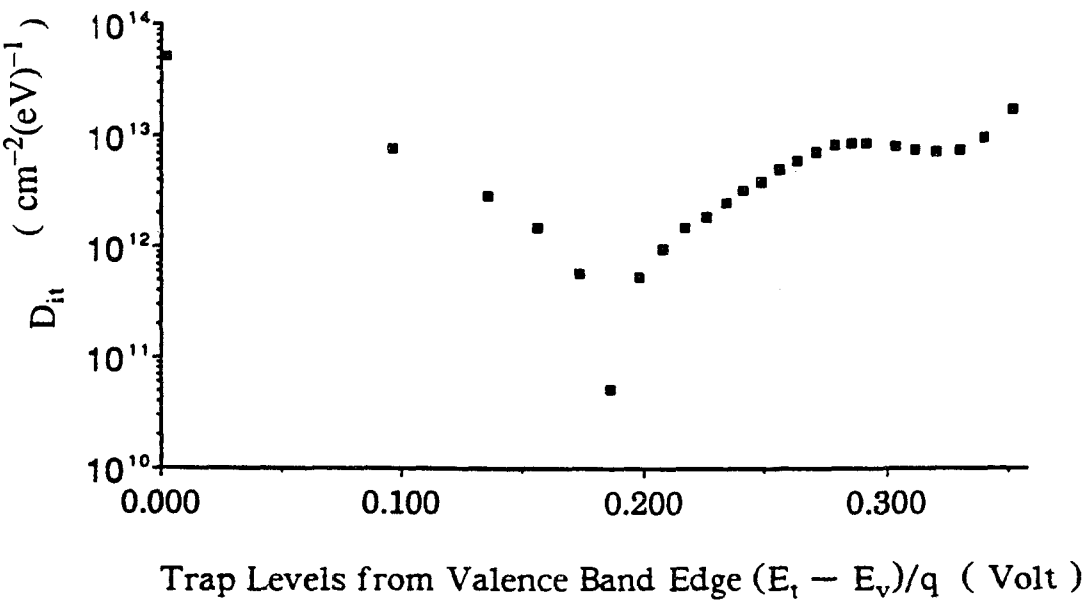

Figure 3.24 Interface trap density spectrum versus the trap level location from the majority carrier band edge (E_v) at the silicon surface for capacitor with oxide grown at 400°C for 1 hour with 1 cm electrode distance.

In summary, the oxidation rate of silicon using point-to-plane corona discharge in dry oxygen ambient at temperatures between 25°C to 500°C has been investigated. The rate of oxidation increases significantly in comparison with the rate of conventional thermal oxidation of silicon. As the thickness of the film increases, the refractive index of the oxide grown by this technique approaches the value obtained for high temperature thermally grown oxides. Uniformity of the grown oxide layer of ±20% across a 2.5 cm diameter wafer has been obtained. Capacitor structures were fabricated by evaporating aluminum dots on the grown oxides and the electrical quality of the oxides were investigated. When the aluminum gate was biased negatively with respect to the substrate, the measured dc current was higher than the measured current value under positive bias. The C-V characteristic curve for the MOS capacitors fabricated showed a shift in the flat-band voltage. A negative flat-band shift of 1.5 V was obtained for oxides grown at room temperature with 17 μA corona discharge current. As the corona current density during the oxidation is decreased, both leakage current and the shift in the flat-band voltage decreases for the samples grown at room temperature. A study of dc leakage current indicated Frenkel-Poole emission as the likely mechanism for positive voltages applied to the gate while tunneling was observed to be the likely mechanism for negative voltages applied to the gate. The interface trap density spectrum in the range of $5x10^{10}$ to $5x10^{13}$ $cm^{-2}(eV)^{-1}$

was obtained for a sample with oxide grown at 400°C for 1 hour with 1 cm electrodes distance and 17 μA corona current. The interface trap density N_{ss} was calculated to be $3.3x10^{13}$ cm^{-2}. The obtained interface trap density value is higher than the interface trap density of the oxides grown by conventional thermal oxidation. The values of the leakage current, shift in flat-band voltage, and interface trap density seemed to be a function of the process parameters such as electrodes distance, temperature, and current density. The overall electrical quality of the oxide grown by this method at low temperature suggests that the oxide grown by this technique may have a good potential for selective implementation in VLSI fabrication technology.

CHAPTER 4

OXIDATION MECHANISM

4.1 Introduction

Oxidation of silicon is one of the important steps in the fabrication of VLSI circuits. As the MOSFET design rules approach towards 0.5 μm line width, the gate insulator thickness will scale down to about 10 nm. The well known Deal-Grove model[47] used for modeling of thermally grown oxides for nearly two decades is not suitable for today's 30 nm thermal oxidation technology. The Deal-Grove model is based on the diffusion of oxidant species at high temperatures (700° - 1200°C) as a rate-limiting step and is accurate for oxidation temperature in this range and for thick oxide layers (30-2000 nm). It is valid for oxidation pressures from 0.1-1.0 atm in both wet and dry ambients. At lower oxidation temperatures and/or thin oxide growth regimes where other mechanisms can be the rate-limiting step, this model ceases to be useful. Some researchers have tried to modify this model so that it will be suitable for thin oxide layers.[48,49] Some others have tried to develop new models based on viscous flow concepts.[50–53]

Recently, Nicollian and Reisman[53] have developed a new model which is based on a viscous flow principle. In contrast with Deal-Grove

model, there is no "anomalous" oxidation region at small thicknesses in the early stage of oxidation. It is derived on physical fundamentals which can give better understanding of the oxidation mechanism during the initial oxidation phase. This chapter gives some physical explanation of the parameters involved in this model as they relate to the negative point to plane corona discharge oxidation. The parameter values are compared with those obtained for thermal oxidation of silicon. In Section 4.2, a brief review of Deal-Grove model is given. In Section 4.3, oxidation species are considered. In Section 4.4, a brief review of Nicollian-Reisman thermal oxidation model is given. The data on corona discharge oxidation of silicon at low temperatures and at high temperatures are curve fitted and the corresponding value for each parameter is given in Section 4.5. Finally, an explanation is suggested for the enhancement observed during the oxidation of silicon using point to plane corona discharge in dry ambient.

4.2 The Deal-Grove Model

The Deal-Grove model on the thermal oxidation of silicon was presented in 1965.[47] It was determined experimentally that oxidation species move inward rather than silicon move outward from the substrate to form the oxide. After the transport of oxidant species through the oxide, silicon reacts with the oxidant species. During thermal oxidation of

silicon wafers, there are four important regions to consider. These are the gas stream in the oxidation furnace, the gas stagnant layer, the oxide layer growing on the silicon surface, and the silicon wafer. These regions are shown in Figure 4.1. As the diffusing oxidant species react with the silicon atoms, the boundary between the oxide and silicon will change in time. This time varying boundary is assumed to be quasi-static.[54–55] There are three fluxes F_1,F_2 and F_3 involved which must be equal during the steady state oxidation. The quadratic equation for film thickness x_o in this case can be obtained as[54]

$$x_o^2 + Ax_o = B(t + \tau) \tag{4.1}$$

where t is oxidation time, τ is related to the initial oxide thickness x_i, present before oxidation. Here parameters A, B and τ are given as:

$$A \equiv 2D_{eff}(1/k_s + 1/h) \tag{4.2a}$$

$$B \equiv 2D_{eff}C^*/N_1 \tag{4.2b}$$

$$\tau \equiv \frac{x_i^2 + Ax_{i.}}{B} \tag{4.2c}$$

where D_{eff} is the effective diffusion coefficient, k_s is the chemical surface-reaction rate constant, h is the gas-phase mass-transfer coefficient, C^* is the is the concentration of the oxidant in the oxide in equilibrium with the bulk of the gas, and N_1 is the is the number of oxidant molecules incorporated into a unit volume of oxide. For relatively long oxidation time $t \gg \frac{A^2}{4B}$ and $t \gg \tau$, $x_o^2 \cong Bt$ and the oxidation rate shows a parabolic

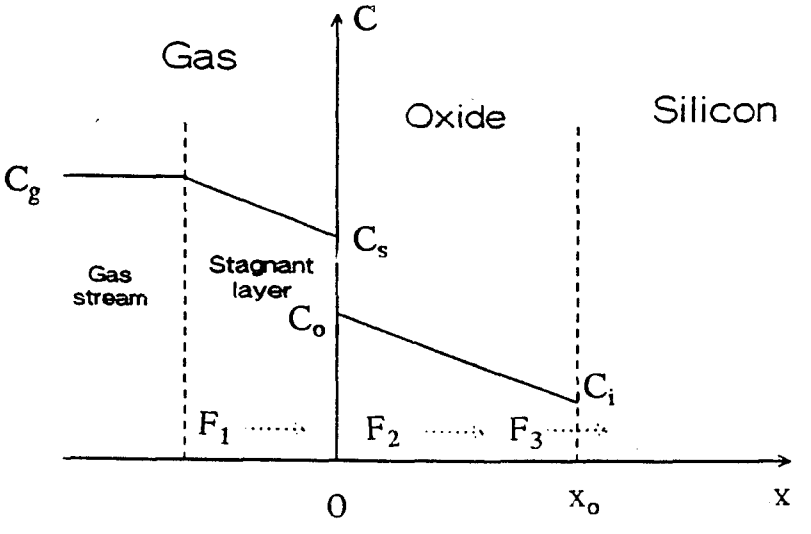

Figure 4.1 Deal and Grove model for the thermal oxidation of silicon.[54]

behavior and hence B is called the parabolic rate constant. In this regime, the oxidation is a diffusion controlled process. For relatively short time of oxidation $t \ll \frac{A^2}{4B}$, $x_o \cong \frac{B(t+\tau)}{A}$ and the film thickness increases linearly with $\frac{B}{A}$ referred to as the linear rate constant. The oxidation in this regime is a reaction controlled process. For dry-oxygen oxidation in the 700° to 1200°C range, for the oxide thickness data extrapolated to zero time the curve intersects the oxide thickness axis at about x_i = 25 nm. Hence, Deal and Grove indicated that a different mechanism of oxidation is present for oxide thicknesses less than 30 nm, as it could not be explained by the model.

Over the past several years, the use of *in situ* ellipsometer has revealed other details of oxidation mechanism related to the Deal-Grove model. Considering the changes in both the parabolic rate constant B and the linear rate constant $\frac{B}{A}$ with temperature, Lewis and Irene reasoned that since both these constants exhibit breaks in their linear Arrhenius plots in the temperature range 900 ° - 1000 °C, this change of the slope (i.e. activation energy) reflects a change in the oxidation mechanism at low temperatures.[56] Also, it has been reported that relaxation of low temperature oxidation stress through viscous flow occurs around 950°C[57].

4.3 Oxidant Species in Silicon Thermal Oxidation

Transport of oxidant species depends on the range of oxidation temperatures[51] and thickness regimes. At high temperatures (> 950°C), Fickian diffusion of oxidant species through the oxide dominates. The well known classical Deal-Grove model[47] is in support of this mechanism. At low oxidation temperatures, Fickian diffusion is slow and interstitial transport of oxidant species occurs through micro-pores. The studies of the thermal oxidation of silicon by oxygen isotope 18 suggested[58,59] that most of the oxide grows by long range migration of oxygen through the oxide, favoring models based on the transport of molecular oxygen for thick oxide regime and growth temperatures above 930 °C. *In situ* study of oxidation of silicon up to 20 nm thickness at temperatures 980 °C and lower, indicates linear oxidation kinetics which is typical of surface controlled reactions.[51] Direct evidence for 1 nm pores in dry thermal SiO_2 has been reported.[60] It is thought that the micro-pores would provide a "short circuit" path to the $Si - SiO_2$ surface and hence, oxidation will be surface reaction controlled. Irene[51] has indicated that the reason for not observing micro-pore effect in the oxidant transport at high temperature may be due to thermal agitation of these 1 nm diameter pores or due to an increase in the solubility of O_2 in SiO_2 at higher temperatures thereby spending little time in the micro-pores before dissolving in SiO_2.

The involvement of charged particles in the oxidation of silicon was reported by Jorgensen[61] in 1962. The validity of the Jorgensen's result has been questioned by Raleigh.[62] A thermodynamic argument presented by Modlin and Tiller[30] indicates that it is energetically unfavorable to form interstitial O^- and/or O_2^- species by the transport of electrons and holes across the SiO_2 layer to SiO_2/gas interface. Hence, for the oxide thicker than 30 nm it is concluded that the dominant oxidant species during thermal oxidation is neutral oxygen molecules.

4.4 Nicollian-Reisman Model for the Thermal Oxidation of Silicon

Recently, a new model for thermal oxidation of silicon has been proposed by Nicollian and Reisman.[53] The "dry" silicon oxidation data obtained from 1965 onwards for 800°C to 1000°C oxidation temperature and from $1x10^{-5}$ atm to 20 atm oxygen partial pressure have been modeled with good accuracy by this model.[63] The model describes behavior in the thin oxide growth regime and hence, includes the "anomalous" oxidation region at small thicknesses not explained by the previous model. If the partial pressure of oxygen at the Si–SiO_2 interface is time independent and equal to the input partial pressure, the oxidation is surface reaction rate controlled. For the temperatures and pressures of interest in integrated circuit technology, the oxide thickness versus time is given by

$$x = k_f\, p^n\, t \tag{4.3}$$

where k_f, p, n and t indicate the forward specific reaction rate, partial pressure of oxygen, the order of the forward reaction and the oxidation time respectively. If the partial pressure of oxygen at the Si–SiO_2 interface is less than the input partial pressure and/or varies with time, oxidation is mass transport limited and the oxide thickness versus time is given by

$$x = D^{1/2}\, t^{1/2} \tag{4.4}$$

where D is the diffusion coefficient. Equation (4.3) or (4.4) can be considered as special cases of general power law of the form

$$x = a\, t^b \tag{4.5}$$

where b=1 for surface reaction rate controlled oxidation and b = 0.5 for mass transport controlled oxidation. Nicollian-Reisman reason that since coefficient b varies between 0.24 to 0.9 for all cases considered[53], the upper limit of b is unity and since b is neither 0.5 nor 1 means that either k_f or D must decrease with time according to a power law. They postulate that the thermal oxidation is reaction rate controlled with the rate limiting mechanism being the viscous flow of the oxide as explained below. This also implies that oxidant transport through the oxide must be rapid. At low temperatures and under dry oxygen ambient case, the existence of micropores in the thermal oxide will facilitate the transport of oxidant to the SiO_2 interface[60]. Upon the arrival of oxidant molecules at the Si–SiO_2

interface, the following events of oxidant molecule dissociation, breaking of bonds and the formation of SiO_2 molecules lead to the free volume expansion. Unless, free volume expansion occurs to accommodate the new forming oxide which occupies about 2.2 times the volume of silicon from which it is formed, oxidation can not proceed. Therefore, specific reaction rate coefficient is dependent on the creation of free volume . This free volume expansion is provided by viscous flow of oxide.[64] If the free volume is created slowly in comparison with the process of reaction, viscous flow will be rate limiting and b in equation (4.5) will be less than unity. Otherwise, reaction itself is rate limiting and b will be equal to unity. Based on viscous flow mechanism in oxidation of silicon, Nicollian and Reisman have derived the expression for parameters a and b of equation (4.5) as given below:[53]

$$a = k_A\, p^n \exp\left(- \frac{\Delta E_F}{kT}\right) \eta_o G\, b(p,T)^{-1} \qquad (4.6a)$$

and

$$b(p,T) = 1 - \phi(p,T) \qquad (4.6b)$$

where k_A is the forward specific reaction rate coefficient, p is the instantaneous pressure of oxygen, n is the order of forward reaction, η_o is the average oxide viscosity value extrapolated to an infinite temperature, T is the absolute temperature, k is the Boltzmann's constant, ΔE_F is part of the energy required for the reaction to occur which includes the activation

energy to break the Si-Si bonds which is different from the energy required to produce the free volume by viscous flow to accommodate the volume expansion, $\phi(p,T)$ determines the shape of viscosity η vs t, G is constant independent of pressure and temperature. The parameter $\phi(p,T)$ determines how fast the average viscosity increases at times t greater than t_i in the relation $\eta(t,p,T) = G(t - t_i)^{\phi(p,T)}$ where t_i is the time it takes to form the original ordered structure.

4.5 Application of Nicollian-Reisman Model to Point-to-Plane Corona Oxidation

The rate of oxidation of silicon enhances significantly with negative point to plane corona discharge in dry oxygen ambient at both high temperatures in 600 °-1000°C regime[30] and at low temperatures in 25°-500°C range as observed in this work. The grown oxide thickness as a function of oxidation time is proportional to the negative ion current density during oxidation. The refractive index of the grown oxide with this method at low temperature approaches the refractive index of the thermal oxide grown at 1200 °C as the time of oxidation increases. The corona discharge at 800 °C has been reported to fully relax the stress present in a thermally grown oxide on Si at 800°C.[65] The corona-relaxed oxides are shown to be equivalent to ~ 1200°C thermally grown or thermally relaxed oxides, both with respect to their refractive index values and the value for

diffusion coefficient of oxygen through them. There have been numerous studies about the stresses which arise at low temperature of oxidation of silicon.[66] These stresses are due to the difference in thermal expansion coefficients between Si and SiO_2 at the oxidation temperature, typically about 950°C and lower. The volume expansion associated with SiO_2 molecules formed from silicon atoms during thermal oxidation is facilitated by viscous flow.[64] This flow is derived from a compressive plane stress present in the grown oxide when oxygen is moved into the silicon lattice of the SiO_2/silicon interface. Several new models based on relaxation of viscous flow have been developed.[50–53] Nicollian-Reisman model is the most complete among them to-date and can fit thermal oxidation data gathered during the past 20 years for different oxidation pressures and temperatures.

In this work, the available data for corona-discharge oxidation at temperatures in the range of 700 °C and 900 °C[30], and data for corona-discharge at low temperatures obtained in this present work here are curve-fitted with the power-law model developed by Nicollian-Reisman[53] based on viscous flow. In the computational procedure, Gauss-Newton iterative technique is used. The a and b parameter values obtained after curve-fitting are listed in Table 4.1. The initial oxide thickness x_i is assumed here to be 1.5 nm for some cases considered to obtain a good fit between the data and the theory. It is also the thickness of the oxide

generally present over an otherwise unoxidized Si wafer. The errors listed in Table 4.1 are calculated using the following equation :

$$\text{error} = \frac{1}{N}\sum_{j=1}^{N}\frac{[x_p(j) - x(j)]^2}{x(j)} \tag{4.7}$$

where x_p is the predicted value for the oxide thickness by the model, x is the actual oxide thickness, and N is the number of the data points. A comparison between parameter b obtained for 700 °C and 900 °C corona-discharge oxidation with corresponding thermal oxidation data at the same temperatures[49] shows an increase in the value of parameter b which corresponds to a more relaxed oxide state and a higher rate of viscous flow. For the oxides grown with corona-discharge at a temperature close to the thermal viscous flow temperature of 950 °C, the unity value for the parameter b indicates that the oxide is completely relaxed (i.e. the total activation energy $\Delta E >> \Delta E_v$ the energy required to produce free volume by viscous flow). When ΔE is much greater than ΔE_v, the oxidation process is fully reaction rate controlled since the oxide network is fully relaxed as is the case for thermal oxidation at high temperatures. This result is consistent with Landsberger-Tiller[65] work which indicates that the activation energy for oxygen diffusion through a completely relaxed corona discharge oxidation is 0.8 (eV) which is close to the value observed for thermally grown oxide at temperatures in the range of 1150 °C - 1200 °C. The value of parameter b obtained for the oxide grown at

900 °C with corona-discharge is considerably higher than the value of b for the same temperature for thermal oxidation. Also, oxidation rate at low temperature significantly increases with corona-discharge. Therefore, it is concluded that negative point to plane corona-discharge will relax the SiO_2 stress and let viscous flow to occur at lower temperatures. This also could imply that the dominant factor in the enhancement of oxidation rate of silicon using negative point to plane corona discharge is the increase in the viscous flow or lowering of free volume activation energy and is not directly due to the effect of involvement of ionic oxidant in the transportation process through the oxide. Transportation of oxygen at low temperatures are facilitated through the micro-channels or pores that exist in the SiO_2 structure.[60] The effect of corona-discharge on the kinetics of viscous flow needs more experimental as well as theoretical work.

Table 4.1 Parameters "a" and "b" in Nicollian and Reisman model for conventional thermal and corona discharge oxidation of silicon.

Oxidation Temperature	Oxidation Techniques							
	Thermal				Corona-assisted			
	a	b	x_i	error	a	b	x_i	error
950 °C[49]	18.99	0.702	15.108	-	-	-	-	
900 °C[49,30]	11.88	0.682	15.0	0.037	14.00	1.0	15.0	3.677
800 °C[49]	7.011	0.581	13.938	2.833	-	-	-	-
700 °C[49,30]	4.010	0.502	17.48	0.772	34.99	0.802	14.74	6.413
492 °C	-	-	-	-	14.00	0.700	15.00	0.387
300 °C	-	-	-	-	58.00	0.600	15.00	4.249

CHAPTER 5

SUMMARY, CONCLUSIONS AND RECOMMENDATIONS

In this work, oxides are grown on silicon by negative point to plane corona discharge at low substrate temperature values in the range of 25°C to 500°C. Some of the electrical properties of the oxide films grown by this method are examined. Interface properties of the oxide grown by this technique are also studied for possible utilization of this technique in fabrication of semiconductor devices. Some of the important results obtained in this work are summarized below.

1. The rate of oxidation of silicon using negative point to plane corona discharge is significantly higher than the rate of oxidation of silicon using conventional thermal oxidation techniques. In fact, the oxidation of silicon is possible at temperatures as low as the room temperature to yield significant oxide thickness in a reasonable oxidation time.

2. The refractive index of the grown oxide using point to plane corona discharge approaches the refractive index of the oxide film grown with conventional high temperature oxidation technique as the oxide thickness increases.

3. The uniformity of a grown 12 nm thick oxide film was within 20 percent across a 2.5 cm diameter wafer for a 2 cm electrode spacing. However, the uniformity of the grown oxide is a function of the distance between the two electrodes, the shape of the top electrode needle and possibly certain other process parameters.

4. The resistivity of the starting material has no significant effects on the oxidation rate.

5. The dc I-V characteristic curves for the MOS capacitors with the oxide grown by this method shows higher conduction current when the aluminum gate of the capacitor is biased negatively with respect to the substrate than the measured current value under positive bias.

6. The C-V characteristic curves for the MOS capacitors fabricated with oxide grown by this method shows a shift in the flat-band voltage towards negative direction on the dc bias voltage axis which indicates the presence of a net effective positive charge density in the oxide near the oxide-semiconductor interface.

7. Bias stress test results indicate a presence of mobile charges in some of the samples grown at room temperature, along with some

charge injection instability on other room temperature grown samples.

8. The logarithm of the current density versus the square root of the positive voltage appearing across the oxide fabricated from oxides grown at room temperatures indicates that the major component of charge transport through the oxide shows behavior similar to the Frenkel-Poole emission mechanism. For negative voltage appearing across this oxide, the tunneling process is observed to be the dominant charge transport mechanism.

9. As the current density of the corona discharge during the oxidation process decreases, the leakage current through the MOS capacitor fabricated with that oxide also decreases. Also, the flat-band voltage shift of the C-V characteristics curve of the fabricated MOS capacitor decreases as well.

10. Interface trap density spectrum in the range of $5x10^{10}$ to $5x10^{13}$ $(eV)^{-1}$ cm^{-2} is obtained from the high frequency C-V curves for the oxide grown at 400°C temperature and 17μA corona current with 1 cm distance between the electrodes. The interface trap density of $3.34x10^{13}$ cm^{-2} was calculated. The interface trap density for this sample is higher than the interface density of the oxides

grown by high temperature conventional thermal oxidation. However, lower interface trap density may be obtained by changing some of the process parameters during oxidation.

11. The available data for corona-discharge oxidation at temperatures of 700°C and 900°C[30] and the data for corona-discharge oxidation at low temperature obtained from this work are curve fitted with the power-low model developed by Nicollian–Reisman[53] based on viscous flow. From the obtained parameters, it can be concluded that the negative point to plane corona discharge will relax the SiO_2 stress and let viscous flow occur at lower oxide growth temperatures.

Some of the recommendations for future work are as follows:

1. The process of oxidation of silicon using negative point to plane corona discharge involves many parameters such as temperature, pressure, current density, needle shape, and the distance between the electrodes. The optimum values for these parameters are desired to yield the best quality oxide. Specifically, more work needs to be carried out to study the effect of needle shape, electrode distance, oxidation temperature, and chamber wall geometry on the corona discharge current density.

2. The effects of platinum needle and platinum foil as substrate holder on the quality of the oxide grown by this method at different temperatures needs to be studied. This work requires a clean room environment.

3. The effect of corona current density on the uniformity of the grown oxide films needs to be examined carefully.

4. Investigation of multiple needle electrodes to plane corona discharge oxidation on the uniformity of the grown oxide film also needs to be studied.

5. Use of *in situ* ellipsometer is needed to study the details of oxidation mechanism of silicon using point to plane corona discharge for various growth temperature.

6. The effect of corona discharge on viscous flow of SiO_2 needs to be studied.

7. The effect of the negative point-to-plane corona discharge on the silicon substrate needs to be examined.

8. The selective oxidation of silicon wafer at low temperature using a

pattern overlayer is of some interest and needs to be investigated. Also, 3-dimensional study of the grown oxide is needed.

9. The effects of annealing on the quality of the grown oxide needs to be examined.

10. Study of MOS transistor fabricated from the oxide grown by corona discharge oxidation technique is needed.

11. Oxidation of GaAs wafers by this method is of interest.

12. All of the above recommendations for positive point to plane corona discharge also needs to be investigated.

13. The study of corona discharge on chemical vapor deposition of dielectric materials may also be of interest.

In conclusion, a low temperature oxidation technique for silicon using point- to-plane corona discharge is developed. The oxidation rate of silicon by using this technique is significantly higher than the conventional thermal oxidation rate of silicon. As the thickness of the SiO_2 films grown at temperatures between 25°C to 500°C by this method increases, the refractive index of the films approach the refractive index of the SiO_2

films grown by conventional thermal oxidation at high temperatures. The quality of the oxide grown by this technique is examined. The C-V characteristic curves of the MOS capacitors fabricated with the oxide grown at low temperatures using negative point-to-plane corona discharge indicate a shift in the flat-band voltage in comparison with the C-V characteristics of the ideal capacitors. The amount of the shift in flat-band voltage is observed to be a function of the oxidation temperature and the corona current density during the oxidation process. The mechanism of the current leakage of the grown films at room temperature is examined. The leakage current of the capacitors fabricated with the oxide grown by this method are not symmetrical for dc negative and positive gate bias voltages. The interface properties of the grown oxides are studied. Interface trap density spectrum in the range of $5x10^{10}$ to $5x10^{13}$ cm^{-2} $(eV)^{-1}$ is obtained for the oxide grown at 400°C for one hour with 1 cm electrode distance at 1 atm pressure in dry oxygen ambient. An interface trap density value of $3.3x10^{13}$ cm^{-2} $(eV)^{-1}$ is calculated. The interface trap density may be lowered by changing some of the process parameters such as electrode gap, ion current, needle shape and temperature. Also, annealing may reduce the interface trap density to the device quality level. The overall electrical quality of the oxide grown by this method suggests that the SiO_2 film grown by this method has a potential for selective implementation in MOS device technology. The mechanism of the oxidation of silicon using

negative point-to-plane corona discharge is studied. The corona discharge during oxidation of silicon in a dry ambient seems to increase the rate of viscous flow which corresponds to a more relaxed oxide state and a higher rate of oxidation.

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APPENDIX 1

The ideal C-V characteristic curves for the MOS capacitors with a given oxide thickness, gate area, substrate bulk resistivity, and temperature are numerically obtained by using a computer program, which is written for this purpose. For each value of the DC bias voltage V, the surface potential ψ_s is calculated using equation

$$V - V_{FB} = V_i + \psi_s \tag{A.1}$$

where ψ_s is surface potential and V_i is the potential across the oxide due to charges Q_s in the semiconductor. For ideal MOS capacitor, the flat-band voltage $V_{FB} = 0$. Hence, the applied voltage appears partly across the oxide and partly across the semiconductor. The voltage V_i is given by

$$V_i = \frac{-Q_s d}{\varepsilon_i} \tag{A.2}$$

where ε_i is insulator permittivity, and d is the insulator thickness. In equation A.2, Q_s is the total charges per unit area in the semiconductor and is given by

$$Q_s = \pm \sqrt{2}\frac{kT}{qL_D} F(\beta\psi_s, \frac{n_{po}}{p_{po}}) \tag{A.3}$$

where

$$F(\beta\psi, \frac{n_{po}}{p_{po}}) \equiv [(e^{-\beta\psi} + \beta\psi - 1) + \frac{n_{po}}{p_{po}}(e^{+\beta\psi} - \beta\psi - 1)]^{1/2} \tag{A.4}$$

$\beta \equiv q/kT$, q is the electron charge k is Boltzmann Constant, T is the tem-

perature, the potential ψ is defined as zero in the bulk of the semiconductor and measured with respect to the intrinsic Fermi level, n_{po}/ p_{po} is the ratio of electron concentration with respect to hole concentration in a p-type semiconductor in equilibrium, and L_D is the extrinsic Debye length for holes in the p-type material and is given by

$$L_D \equiv \sqrt{\frac{\varepsilon_s}{qp_{po}\beta}} \tag{A.5}$$

where ε_s is the semiconductor permittivity. For each value of the applied voltage V, the value for ψ_s in equation A.1 is calculated. The value for depletion capacitance C_D is obtained by using the calculated value for the surface potential ψ_s and is given as[43]

$$C_D = \frac{\varepsilon_s}{\sqrt{2}L_D} \frac{[1 - e^{\beta\psi_s} + (n_{po}/p_{po})(e^{\beta\psi_s} - 1)]}{F(\beta\psi_s, n_{po}/p_{po})} \tag{A.6}$$

The total capacitance C_c is a series combination of the oxide capacitance $C_i = \varepsilon_i/d$ and the depletion capacitance C_D.

VITA

Mr. Madani received his Bachelor of Science degree in Electrical Engineering from Texas Tech University in December 1976. He obtained his M.S. degree from Southern Methodist University in Dallas while he was employed at Mostek Corporation. During his employment in Mostek, he worked on various projects as a test and characterization engineer and as a research and development process engineer. He is currently a doctoral candidate in the Electrical and Computer Engineering Department at Louisiana State University and works as an Assistant Professor in the Electrical and Computer Engineering Department at The University of Southwestern Louisiana in Lafayette.

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