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MODELING OF THERMALLY AWARE CARBON NANOTUBE AND GRAPHENE BASED POST CMOS VLSI INTERCONNECT

A Dissertation

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

in

The Division of Electrical and Computer Engineering

by
K M Mohsin
M.S., Louisiana State University, Baton Rouge, 2017
B.S., Bangladesh University of Engineering and Technology, Bangladesh, 2011
December 2017

To my parents, for all their life long sacrifices to prepare me for this long journey…

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ABSTRACT

This work studies various emerging reduced dimensional materials for very large-scale integration (VLSI) interconnects. The prime motivation of this work is to find an alternative to the existing Cu-based interconnect for post-CMOS technology nodes with an emphasis on thermal stability. Starting from the material modeling, this work includes material characterization, exploration of electronic properties, vibrational properties and to analyze performance as a VLSI interconnect. Using state of the art density functional theories (DFT) one-dimensional and two-dimensional materials were designed for exploring their electronic structures, transport properties and their circuit behaviors. Primarily carbon nanotube (CNT), graphene and graphene/copper based interconnects were studied in this work.

Being reduced dimensional materials, the charge carriers in CNT(1-D) and in graphene (2-D) are quantum mechanically confined. As a result of this, free electron approximation fails to explain their electronic properties. For same reason, Drude theory of metals fails to explain electronic transport phenomena. In this work Landauer transport theories using non-equilibrium Green function (NEGF) formalism was used for carrier transport calculation. For phonon transport studies, phenomenological Fourier's heat diffusion equation was used for longer interconnects. Semi-classical BTE and Landauer transport for phonons were used in cases of ballistic phonon transport regime. After obtaining self-consistent electronic and thermal transport coefficients, an equivalent circuit model is proposed to analyze interconnects' electrical performances.

For material studies, CNTs of different variants were analyzed and compared with existing copper based interconnects and were found to be auspicious contenders with integrational challenges. Although, Cu based interconnect is still outperforming other emerging materials in terms of the energy-delay product (1.72 fJ-ps), considering the electromigration resistance graphene Cu hybrid interconnect proposed in this dissertation performs better. Ten times more

electromigration resistance is achievable with the cost of only 30% increase in energy-delay product. This unique property of this proposed interconnect also outperforms other studied alternative materials such as multiwalled CNT, single walled CNT and their bundles.

CHAPTER 1
INTRODUCTION

The metal oxide semiconductor field effect transistor (MOSFET) has been the workhorse for semiconductor industries for more than half a century. Interconnect is the highway for electrical signal to travel through the (computer) chip and is commonly known as integrated circuit (IC). Interconnect is referred as a pathway for electrical charge carriers (electrons) to travel through based on the potential differences of the source and destination nodes. In most cases materials with metallic behavior or highly doped silicon (degenerate, poly-Si) could be used as interconnect. Any materials that show no band gap in its electronic band structure is metallic in nature and can be potentially used as interconnect. Besides zero band gap, it is preferred having high density of states near Fermi energy to be a very good conducting interconnect material.

If a transistor is the information processing unit, one can think of interconnect as a connector of all those information processing units. Beside speedy transistor, it also requires to have high speed interconnect in order to obtain superior overall system performance. Besides, providing pathways for electrical signals, interconnects also facilitate the supply of electrical powers to all processing nodes for their function. Any fault and failure in any interconnect line may compromise fidelity of information or lead to the failure of the entire chip. In current technology, more than 50% of capacitance in a CMOS IC is due to interconnects. As a result, more than 50% of dynamic power is consumed by interconnects [1]. This is why interconnect technologies require critical attention alone, with the transistors in a chip.

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[*]Part of the work is reported in the following publication:
A. Srivastava and K. M. Mohsin, "Thermal effects in carbon nanotube VLSI interconnects," *Nano-CMOS and Post-CMOS Electronics: Circuits and Design*, Institution of Engineering and Technology Press, 2016, pp. 172-200.

The more processing units an IC has, the more computation it can perform and as a result more connectors will be necessary. This has been the basic principle of 'scaling' for interconnects where by reducing the physical size of the interconnect, further interconnect paths can be placed to fit into a given chip area. At the same time since electrons will have to travel a shorter distance signal propagation speed will be increased. The idea goes back to 1965, when founder of Intel's Gordon Moore forecasted the increase functionality of ICs, commonly known as 'Moore's Law'. The law states that the number of transistors in an IC would double every 18 months. For nearly five decades, semiconductor industries have fulfilled the prediction of this rule by constantly pushing the computer chip technology and maintained a tremendous effort spanning from material selection, fabrication process and novel architectures to keep the progress uncompromised. However, Moore's law may be reaching its end and a new paradigm shift with a lot more interesting things are on the way [2].

1.1. Present Technology and Its Limitations

In present CMOS technology, copper is used as an interconnect material buried in low-*k* dielectric as shown in Fig.1.1[3] which started at the 220 nm technology node in 1997 introduced by IBM. For several reasons Cu successfully replaced Al (aluminum), a standard technology for chip makers for a long period. The key benefits of using Cu instead of Al are listed briefly in the following,

1. Cu offers 40% less resistivity than Al
2. RC delay decreases by 15%

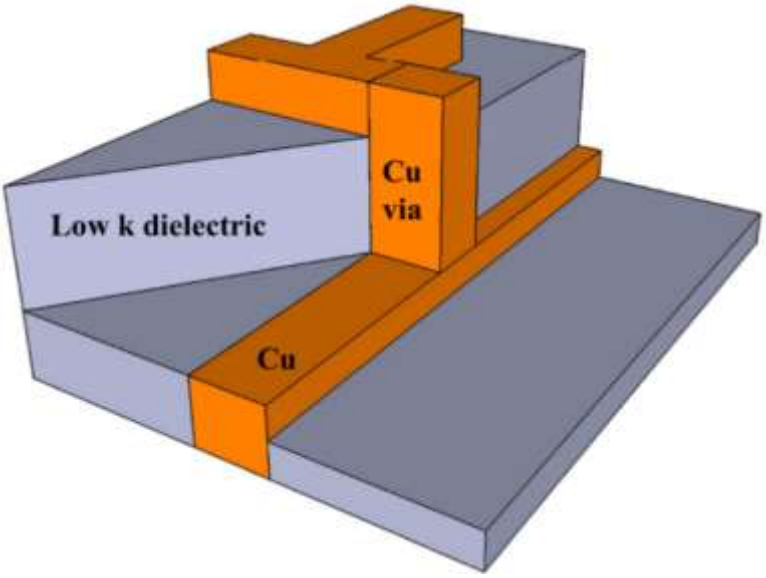

Figure 1.1: Cu/low-k interconnect technology.

3. More durable than Al with 100 times more reliability
4. Scalability of Cu is better than Al
5. Cu enables multiple layers of interconnect deposition with damascene technique

To reduce interference between two adjacent signals interconnect lines, low-k dielectric ($\epsilon_r < 3$) is being used as an interlayer dielectric (ILD) in present CMOS interconnect technology. For patterning Cu lines in a semiconductor chip, damascene technique [4] along with electrodeposition [5] is being used widely. However, unlike Al, Cu is more diffusive in to the interlayer dielectric. This is why a barrier layer is required to keep the metal-dielectric interaction minimum. First step of interconnect technology starts with the photolithography which is a essential step for patterning of metal lines on the previously deposited dielectric layer. Then on the patterned substrate, a barrier layer of tantalum on tantalum nitride (Ta/TaN) or titanium on titanium nitride (Ti/TiN) is deposited. The purpose of the first metal layer (Ti or Ta) is to increase the adhesion between the metal and dielectric layers. The purpose of the second layer, which is essentially a nitride (either TaN or TiN), is to stop Cu diffusion into dielectric. After deposition of this Ti/TaN (or Ta/TaN), a Cu seed layer is deposited by chemical vapor deposition (CVD). This seed layer works as a liner for the electro-chemical deposition of Cu.

Electro-chemical deposition is the main Cu layer deposition step in present interconnect technology. A process called chemical and mechanical polishing (CMP) is being used to planarize the deposited Cu layer. This completes one cycle of damascene technique for Cu deposition. To protect the deposited Cu lines from the top surface a capping layer usually silicon nitride is being used widely. After this silicon nitride, another layer of interlayer dielectric is being deposited which is followed by the next damascene process. This process repeats for several times for each

layer of metallization. Currently, 4-7 metal layers are being used by industry widely. In Fig. 1.2, a summary of current interconnect process technology is presented.

A rapid down scaling of MOSFETs happened following the Moore's law. In lieu of the continuous downsizing of transistors, interconnect technology also requires to be scaled down to get maximum benefit of downsizing. However, scaling down of Cu/low-*k* interconnect is suffering increased heating, electro-migration and void formation [6, 7].

In scaling of interconnects, low-dimensional effects dominate over the bulk properties of materials. Fig. 1.3 shows how resistivity of Cu line is deviating from its bulk resistivity value when line width approaches 10 nm [8]. In Fig. 1.3, *p*, *R* and *u* stands for specularity parameter, surface reflectivity and grain size respectively. Due to decreased volume, Joule heat generation per unit volume increases which causes resistance to increase. Metal ions in interconnect materials are swept by the high electric field and causes void formation which is known as electro-migration. On top of this electro-migration, Joule heating makes things worse. Due to Joule heating, center of interconnect reaches the melting point of the material and thermal run away causes open circuit. While void and open circuit formation due to electro-migration may happen after long periods of use, Joule heating may happen right after few clock cycles of use. These reliability issues are serious bottlenecks in scaled CMOS technology nodes.

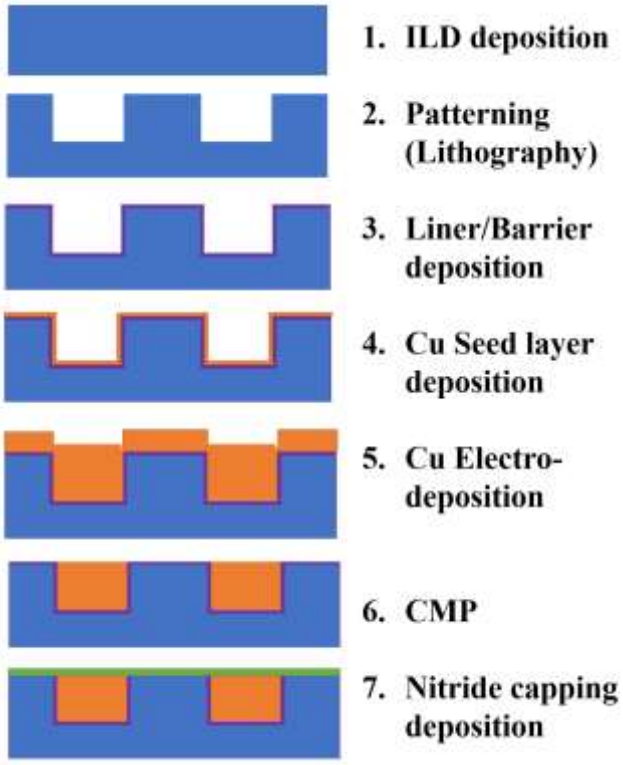

Figure 1.2: Current interconnect (Cu/low-k) process technology.

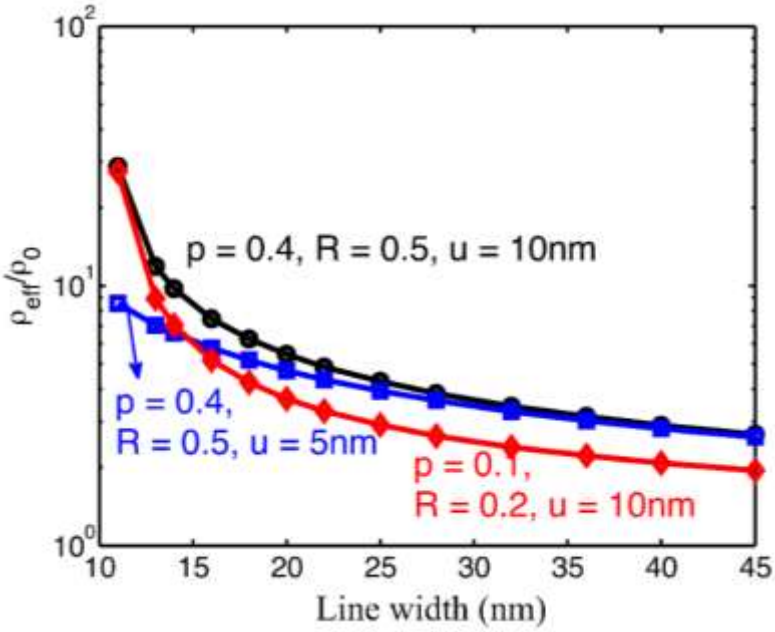

Figure 1.3: Increasing line resistance of Cu-low/k interconnect in scaled technology nodes.

As it has been presented in Fig. 1.4, interconnect delay is exponentially increasing with the shrinking down of technology nodes while transistor gate delay is decreasing linearly. Therefore, interconnect RC delay is dominant over the transistor gate delay [9].

Electromigration (EM) is a mechanism where gradual migration of metallic ions occurs due to electron drag. EM poses another reliability threat for present CMOS interconnect technology. When Joule heating is present on top of EM, interconnect life time decreases significantly. Fig. 1.5 illustrates EM effect and the related breakdown. Because of EM, void formation worsens over time and creates a complete open circuit. This open circuit may cause the failure of the entire or any vital part of the chip. This void formation is more frequent near the corner of the metal line bending.

1.2. Alternative Approaches

Due to the above-mentioned reasons, researchers are continuously in search of better interconnect technology. Following is a summary addressing all these problems in order to find new interconnect technology.

Emerging materials: Emerging materials might possibly give a better electro-thermal conductivity in solving present interconnect technology. New novel materials could be used for charge transport channel, low-k dielectric, interconnect capping, adhesive and liner/barrier. Efforts are being made to find a novel material to replace existing Cu-low-*k* dielectric.

Alternative state variable: Instead of charge carrier transport, some other state variable could be useful in scaling down interconnect technology. Following are few examples of alternate state variable.

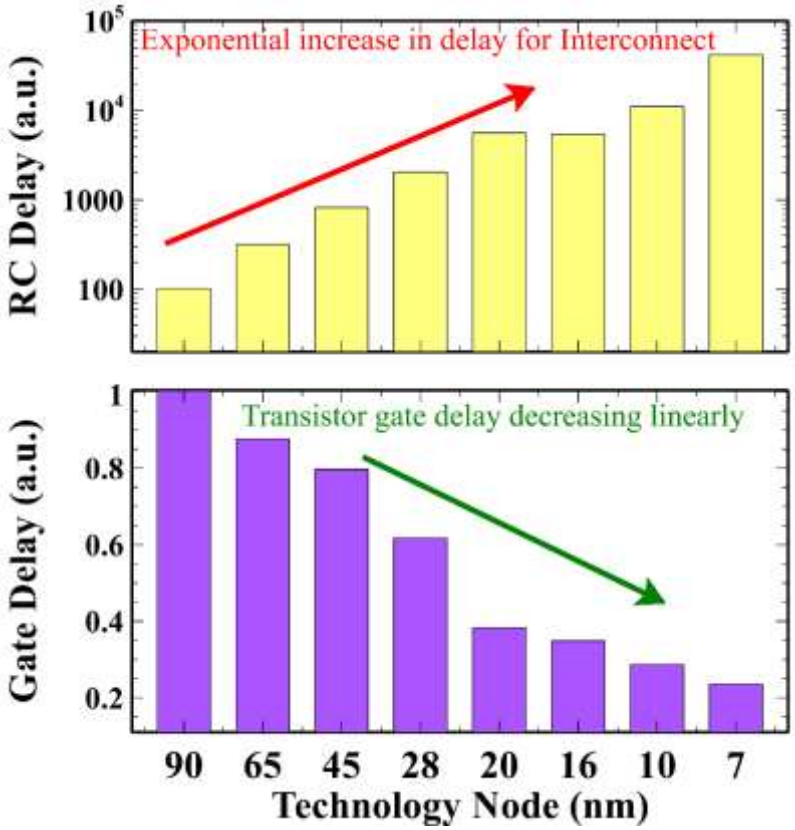

Figure 1.4: Comparison of transistor gate delay with interconnect's RC delay.

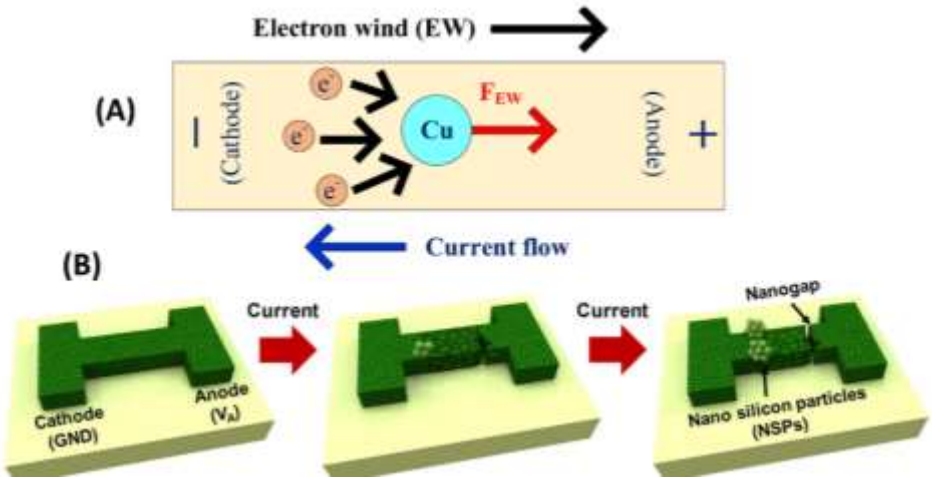

Figure 1.5: (A) Electromigration phenomena (B) Nanogap formation due to electromigration.

Electron's spin: As spintronic is evolving, researchers are also deploying spin transport techniques instead of charge transport in Si [12], metals [13], and graphene [14, 15]. Work is progressed in spin injection [16], transport and detection to realize spin interconnects [12-18]. Spin manipulation works in a very small energy scale and that is why spin interconnect will dissipate less heat than charge transport based interconnect.

Photon: Instead of electron, an optical interconnect works as a wave guide for photons. Since, photon is quanta of light and travels at the speed of light there will be lightning speed in signal transmission across the chips. In very high frequency applications (THz regime) metallic interconnect will fail to transport electrical signal due to increased dielectric loss and increased dynamic power. Hence, optical interconnect will be necessary in high frequency applications and also to obtain unprecedented floating point operations (FLOPS) and corresponding read/write operation [19]. Substantial research has been done in realizing photonics circuits and systems [20].

Phonon: Phonon works as the state variable and a rapidly growing research area called "Phononics" deals with phonon generation, injection and transport [21]. This state variable which is basically quantized atomic vibration modes of atoms was exploited in THz applications as a future interconnect [22].

Beyond above mentioned state variable "plasmon" and "excitons" are also very vibrant filed of research as an alternate state variable to "charge". These are few of many frontiers to address the interconnect issues. In this dissertation, emerging materials based solutions were looked for present interconnect technology.

1.3. Organization

In Chapter 2, carbon nanotubes application as a VLSI interconnect is discussed and a model is proposed to incorporate Joule heating effect into electrical performances. In Chapter 3, a theoretical ground of materials modeling for rest of the dissertation is presented. Density functional theory (DFT) techniques is the center point of this chapter. In Chapter 4, electrical properties of graphene on copper nanoribbon (G/Cu-NR) based interconnects are discussed. Electrical resistivity is estimated from the DFT calculations. In Chapter 5, quantum capacitance of G/Cu-NR which is a very crucial parameter for low dimensional system is reported. In Chapter 6, and application demonstration has been shown for the proposed interconnect materials. Future work is elaborated followed by conclusion in chapter 7. In appendices, necessary codes, simulation parameters and material data are provided.

CHAPTER 2
ELECRTRO-THERMAL TRANSPORT OF CNT BASED VLSI INTERCONNECT

2.1. Introduction

After the discovery of carbon nanotube (CNT) in 1991 by Iijima [23] many researchers envisioned it as the next generation interconnect material [24]. Numerous theoretical and experimental researches reached to the conclusion that CNT is the right choice of material due to its excellent electro-thermal properties [25-28]. In Table 2.1, few properties relevant to CNT VLSI interconnect technology are summarized and compared it to that of Cu. As shown in Table 2.1, different variants of CNT have two orders of more current capacity than Cu, and 5 to 10 times more thermal conductivity. Due to these exotic properties, researchers not only explored this carbon based material as the VLSI interconnect [24-27, 29, 30] but also as sensors [31, 32] and devices [33-36]. In interconnect design, one not only depends on superior electronic properties but also looks into thermal properties to avoid Joule heating induced thermal breakdown.

---

*Part of the work is reported in the following publication:

1. K. M. Mohsin, A. Srivastava, “Modeling of Joule heating induced effects in multiwall carbon nanotube interconnects,” IEEE Transaction VLSI, vol. 25, no. 11, pp. 3089-3098, Nov., 2017.
2. K. M. Mohsin, A. Srivastava, A. K. Sharma, and C. Mayberry, “A thermal model for carbon nanotube interconnects,” Nanomaterials, vol. 3, no. 2, pp. 229-241, April 26, 2013.
3. K. M. Mohsin, and A. Srivastava, "Characterization of SWCNT bundle based VLSI interconnect with self-heating induced scatterings," Proc. GLSVLSI '15, pp. 265-270, 2015.
4. K. M. Mohsin, Y. M. Banadaki, and A. Srivastava, "Metallic single-walled carbon nanotube based temperature sensor with self-heating," Proc. SPIE (Smart Structures/NDE: Nano-Bio-, and Info-Tech Sensors and Systems: SSNO6), pp. 906003-906003-7, 2014.
5. K. M. Mohsin, A. Srivastava, A. K. Sharma, and C. Mayberry, "Characterization of MWCNT VLSI interconnect with self-heating induced scatterings," Proc. IEEE Computer Society Annual Symposium on VLSI, pp. 368-373, 2014.
6. A. Srivastava, and K. M. Mohsin, "Thermal effects in carbon nanotube VLSI interconnects," *Nano-CMOS and Post-CMOS Electronics: Circuits and Design*, Institution of Engineering and Technology Press, 2016, pp. 172-200.

Table 2.1: Thermoelectric properties of Cu, SWCNT and MWCNT

Properties	Cu	SWCNT	MWCNT
Max current density (A/cm^2)	10^7	$>10^9$	$>10^9$
Melting point (K)	1356	870 [37]	3000-4000*
Thermal conductivity ($Wm^{-1}K^{-1}$)	385	1750-6000 [38]	3000 [39]
Mean free path (μm)	0.04	~1	25 (100 nm outer diameter)

*Reported in literatures to be close to the melting point of graphite.

Since CNT has high thermal conductivity it can quickly drain out the generated heat into the dielectric. This is why it is perceived that different variants of CNT interconnects will be inherently more thermally stable than the Cu based interconnect [25, 40]. In explaining electrical properties, Srivastava et al. [27, 41] explained how to use one dimensional fluid based model for SWCNT and MWCNT interconnects. Single conductor based transmission line model has been proposed by Sarto and SPICE compatible circuit models have been proposed by D' Amore et al. [42, 43]. Most of these works highlighted the electronic properties and overlooked the thermal stability. Chiang et al. [44] addressed the issue of Joule heating induced performance degrading of Cu-low-*k* interconnects. However, not much is reported in literature on Joule heating induced scattering, which is a serious roadblock in achieving the large current density. Pop [37] studied thermal break-down in metallic SWCNT with Fourier heat equation. One-dimensional Fourier heat equation has been used by Yamada et. al. [45] and Kitsuki et. al. [46] to explain experiments of carbon nanofiber thermal breakdown. Further literatures will be provided when necessary in the rest of the chapter in discussing all three variants of CNT.

2.2. Electrical Properties of CNTs

A CNT is rolled up in a single layer graphene sheet consisting sp^2 hybridized carbon atoms with 0.142 nm bond length as shown in Fig. 2.1. Depending on the number of layers of graphene, CNT could be single walled (SWCNT) or have multiple walls (MWCNT). Geometry of a SWCNT is just a hollow cylinder while MWCNT consists of multiple concentric cylindrical shells. Each of these shells is a rolled over single layer sp^2- sp^2 hybridized sheet of carbon atoms. Hence, MWCNT is a piling of concentric multiple SWCNTs where each shell has essentially different diameters. All the layers are bonded by the weak Van der Waals attraction forces with bonding length 0.34 nm [47]. Beside naturally obtained bundle of SWCNT and MWCNT or any of their mixed kind, it is also possible to use isolated SWCNT or MWCNT as VLSI interconnect. In this chapter, focus is only on SWCNT, MWCNT and SWCNT bundle. Same approaches can be applied for MWCNT bundle and any kind of mixed bundle. In the next section, electrical properties of different CNTs will be discussed.

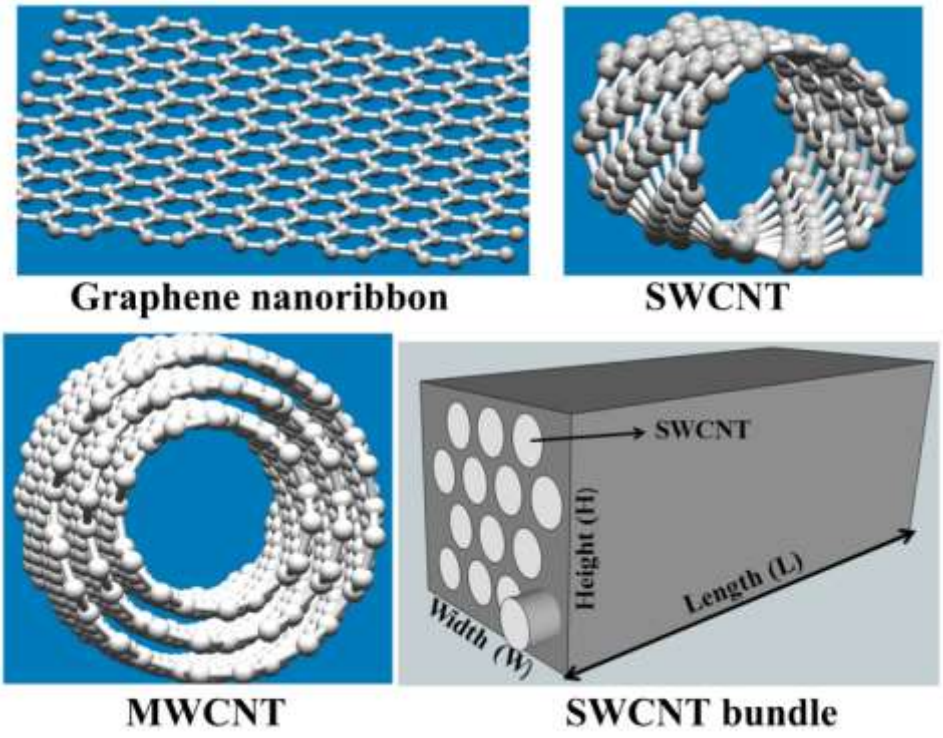

Figure 2.1: Different carbon-based nanomaterials.

2.2.1. Equivalent Resistance (R_{eqv})

An isolated SWCNT can be implemented in between metal contacts as interconnecting wire as shown in Fig. 2.2. Earlier it was challenging to align SWCNTs in between the contacts but recently that has been implemented successfully [48]. For interconnect applications, SWCNT can also be replaced by MWCNT or SWCNT bundle to get a better performance in terms of current capability. Electrically SWCNT can be approximated as one-dimensional conductor [49]. MWCNT or SWCNT bundle can be approximated as parallel SWCNTs. In case of MWCNT, all the shells are concentric and shell diameters are necessarily different. However, in SWCNT bundle it is not necessary to have different shell diameters.

SWCNT bundle shown in Fig. 2.1 is of same shell diameter. In this section, a set of general formulae to estimate electrical properties applicable to these three variants of CNT are presented. From Landauer-Büttiker, formalism, dc resistance of a CNT shell, R_k, can be calculated from Eq. (2.1).

$$R_k = \frac{h}{2q^2}\frac{1}{M_k}\left(1+\frac{L}{\lambda_{eff}(L, D_k, T_k, V)}\right) \tag{2.1}$$

where different parameters are defined as follows:

L = length of interconnect,

D_k = diameter of kth shell in MWCNT or in SWCNT bundle,

T_k = temperature of kth shell,

q = electronic charge,

h =Plank constant,

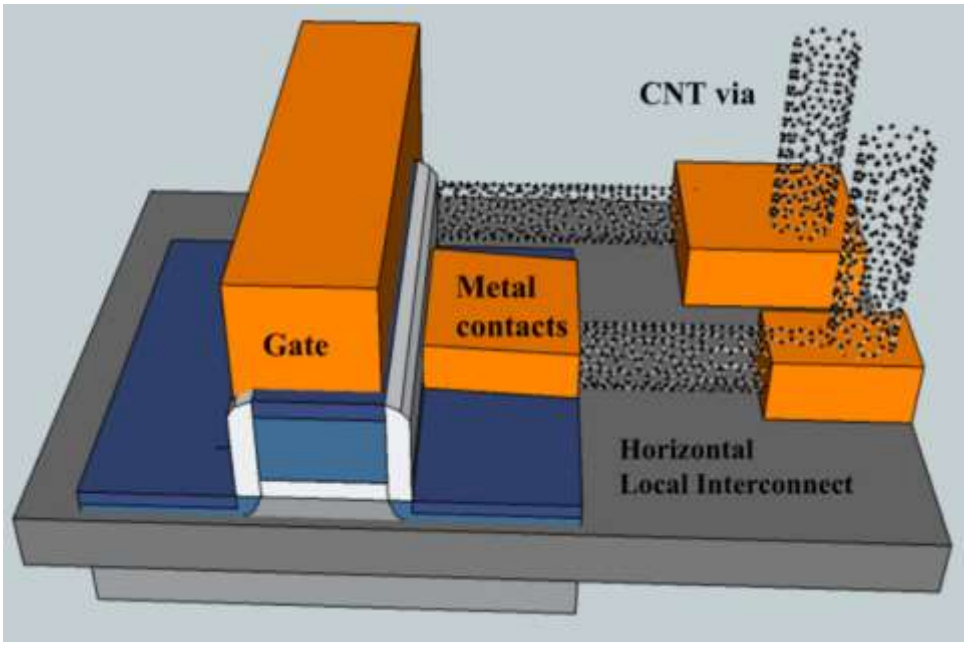

Figure 2.2: SWCNT based VLSI interconnects.

λ_{eff} = effective mean free path of an electron,

M_k = equivalent conducting channels (spin degenerate), and

V = biasing voltage across interconnect.

The effective mean free path, λ_{eff} takes into account the electron scattering with acoustic and optical phonons and will be discussed in Section 2.4.4. For SWCNT, D_k is just the shell diameter of CNT.

The first term in Eq. (2.1) is quantum in nature and the second term is a diffusive resistance, which is proportional to the length. It is apparent from Eq. (2.1) that even for the zero length, resistance is nonzero because of the first term, quantum resistance. This nonzero resistance is due to the effect of contacting quantum channels. Each spin channel contributes to h/q^2 resistance. Considering spin "up" and "down" running parallel, overall resistance for each channel is $h/2q^2$. Now considering M_k as the average number of transport channels in each shell the total quantum resistance will be the first term in Eq. (2.1). The "contact resistance" should not to be confused with this first term, quantum resistance. It is the contribution of contact in intrinsic part of the interconnect. To clarify further, here only CNT resistance is taken in to account not considering "CNT-metal" interface resistance or "contact resistance". Hence, to get the total resistance including contacts one requires adding contact resistance. Otherwise, this Eq. (2.1) will only compute the intrinsic resistance of the materials at hand. The inclusion of "CNT-metal" contact resistance into the model can be obtained by Eq. (2.4). The discussion of this contact resistance followed by Eq. (2.4).

For SWCNT there is only one shell. However, for MWCNT and SWCNT bundle different shells could be at different temperatures. This is why in Eq. (2.1), T_k has been introduced to take

into account the temperatures of different shells. M_k is the equivalent conducting spin degenerate channels of interconnect. For metallic SWCNT it is 2. Statistically for naturally obtained SWCNTs, 1/3 are metallic and 2/3 semiconducting. From statistics, one can estimate M_k value of any kind of CNT interconnect with the following equation [50],

$$M_k = \begin{cases} \frac{2}{3} & for\ D_k < \frac{1900}{T_k} \\ a_1 D_k T_k + a_2 & for\ D_k > \frac{1900}{T_k} \end{cases} \tag{2.2}$$

Where, a_1 and a_2 are fitting parameters. It is noteworthy that spin degeneracy has been taken into account in Eq. (2.2). Fitting parameters a_1 and a_2 take the values as 3.26×10^{-4} $nm^{-1}K^{-1}$ and -0.08, respectively. Since Eq. (2.2) has been calculated from the knowledge of band structure, it can be used reliably as a compact equation for quick estimation of resistance of interconnect without any detail calculations. Now from Eqs. (2.1) and (2.2), the resistance of each CNT shell can be obtained regardless of whether they are metallic or semiconducting. Equivalent resistance of MWCNT or SWCNT bundle can be obtained assuming that CNT shells are parallel electrical conductors. On the other hand, SWCNT having only single shell its equivalent resistance R_{eqv} is R_k itself. Details of SWCNT modeling has been explained in our work reported in [49].

To estimate equivalent resistance of SWCNT bundle or MWCNT, one requires to have a knowledge of total number of CNT shells in that particular kind of CNT based interconnect. In case of MWCNT (Fig. 2.3), total number of shells, N_{shell}, can be obtained from Eq. (2.3) as follows,

$$N_{shell} = 1 + \left(\frac{D_{out} - D_{in}}{2\delta}\right) \tag{2.3}$$

where various parameters are described below,

D_{out} = outer diameter of a MWCNT,

D_{in} = inner diameter of a MWCNT and

δ = inter shell gap and equals to 0.34 nm.

In Fig. 2.3. MWCNT and its distribution of concentric shell is shown where MWCNT is lying on a ground plane. Here t_{ILD} is the thickness of interlayer dielectric. After obtaining the total number of shells in MWCNT, equivalent resistance of interconnect can be obtained. Since all these shells are contributing in transport with their average number of conducting channels regardless whether these are metallic or not; by combining them together will give the total contribution of all shells. Equivalent resistance can be then obtained from the following equation [51],

$$\begin{aligned} R_{eqv} &= \left(\frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_k} + .. + \frac{1}{R_{N_{shell}}}\right)^{-1} + R_{contact} \\ &= \frac{h}{2q^2}\left(\sum_{k=1}^{N_{shell}} \frac{M_k \lambda_{eff}(L, D_k, T_k, V)}{\lambda_{eff}(L, D_k, T_k, V) + L}\right)^{-1} + R_{contact} \end{aligned} \tag{2.4}$$

In Eq. (2.4), $R_{contact}$ is non-ideal resistance between CNT and metal. Contact resistance has been measured and is found varying widely because of contact metal, contact area, contact length and defects [52]. As reported contact resistance varies from few hundreds of ohms to several kilo-ohms [37, 53, 54]. In this study, an experimental value of 1 $k\Omega/m^2$[55] is used. It is obtained by calculating the annular contact region multiplied by 1 $k\Omega/m^2$.

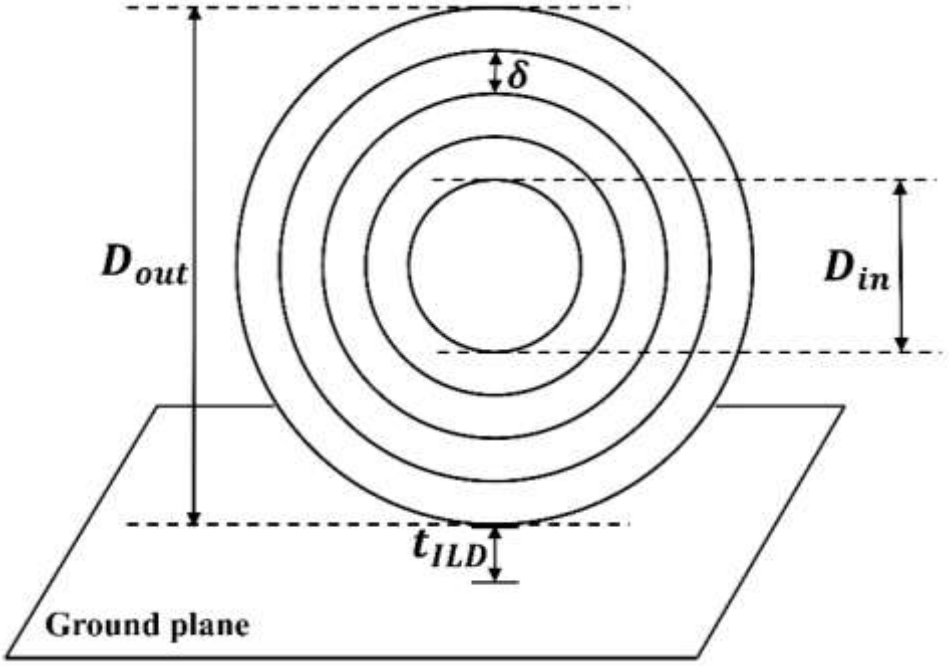

Figure 2.3: Concentric circles showing MWCNT shells with the ground plane.

SWCNT bundle can be obtained by piling SWCNTs in different geometrical shapes. In this work, rectangular shape as shown in Fig 2.1 is considered. This is the most common interconnect geometry for VLSI technology. For SWCNT bundle, total number of CNT shells is different and can be obtained from the following equation:

$$N_w = Int\left\{\frac{W - D}{D + \delta}\right\} + 1 \tag{2.5}$$

$$N_H = Int\left\{\frac{2(H - D)}{\sqrt{3}(D + \delta)}\right\} + 1 \tag{2.6}$$

$$N_{shell} = N_W N_H - Int\left\{\frac{N_H}{2}\right\} \tag{2.7}$$

where various parameters are explained as follows,

N_w = number of CNT shells in the direction of width,

N_H = number of CNT shells in the direction of Height,

D = diameter of CNT and

δ = inter shell gap and equals to 0.34 nm.

Function *Int* computes an integer value for everything enclosed in by curly brackets. Eq. (2.7) counts N_{shell} as the total number of SWCNT shells, which could fit for a rectangular cross-sectional geometry of SWCNT based interconnect. Once N_{shell} is available, Eq. (2.4) can be used to estimate the equivalent resistance of SWCNT bundle based interconnect. Again, for SWCNT, N_{shell} is 1.

2.2.2. Equivalent Inductance (L_{eqv})

After knowing equivalent resistance, it is important to estimate the inductance and capacitance of interconnect. For small device dimension besides classical electrostatic

capacitance, there is also quantum capacitance. For the same reasoning besides magneto-static inductance, there is also kinetic inductance. In this section, formulae for these both kinds of inductances associated with different kinds of CNT based interconnects is disucssed. Magnetic inductance, L_{MK}, which depends on the geometrical factor, can be obtained from Eq. (2.8) for a cylindrical conductor [27],

$$L_{Mk} = \frac{\mu}{2\pi} \ln\left(\frac{h_k}{2r_k}\right) \tag{2.8}$$

where various parameters are described as follows,

h_k = distance between ground plane and the center of kth CNT shell,

r_k = radius of CNT shell, and

μ = magnetic permeability of the CNT environment.

This magnetic inductance is quite important for SWCNT because of the small diameter. However, for a MWCNT with many concentric shells the magnetic inductance plays a lesser important role in overall inductance. Since diameters of outer shells are large, magnetic inductance becomes less significant for outer shells. Again, if one counts these in parallel to estimate overall inductance it will be less significant. Quantum inductance which comes in series with the magnetic inductance, L_K, can be estimated from the following equation [56],

$$L_K = \frac{\pi\hbar}{2q^2 v_F M_k} \tag{2.9}$$

Where v_F is Fermi velocity (8.854×10^5 ms^{-1}) [42], and $\hbar$ is reduced Planck constant. To obtain equivalent inductance, one requires adding right side of Eqs. (2.8) and (2.9) and then counting them in parallel as done in the case of equivalent resistance in Eq. (2.4). Calculations would be easier if one assumes that magnetic inductance is less significant in comparison to kinetic inductance. In case of SWCNT bundle, while taking all the shells into consideration, contribution from magnetic inductance will be divided by the total number of shells. In case of MWCNT, different shells correspond to different diameters. Shell diameters of a MWCNT increases from center to the surface. For increased diameter, magnetic component of inductance becomes less important as described in Eq. (2.8). For instance, for a MWCNT with 100 nm outer diameter, quantum inductance of innermost shell is 5.8188×10^4 times greater than the claimed magnetic inductance of that shell [51]. On the other hand, SWCNT with a diameter of ~1 nm and oxide thickness over which SWCNT is deposited is ~100 Å, the calculated value of L_{Mk} ~1 pH/μm which is very small compared to the value of L_{k} which is in the range of nH/μm. With this argument, one can simplify the equivalent inductance though with some loss of accuracy and express by the following equation,

$$L_{eqv} = \frac{\pi\hbar}{2q^2 v_F \sum_{k=1}^{N_{shell}} M_k} \tag{2.10}$$

N_{shell} can be calculated for MWCNT and for SWCNT bundles from Eqs. (2.3) and (2.7) respectively. In case of metallic SWCNT, total number of conducting channels are only 2. For SWCNT bundle and MWCNT based interconnect one needs to carry summation over all CNT shells to obtain total number of conducting channels. It is to be noted that total number of shell is

different than the total number of conducting channels. Number of shells is a physical quantity which counts the total number of SWCNT tubes fitted in to the interconnect geometry. On the other hand, number of conducting channels are electronic channels, which are coming from the band structure calculations. One CNT shell might have multiple electronic channels for transportation of electrons. Finally, for SWCNT bundle based interconnect assuming same diameters of all CNTs one can further simplify the equivalent inductance from Eqs. (2.2) and (2.10) as follows,

$$L_{eqv} = \frac{\pi\hbar}{2q^2 v_F \sum_{k=1}^{N_{shell}} M_k} = \frac{3\pi\hbar}{4q^2 v_F N_{shell}} \tag{2.11}$$

2.2.3. Equivalent Capacitance (C_{eqv})

As for inductance, small dimensional interconnects have two kinds of capacitances. One is electrostatic in nature and depends on the geometric shape and dielectric constant of materials. The other one is quantum in nature. Electrostatic capacitance (C_{EK}) of a CNT is similar to a cylindrical conductor and can be estimated as follows,

$$C_{Ek} = \frac{2\pi\varepsilon}{\ln\frac{h_k}{2r_k}} \tag{2.12}$$

where, ε is dielectric permittivity, h_k is distance between ground plane and the center of k^{th} CNT shell and r_k is radius of CNT shell. Quantum capacitance is in series with this electrostatic capacitance and can be estimated from the following equation [3],

$$C_Q = \frac{2q^2}{hv_F} M_k \quad . \tag{2.13}$$

For metallic SWCNT M_k is 2. Usually, everyone wants a material with low dielectric constant as an ILD to surround the interconnect into. Since electrostatic and quantum capacitances are in series, the one lower in value will dominate in estimation of overall capacitance. If the dielectric constant is low and the distance of interconnect layer from the ground plane is high electrostatic capacitance will dominate over the quantum capacitance. Actually, there is no general rule to find out which one will dominate over the other one. Therefore, for detail calculations one always requires to include both of them to estimate equivalent capacitance numerically. However, to express analytically one can make simplified assumptions. Electrostatic capacitance is dominant over quantum capacitance only for MWCNT with fewer shells. For a MWCNT with more shells quantum capacitance is approximately thousand times more than the electrostatic capacitance of the outer shell [51]. Hence, in calculation of equivalent capacitance considering only quantum capacitance is a good approximation. Considering only quantum capacitance, equivalent capacitance can be then estimated from the following equation,

$$C_{eqv} = \frac{2q^2}{hv_F} \sum_{k}^{N_{shell}} M_k \tag{2.14}$$

For SWCNT bundle, it can be further approximated using Eq. (2.15) as follows,

$$C_{eqv} = \frac{2q^2}{hv_F} \sum_{k}^{N_{shell}} M_k = \frac{4q^2 N_{shell}}{3hv_F} \tag{2.15}$$

2.2.4. Effective Mean Free Path (λ_{eff})

One of the most important parameter in electronic transport properties is the carrier mean free path (MFP). In CNT, electrons are the major charge carriers. Electrons in a CNT go through many different collisions. In this section, different mean free paths associated with different collisions are calculated and finally Matthiessen's rule is to be used to estimate effective MFP, λ_{eff}, of an electron. Phonons are quantized lattice atom vibrations. Due to vibrations, positive ions of atoms are displaced from their equilibrium positions and this changes the potential profile in the atomic scale. This change in potential is the cause for delocalized electrons to get scattered. Optical phonons and acoustic phonons interact with mobile electrons and thus scatter electrons. Even without any biasing, electrons spontaneously get scattered with the optical and acoustic phonons. Scattering lengths of electrons due to acoustic (λ_{ac}) and optical phonons (λ_{op}) can be estimated from the following equations [57],

$$\lambda_{ac} = \frac{400.46 \times 10^3 D}{T} \tag{2.16}$$

$$\lambda_{op} = 56.4D \tag{2.17}$$

In Eqs. (2.16) and (2.17), D is the diameter of a SWCNT and T is the temperature of a particular shell. The increase in temperature increases the population of acoustic phonons, which eventually increases the collision rate. Hence, an increase in temperature decreases the scattering length of electrons. The scattering length, λ_{ac} contributes directly to MFP. However λ_{op}, which is only

dependent on the diameter, needs to be modified with temperature dependence as in Eq. (2.18). An electron can get scattered by absorbing or emitting an optical phonon. The scattering length due to optical phonon absorption, $\lambda_{op,abs}$, has been modeled by the following equation [37],

$$\lambda_{op,abs} = \lambda_{op} \frac{N_{op}(300) + 1}{N_{op}(T)} \tag{2.18}$$

In Eq. (2.18), λ_{op} can be obtained from Eq. (2.17). N_{op} in the following describes the optical phonon occupation, which is the Bose-Einstein statistics and given by,

$$N_{op} = \frac{1}{\exp\left(h\omega_{op}/K_B T\right) - 1} \tag{2.19}$$

In Eq. (2.19), ω_{op} is the optical phonon frequency and its typical energy value varies from 0.16 eV to 0.20 eV. For numerical calculations, this value is taken as 0.16 eV. From Eq. (2.19), it is obvious that as the temperature increases, N_{op} increases. Consequently, if N_{op} increases, scattering length due to optical phonon absorption ($\lambda_{op,abs}$) decreases according to Eq. (2.18). Therefore, at a high temperature or high bias, an electron suffers more scatterings due to optical phonon absorption. Electrons also get scattered due to the emission of optical phonons. Optical phonon emission process has two components. One is due to the absorbed energy. The other component is due to the electric field induced by the bias across the SWCNT length. Both of these components can be estimated as follows:

$$\lambda_{op,ems}^{abs} = \lambda_{op,abs} + \lambda_{op} \frac{N_{op}(300) + 1}{N_{op}(T) + 1}. \tag{2.20}$$

$$\lambda_{op,ems}^{fld} = \frac{h\omega_{op} - K_B T}{qV/L} + \lambda_{op} \frac{N_{op}(300) + 1}{N_{op}(T) + 1}. \quad (2.21)$$

In Eqs. (2.20) and (2.21), q is electronic charge, V is the bias voltage across the CNT and L is the length. From Matthiessen's rule, one can estimate the MFP due to these aformentioned scattering processes and is expressed as follows,

$$\frac{1}{\lambda_{op,ems}} = \frac{1}{\lambda_{op,ems}^{abs}} + \frac{1}{\lambda_{op,ems}^{fld}}. \quad (2.22)$$

Eq. (2.22) estimates the effective MFP only due to the optical phonon emission. Following equation can be used to estimate overall MFP of electrons.

$$\frac{1}{\lambda_{eff}} = \frac{1}{\lambda_{ac}} + \frac{1}{\lambda_{op,ems}} + \frac{1}{\lambda_{op,abs}} \quad (2.23)$$

Near charge neutrality point, electron-electron scattering mean free path is on the order of several micrometers and it is observed experimentally [58]. Because of the large mean free path, electron-electron interaction is not a dominant scattering event to consider in Eq. (2.23) while electron-phonon scatterings are the dominant events [59]. Eq. (2.23) serves as a quick estimation of effective MFP of an electron. The effective MFP (λ_{eff}) can be used in Eq. (2.4) to estimate the temperature and geometry dependent equivalent resistance of CNT interconnects.

2.2.5. Equivalent Circuit

Once the equivalent resistance is obtained, inductance and capacitance of a CNT interconnect, one can model its equivalent circuit. Yao et al. [41] and D'Amore et al. [60] have

showed how to model equivalent circuit for MWCNTs . SWCNT bundle has been modeled by Sarto et al. [61]. These models mostly involved RLC parameters of multiple lines and coupling impedance in between lines. In inductance and capacitance, they considered both the classical and quantum counterparts. However, it is required to have a single conductor transmission line model to describe the electrical performances in a way that is more compact. It is to be noted that compact modeling can help to simulate a large system with limited computing resource. Sarto et al. [42] proposed single conductor transmission line model for the MWCNT which can be modified for any kind of CNT. Following this one can have a single conductor transmission line model for any kind of CNT as described here. Only the equivalent R, L and C values will be different depending on which kind of CNT interconnect needs to be modeled. For high frequency characterization of interconnect, this transmission line model will be very useful. In scattering parameter calculations, this equivalent single conductor model has been used along with per unit length circuit parameters. Equivalent circuit is as shown in Fig. 2.4.

2.3. Thermal Properties

Now it is important to know thermal properties and to study how these affect electronic transport. The motivation of this chapter is to examine how Joule heating limits electronic transport through CNT VLSI interconnects. Therefore, it is important to analyze different CNT variants in terms of thermal stability. The fundamental approach is to model temperature distribution and to study thermal stability of interconnect. Phenomenological heat diffusion equation can be used as long as the length of CNT is long enough in comparison to the mean free path of a phonon. If the CNT length becomes comparable to the phonon mean free path necessary

physics cannot be described by the phenomenological Fourier heat equation. In the latter case, one needs to solve the Boltzmann transport equation (BTE) for phonons which is less intuitive and computationally more expensive. Again, standard BTE has its own limitations of treating phonon as a classical particle instead of the quantum nature of phonon. Cahill et al. [62, 63] have reviewed the recent progress of thermal transport in the nanoscale dimension. In most of the practical cases, CNT lengths are in the order of a few micrometers whereas phonon effective MFP is in the order of a few hundreds of nanometers. Therefore, it is permissible to use Fourier heat equation with necessary boundary and initial conditions. In this section, different variants of Fourier heat equation are described with their boundary conditions for different kinds of CNT interconnects. Since MWCNT and SWCNT bundle consists of SWCNT in different geometric orientations it is natural to study the thermal properties of SWCNT based interconnect first and then other variants of CNT.

2.3.1. Thermal Properties of SWCNT

SWCNT is a quasi-one-dimensional and does not have enough surface area and cross-sectional area to dissipate heat. Hence it is prone to thermal break down more than any other variants of CNT. Even though SWCNT is highly heat conductive, it has been observed experimentally that the conducting carbon nanotube breaks down due to Joule heating and thus limits its current density [64, 65]. Thermal break down of SWCNT has been studied by Pop et al. [37]. Huang et al. [66] have studied thermal transport and observed experimentally that the hottest

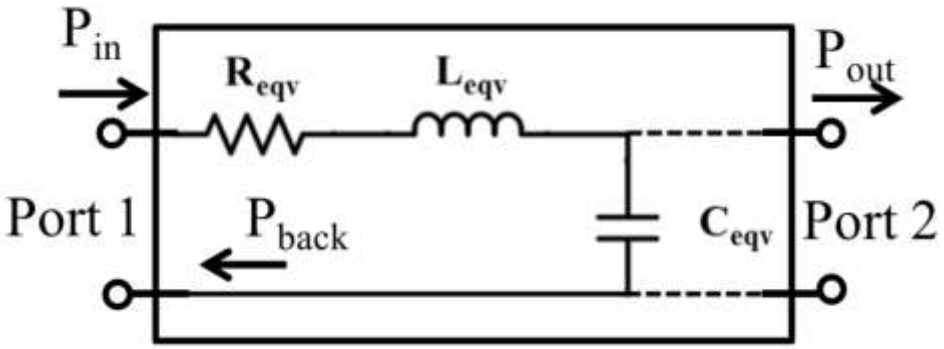

Figure 2.4: Single conductor transmission line model of CNT interconnect.

spot is located at the center of the tube from where breakdown is initiated. Geometry of SWCNT is essentially a single one-dimensional wire. Therefore, the Fourier heat equation can be described by one-dimensional equation.

$$\frac{\partial}{\partial z}\left(A\kappa\frac{\partial T}{\partial z}\right)+p=A\rho c\frac{\partial T}{\partial t} \tag{2.24}$$

In Eq. (2.24), κ is the heat conductivity, A is the cross-sectional area ($D\pi\delta$), t is time, T is the temperature at a given point of SWCNT, p is Joule heating source power per unit length, c is specific heat of CNT and ρ is density of CNT. A typical diameter of SWCNT is 1 nm and thickness is 0.34 nm which is the interlayer distance in graphite. Under the assumption of uniform heating, uniform cross sectional area of CNT, steady state solution can be obtained using the work of Pop et al. [37],

$$A\frac{\partial}{\partial z}\left(\kappa\frac{\partial T}{\partial z}\right)+p-g\left(T-T'\right)=0 \tag{2.25}$$

where T' is the substrate temperature, g is the measure of heat conductivity of CNT through substrate. The higher value of g implies that CNT will be more thermally stable. Right hand side of Eq. (2.25) equals zero since a steady state solution is preferred. Being a one-dimensional problem, only one boundary condition is required to solve this problem. Typical substrate temperature is 60°~70°C. Again, g depends on the interface of CNT and substrate and can either be measured experimentally or can be estimated from extensive first principle calculations. Pop et al. [37] measured the value of g associated with silicon substrate and found its value to be 0.15

$Wm^{-1}K^{-1}$. Thermal conductivity (κ) is the most disputed parameter for CNT. It ranges from few hundreds to few thousands of $Wm^{-1}K^{-1}$. In the work of Yamada et al. [45] and Kitsuki et al. [46] thermal transport has been studied considering the thermal conductivity of CNT as constant. However, studies in [37, 40, 53, 67-69] have shown that the thermal conductivity is temperature dependent. This is why one needs to check with the most recent agreed experimental values for thermal conductivity until an established theoretical and experimental value has been obtained. For a constant value for thermal conductivity (κ) a compact analytical solution has been shown in [37] as follows:

$$T(z) = T' + \frac{p}{g}\left[1 - \frac{\cosh\left(\frac{z}{\sqrt{\kappa A g}}\right)}{\cosh\left(\frac{L}{2\sqrt{\kappa A g}}\right)}\right]. \tag{2.26}$$

One of the important outcomes of Pop's study [37] is defining thermal healing length as follows:

$$L_H = \sqrt{\kappa A g}\ . \tag{2.27}$$

If the length of CNT is very large in comparison to the thermal heating length (L_H) most of the heat will be lost by the substrate. On the other hand, if the length is comparable to L_H most of the heat diffuses through the contacts. In Eq. (2.26), p/g determines the peak temperature of the hottest spot which is the midpoint (z=0) temperature of SWCNT. Now from Eq. (2.26), one can find the temperature distribution for a given Joule heating (p) per unit length which is I^2R per unit length. Therefore, Eq. (2.26) is resistance (R) dependent. Again from Eq. (2.4) one knows that R is T dependent. Hence, there is a nonlinear relationship between R and T. This nonlinear relationship

can be taken into account by the iterative scheme, which is discussed in Section 2.3.4. Once T and R can be calculated from the coupled electro-thermal equations, thermal stability can be determined. If the temperature at any point of a SWCNT goes above the breakdown temperature 873 K, it melts down at that point and breaks the circuit. Since peak temperature is being determined by p ($=I^2R$), thermal stability depends directly on the bias current. This is how the Joule heating limits the current density and in worst case scenario, causes thermal breakdown of interconnects. For a 3 μm long SWCNT and 2 nm diameter, maximum current has been calculated to be 20 μA [37, 65]. Since longer SWCNT has more contacts with substrate it can dissipate heat quicker than the shorter one. Hence a length dependence of thermal stability comes into the picture. In our previous work reported in [49], length dependence of resistance has been presented as shown in Fig. 2.5. To summarize, length, diameter, temperature and bias voltage or bias current decide the mean free path and resistance of CNT interconnect. Resistance and temperature are intertwined and needs to be solved with iterative scheme described in Section 2.3.4.

2.3.2. Thermal Properties of SWCNT Bundle

Heat equation for SWCNT bundle is a three-dimensional problem to be solved with necessary boundary conditions. If the cross-sectional area is very small and the length is very large, one can assume it as a one-dimensional problem. For one-dimensional case, the solution of heat equation is already discussed in previous section. However, in case of local interconnect the cross-section is large enough and interconnect is not comparatively long enough to assume one-dimensional problem. Hayashi et al. [70] noted that there is anisotropy of heat conductivity in MWCNT. This anisotropy suggests that heat conductivity is very high in axial direction in comparison to the radial direction. Since MWCNT and SWCNT bundle only vary in placement

of SWCNT shell in different geometric orientation; similar anisotropy is also possible for SWCNT bundle. Heat conductivity will be always dominant in axial direction while electron and phonon transport is happening in the shell. In contrast whenever transport involves with an adjacent shell, heat carriers need to face the inter-shell thermal resistance. Hence heat conductivity will not be high in the radial direction. Therefore, in cross-section of SWCNT based interconnect temperature gradient will be observed. There will be a temperature distribution in the cross-section of SWCNT bundle based interconnect due to this anisotropy of heat conductivity. A cross sectional distribution of temperature means different SWCNT wires will be at different temperatures causing different temperature dependent resistance (R_k). Thus, a three-dimensional heat equation is to be solved as follows:

$$\frac{\partial}{\partial x}\left(A\kappa_x \frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(A\kappa_y \frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(A\kappa_z \frac{\partial T}{\partial z}\right)+ p - g\left(T - T'\right) = A\rho c \frac{\partial T}{\partial t}. \qquad (2.28)$$

Where, κ_x, κ_y, and κ_z is heat conductivity in x,y and z directions. The geometry of SWCNT bundle based interconnect is a three-dimensional rectangular bar, $p= (I^2R_{eqv})/ (WxLxH),$ where W, L, and H are width, length and height of interconnect. Substrate temperature T' can be taken as 300 K and will serve as a boundary condition for solving Eq. (2.28). Definition of other parameters are given in the previous section. Under the following assumption, one can simplify Eq. (2.28) to solve this problem analytically or numerically. Following assumptions are made:

1. Heat generation is uniform throughout the whole interconnect
2. Cross-section of interconnect is uniform

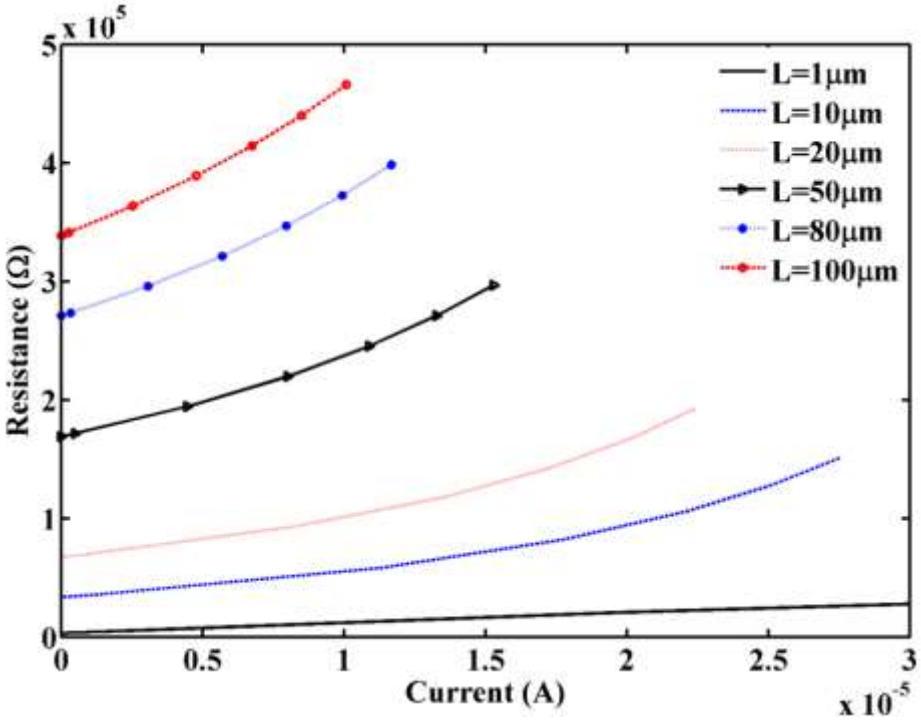

Figure 2.5: Length dependence resistance of SWCNT interconnect.

3. Anisotropy of heat conductivity is only two-dimensional: radial and axial direction of a CNT
4. Steady state solution
5. Interconnect length is short enough so there will be no temperature variation along the length (z-axis)

Considering above-mentioned assumptions, following equation is to be solved:

$$\kappa_x \frac{\partial^2 T}{\partial x^2} + \kappa_y \frac{\partial^2 T}{\partial y^2} + p - g\left(T - T'\right) = 0\,. \tag{2.29}$$

In Eq. (2.29), constant cross-sectional area (A) can be absorbed into other constants. Heat conductivity through substrate (g) is yet to be measured experimentally for SWCNT bundle based interconnect. Although heat generation might not be uniform in real experiments we assumed it for the simplicity of modeling.

2.3.3. Thermal Properties of MWCNT

Three-dimensional MWCNT is inherently more stable than SWCNT in terms of thermal stability. On top of thermal stability, growth techniques of MWCNT are easier than SWCNT. This is why MWCNT is preferred over SWCNT as the VLSI interconnect. For better understanding the performances of various CNT interconnects and to compare them it is essential to study MWCNT interconnect as well. Temperature distribution along the MWCNT considering Joule heating has been reported by Feng et al. [71] and later they studied the cross-talk effects for the VLSI interconnect [72].

In most of early studies of MWCNT based interconnect, radial heat flow has been neglected assuming graphite like isotropic thermal conductivity of MWCNT [45, 71]. Hayashi et al. [70] have reported that due to anisotropy of thermal conductivity temperature variation can also be observed in the cross-section of MWCNT. It is necessary to include this anisotropy in consideration to get accurate results. From the experimental results Hayashi et al. [70] calculated thermal conductivity in axial direction as κ_{axial} =1800 $Wm^{-1}K^{-1}$ and in radial direction, κ_{radial}=0.05 $Wm^{-1}K^{-1}$. This is a significant anisotropy that is to be taken into account in thermal study. Since axial component is very high in comparison with the radial component it is suggestive that heat dissipation along the length of MWCNT is quicker than in radial direction. Hence MWCNT interconnect will quickly reach thermal equilibrium along all over the length but in cross-section it may not be that quick. This is how anisotropy of thermal conductivity will cause temperature variation in cross-section. However, temperature variation will not be significant in the direction of length for the aforementioned reason. One can take this as an advantage to reduce the problem from three-dimension to two-dimension by considering only the cross-section. Again, under the assumption of uniform diameter throughout and all over the length, one can assume that heat will not flow in circumferential direction too. Therefore, one can reduce the heat equation to a radial equation.

Although, Hayashi et al. [70] modeled MWCNT in two-dimensional cylindrical co-ordinates with anisotropic values of thermal conductivity they did not take the Joule heating generation term in their governing equation. In our previous work reported in [51], heat generation term was considered but conduction through dielectric (g) was not presented. To be more accurate one should always include all heat sources and sinks which are shown in Fig. 2.6.

For the example here, our previous work reported in [51] is adapted. Governing equation is to be solved in for MWCNT is as follows:

$$\kappa_{axial}\frac{\partial^2 T}{\partial z^2}+\kappa_{radial}\frac{1}{r}\left\{r\frac{\partial^2 T}{\partial r^2}+\frac{\partial T}{\partial r}\right\}+p=0\,. \tag{2.30}$$

Here thermal conductivity in axial direction is expressed as κ_{axial} =1800 $Wm^{-1}K^{-1}$ and in radial direction as, κ_{radial} =0.05 $Wm^{-1}K^{-1}$. Joule heat generation term (p) is V^2/R per unit volume. Eq. (2.30) gives steady state solution for temperature inside the cross-section and along length (z-axis) of MWCNT interconnects. As boundary condition for MWCNT, outer CNT shell is in thermal equilibrium with the dielectric. In addition, two ends of interconnects are also in thermal equilibrium with the ambient chip temperature.

2.4. Electrothermal Coupled Equations

Since resistance and temperature are interdependent one has to solve coupled electrothermal transport equations iteratively until convergence is achieved either for the resistance or for the temperature. Chip ambient temperature is used as an initial temperature, which is 350 K. Using Eq. (2.23), effective MFP for a MWCNT can be calculated. From Eq. (2.4) overall resistance can be estimated once one has obtained the MFP. From resistance, one can calculate the Joule heating term $p= V^2/R$ for a fixed voltage across interconnects. After calculating the Joule heating (p) term, it is used in the governing equation with the boundary conditions to obtain a temperature profile in (r, z) coordinate system using the finite element method (FEM). The obtained temperature is then used for the resistance calculation.

The updated average temperature is then used as the initial temperature for the next cycle of iteration. This way, iteratively we can solve for the temperature until we get an error less than 1 K or the temperature reaches to a breakdown temperature, 873 K. Tolerance is considered as1K,

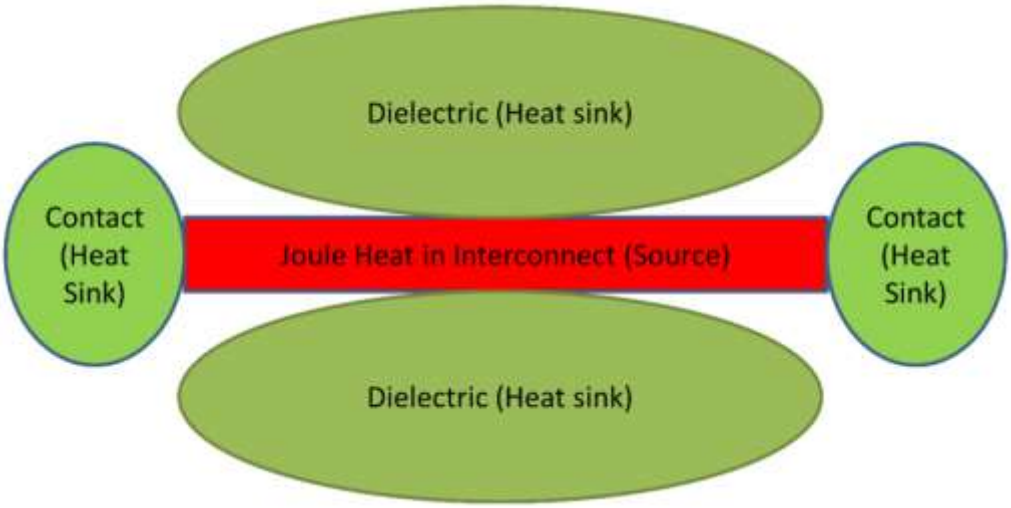

Figure 2.6: Heat source and sinks in VLSI interconnect.

to be a good tolerance in comparison to a high breakdown temperature. To compare new and old temperature profiles, we actually took an average of outermost and innermost shell temperatures. From the observation, we found that the innermost shell always has a higher temperature than the outermost shell. Hence in deciding about breaking point, only the innermost shell temperature to reach the 873 K. The iterative scheme is shown in Fig. 2.7.

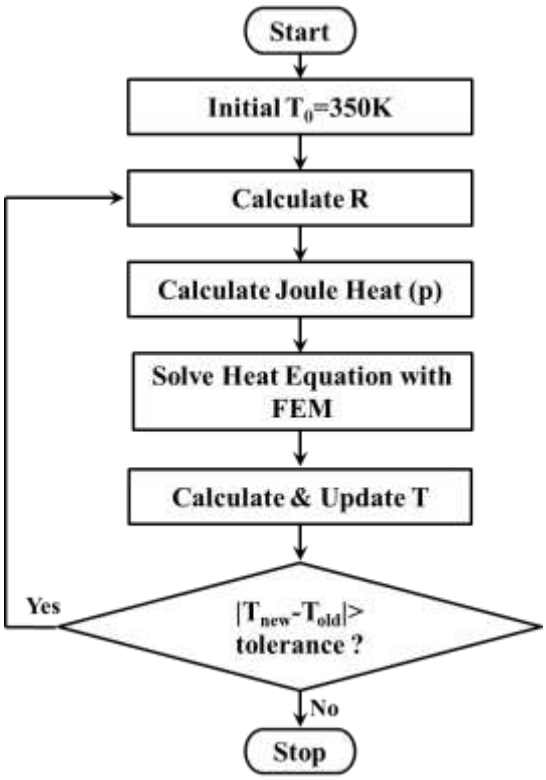

Figure 2.7: Iterative solution to electrothermal coupled equations.

2.5. Temperature Profile Inside the Interconnect

In SWCNT, temperature profiling is one-dimensional showing temperature variation only in the direction of length of the CNT. It has been experimentally verified that the hot spot is at the center of the CNT and Joule heating induced breaking occurs at the center of CNT. In Fig. 2.8 an example of SWCNT temperature distribution is presented. From Fig. 2.8, it is seen that the maximum temperature depends on the biasing voltage and is peaked at the center. SWCNT wire of 1 nm diameter will survive any voltage below 4 V. In Fig. 2.8, 0.1V line is superimposed with 0.5V line. Above 4 V, probability of melting down from the center is high and thermal breakdown resistance become infinite. Earlier resistances up to breakdown is shown in Fig. 2.5.

In Fig. 2.9, cross-sectional temperature profile of a SWCNT bundle based interconnect has been shown from our previously reported work [73]. The central CNTs have mostly high temperature and center most shell achieves the maximum temperature. Therefore, if any break down occurs it will occur from the center of the central CNT shell. In Table 2.2, equivalent resistance is presented for various geometry.

Table 2.2: Temperatures and equivalent resistances of SWCNT bundle interconnect

Bias current (mA)	Width=Height (nm) D=1nm unless mentioned	Number of SWCNTs	Current Density (1×10^{10} A/cm^2)	Highest Temperature (K)	Equivalent Resistance (KΩ)	Comments on Break down
10	5	14	4.0	360	26.8	No
	10	52	1.0	303	7	No
23	5	14	9.2	820	27	Critical

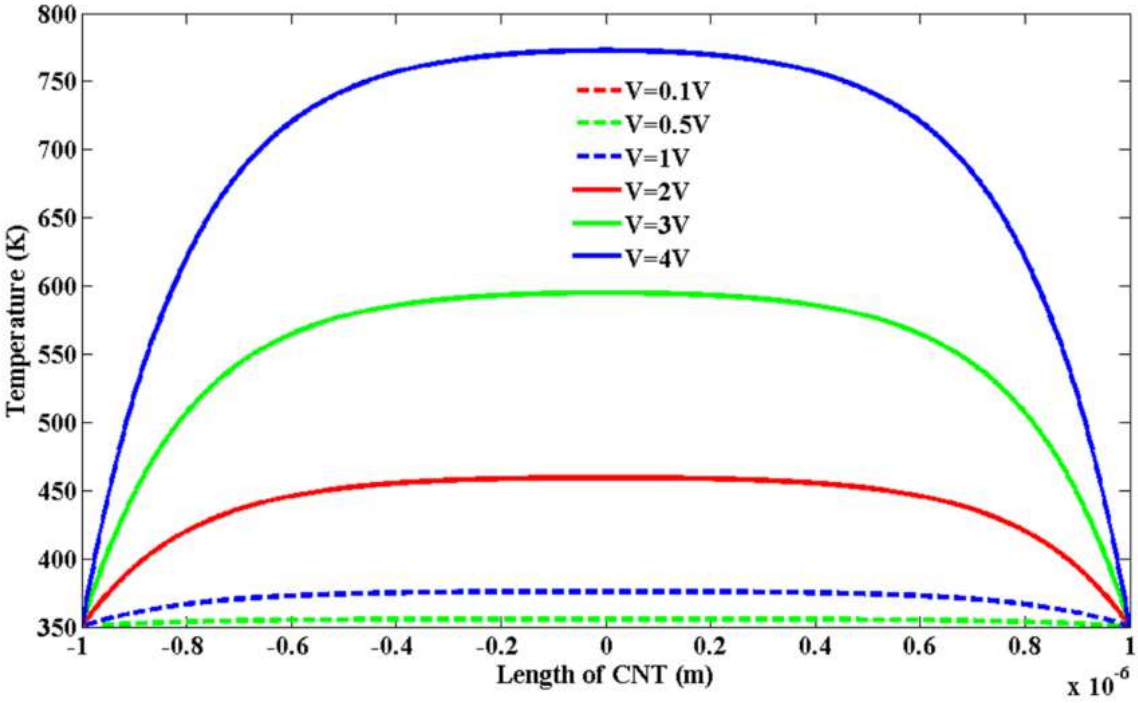

Figure 2.8: Temperature profile of SWCNT interconnects.

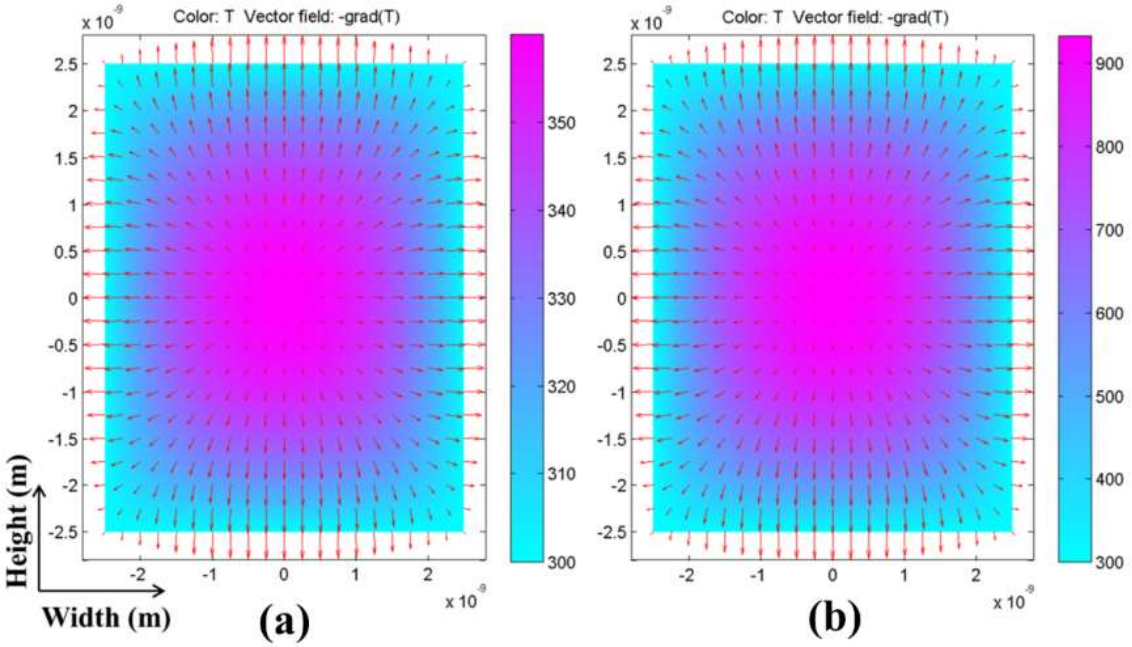

Figure 2.9: Cross sectional temperature distributions (color) and heat flow vector (arrow) for 10 mA current bias (a) D =1nm, L=1μm, (b) D =4 nm, L=1 μm. In case of (b) central shell temperature is above melting point (873K), therefore breakdown will occur.

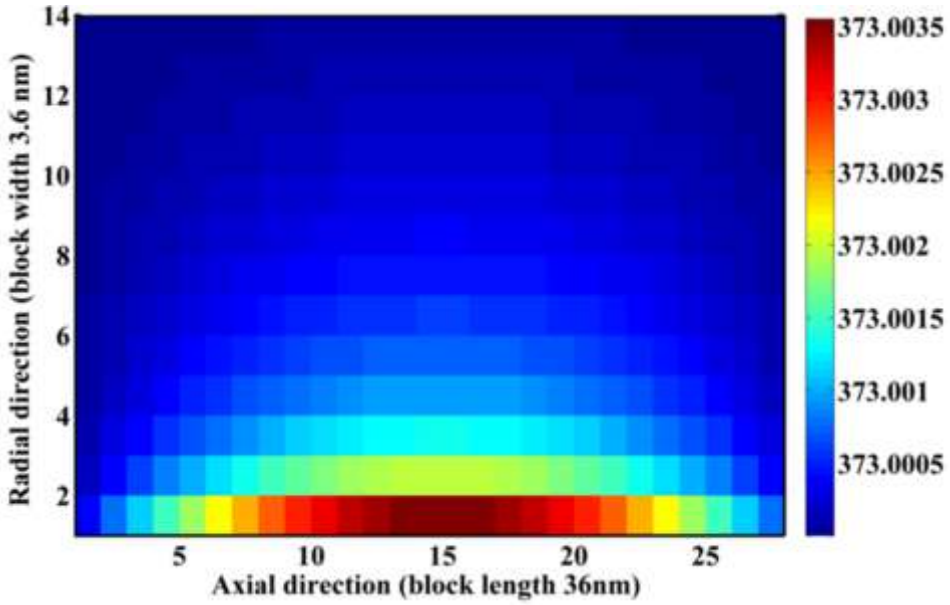

Figure 2.10: Temperature profile of MWCNT interconnect cross section.

For MWCNT the temperature distribution has been calculated in our earlier work reported in [51] and shown in Fig. 2.10. It has been found that MWCNT is inherently thermally more stable than any other kind of CNT interconnects. Most theoretical models assume that one third of the MWCNT shells are metallic and the rest of them are semiconducting which is statically sound. On the other hand, in real measurement this statistical assumption will not work. In real measurement, one could obtain different numbers of metallic shells than the theoretical assumption. This is why total resistance can vary from experiment to experiment.

2.6. Effect of Interlayer Dielectric

In this section, porous silica xerogel film as a low-k (ε_r~2.0) interlayer dielectric around the MWCNT based interconnect is considered for thermal calculations [74, 75]. With a two-dimensional thermal equation with a single conductor transmission line model [42], the impact of Joule heating phenomenon on the performance of MWCNT-based interconnects is examined. The anisotropic thermal conductivity of the MWCNT has been used to solve a two-dimensional heat equation with the finite element method (FEM) to obtain temperature distribution and hot spots. We have studied thermal breakdown conditions and electrical performance for different geometries.

2.6.1. Assumption and Boundary Conditions

An MWCNT with a uniform cross section is considered in this work. It is assumed that the heat generation is uniform everywhere inside the MWCNT. It is also assumed that the two ends of an interconnect will be in thermal equilibrium with the surrounding temperature (T_0). This assumption gives boundary conditions shown in Eq. (2.31). Again, ILD thickness is taken as 500

nm to dissipate heat up to the chip ambient temperature. Chip ambient temperature is taken as 350 K. Circumferential flow of heat is not considered because of the circular symmetry. Hence the real three-dimensional problem can be reduced to a two-dimensional problem as shown in Eq. (2.32). Unlike a one-dimensional SWCNT conductor, an MWCNT has more ways of dissipating heat and can reach to the steady state. The boundary conditions for the steady state solution is as follows:

$$T_{mwcnt}(r,z)|_{z=L} = T_{mwcnt}(r,z)|_{z=0} = T_0, \qquad T_{ILD}(r,z)|_{r=r_0+t_{ILD}} = T_0. \tag{2.31}$$

In Eq. (2.31), (*r, z*) are the co-ordinates in the cylindrical coordinate system towards radius and length, respectively. *L* is the total length of an MWCNT. In this study *L*= 1, 2 and 5 μm, r_o is the outer radius of the MWCNT which depends on the technology nodes. Here MWCNTs with outer diameters from 10 nm to 50 nm at T_0=350 K are studied and compared.

2.6.2. Governing Equation

We have used Fourier law of heat conduction as the governing equation to study the thermal transport. In this work, ILD heating along with the MWCNT interconnect is included. Therefore, two separate governing equations are required to study thermal behavior. In following equations, first one is for the MWCNT and the second one is for the ILD.

$$\kappa_{axial}(T)\frac{\partial^2 T}{\partial^2 z} + \kappa_{radial}(T)\frac{1}{r}\left(r\frac{\partial^2 T}{\partial^2 r} + \frac{\partial T}{\partial r}\right) + p - g(T - T') = 0 \tag{2.32}$$

$$\kappa_{ILD}\left(\frac{\partial^2 T}{\partial^2 z} + \frac{1}{r}\left\{r\frac{\partial^2 T}{\partial^2 r} + \frac{\partial T}{\partial r}\right\}\right) = 0 \tag{2.33}$$

Here *p* is the heat generation term (= V^2/R) per unit volume. Because of steady state solution, right-

hand side of this governing equation is necessarily zero. Another way heat can be generated is due to switching activity [76] which contributes to heating in a power dissipation network with multiple nodes. Particularly for a single resistive wire where only two contact nodes are associated, heat generated by the switching activity (IV) and heat generated from the Joule heating (V^2/R) essentially estimate the same amount of heat. Besides the heat generation term, substrate heat loss term, g is also included. Substrate heat term (g) accounts for the heat loss to the substrate from per unit length of the MWCNT and is equivalent to thermal interface resistance (TIR). TIR depends on MWCNT-substrate interface and diameter of the outer shell of MWCNT. Substrate heat term (g) is extracted from the molecular dynamics simulation reported in [77], and it is $0.065D$ $Wm^{-1}K^{-1}$ where D is the outer shell diameter, and $T - T'$ is the temperature difference at the interface. Since exact data for TIR in case of CNT-porous silica xerogel is not available, it's value is extracted from CNT-silica data reported in [77] with the assumption that CNT-porous silica will be more resistive and TIR is proportional to the thermal conductivity. The volumetric heat generation term p is significantly higher than the heat loss term g which makes $(p-g)$ less sensitive to the variation of g due to inaccurate value of g. In Eq. (2.33), heat generation term is not included as it is assumed that unlike the MWCNT there is no active Joule heating inside the ILD. Here, κ_{ILD} is isotropic thermal conductivity of xerogel taken as 0.12 $Wm^{-1}K^{-1}$ [74]. The thermal conductivity of a MWCNT in axial direction is taken from [67] and radial direction as 0.05 $Wm^{-1}K^{-1}$ [70].

In Fig. 2.11, temperature variation at different bias voltages has been plotted for a 1 μm long MWCNT. In each plot of the Fig. 2.11, biasing voltage is shown. In (a), (b) and (c) biasing voltages are less than the breakdown voltage, while in (d) it is above the breakdown voltage. The color bar is shown with the temperature in Kelvin scale. In each plot of (a), (b) and (c), the

temperature reaches below the breaking point, 873 K. If any of the MWCNT shells reaches to 873 K temperature, it is noted as the breakdown. From Fig. 2.11, it is apparent that only the innermost shell reaches the highest temperature at any given bias and at any geometrical configuration. This computation suggests that the temperature gradient exists in both the radial and axial direction in accordance with the measurement in the work of Costa et al. [78]. Since thermal conductivity in the axial direction is 4 to 5 orders larger than the radial direction, the temperature gradient in the radial direction is not noticeable in Fig. 2.11. Most of the heat energy is trapped inside the MWCNT. Outer areas can dissipate heat through the ILD whereas the innermost shell cannot dissipate that quickly because of 0.05 $Wm^{-1}K^{-1}$ radial thermal conductivity of the MWCNT. Although heat conduction is treated in two-dimension, electrical conduction is taken only in one direction because voltage bias is along the axial direction only. On top of the voltage biasing, interconnect is buried in the electrical insulator around the radial direction to block any electrical current towards that direction. Electrical leakage current in the radial direction is not considered here for this reason.

Fig. 2.12 shows the temperature distribution along the MWCNT length. MWCNT of D_{out}=50 nm, D_{in}=10 nm and length of 1μm is considered here. In Fig. 2.12, a marker with a red circle is for 10 V, a dark red star is for 15 V and the blue diamond is for 20 V. All these three markers show the normal operating condition. Normal condition means biasing voltages are less than the breakdown voltage. Here, 873 K is the breakdown temperature which is shown in this figure with a red dash line. Center of the MWCNT reaches to a maximum temperature. Hence, if any breakdown happens it will be at the center of the MWCNT. For the longer interconnect, the temperature profile is flat in the middle whereas for the 1 μm long it is parabolic. In a longer

MWCNT, the temperature gradient is zero at the middle of the temperature profile. Therefore, not much heat will flow in the axial direction toward contacts. Hence, most of the heat for the longer MWCNT (>1 μm) will be dissipated through the ILD, whereas for the shorter MWCNT it will be towards the contacts. For comparatively longer MWCNT as in global and intermediate interconnects, more than 60% of the length shows a constant temperature. Only near the contact, the temperature gradient is observable. At the breakdown condition, while the innermost shell temperature reaches to 873 K, the outermost shell is still below the breaking point temperature. Therefore, at breakdown there will still be conducting shells [79]. Huang et al. [79] found that the breaking of MWCNTs starts "unambiguously" from the outer shell in one of their three observations. In other observations, they found that breakdown starts from the innermost shell.

From the calculation of the temperature profile, as shown in Figs. 2.11 and 2.12, breakdown should always start from the inner shell and not from the outermost shell for all contacted shells. One can argue why Huang et al. [79] observed breakdown starting from the outer shell. It could be triggered by prevailing impurities or vacancies in the outer shell, which act as the scattering center and creates a hot spot. The outer most shell is more prone to defects than the inner shells due to processing. Another possibility is that the heat conduction with the nonaligned tubes is from tube to tube where only outer shells are connected to the contact to carry heat and charge carriers.

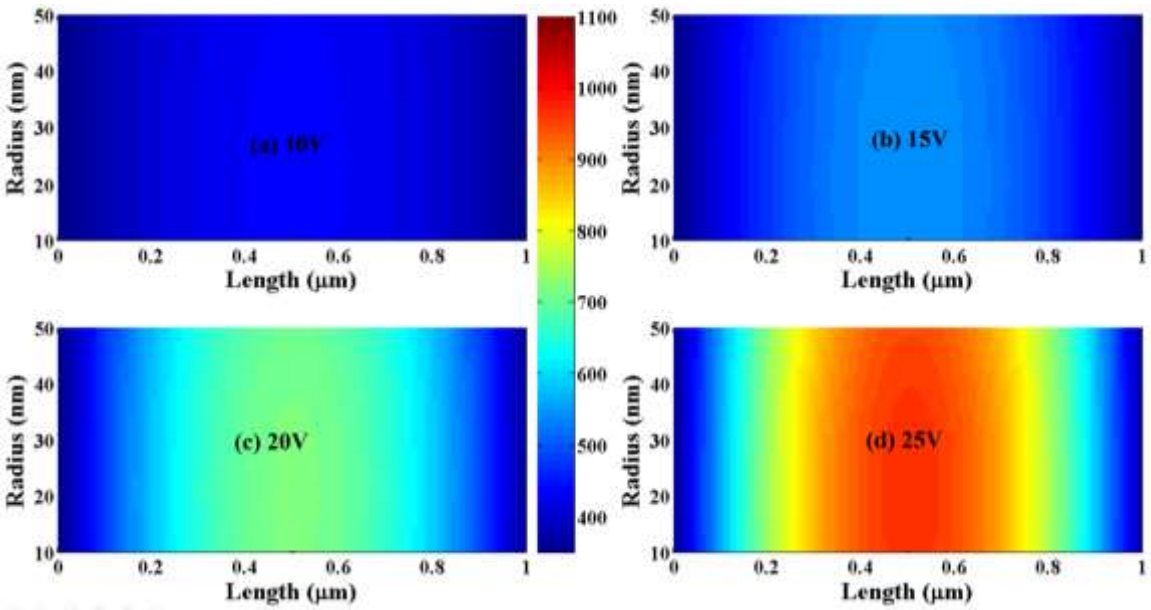

Figure 2.11: Spatial variation of the temperature inside a MWCNT with D_{out}=50 nm and D_{in}=10 nm. Note: Length is 1μm in these subfigures.

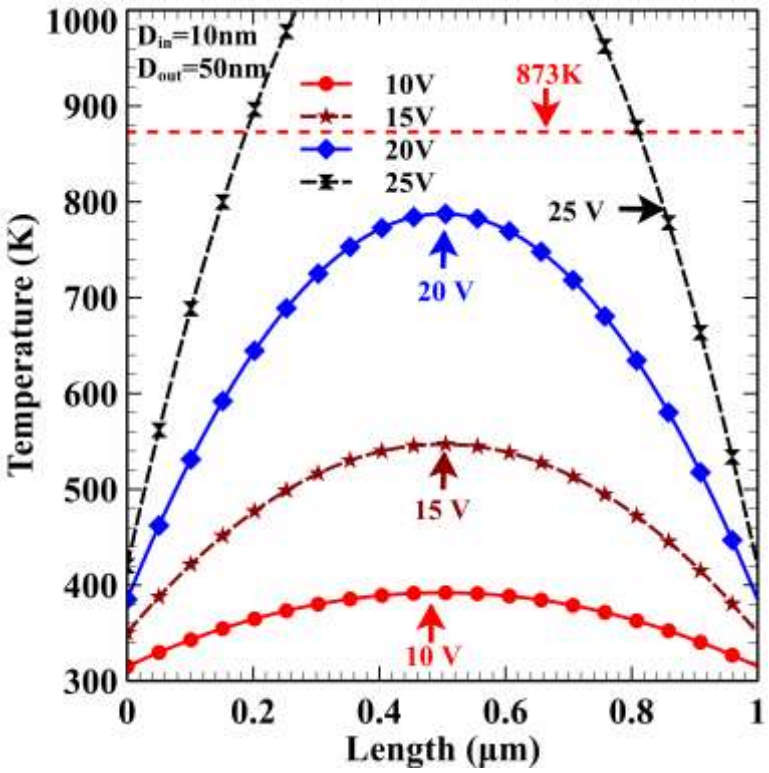

Figure 2.12: Temperature distribution over the length of a MWCNT for different biasing voltages.

Therefore Joule heat dissipates in outermost shell and flows inwardly. Moreover, after the breakdown of outermost shell, they observed that breakdown continues from the innermost shell. For shells with good contacts, the breakdown should initiate from the center of the innermost shell and continue to the second innermost shell and so on. Due to anisotropic heat conductivity [70] comparatively, inner shells will reach the breaking point before the outer shells. Nevertheless, reproducibility of this kind of experiments is always challenging due to lack of control of chirality, alignment and the contact. For the modeling purpose, we did not consider these conditions due to process variability in fabrication and for simplicity in computation. Regardless of the breakdown sequence, this is certain that the breakdown of any shell causes some extra resistance due to loss of some parallel transport channels. Eventually, this will cause the temperature to go high at a fixed current bias.

In Fig. 2.13, the highest temperatures in an MWCNT at different bias voltages is shown which could not be covered in Figs. 2.11 and 2.12. In Fig. 2.13, the outer and inner diameters are 50 nm and 10 nm, respectively. All points below 873 K line corresponds to a normal condition where breakdown will not occur. If the peak temperature crosses this 873 K line breakdown will occur.

In Fig. 2.14, breakdown voltages for an MWCNT of different lengths are presented. Outer diameter is 50 nm while inner diameter is varied. Inner diameters 40 nm, 30 nm, 20 nm and 10 nm are corresponding to 16, 31, 46 and 60 shells, respectively. For a particular outer diameter, inner diameter is varied to see which geometry can withstand a higher breakdown voltage. MWCNTs with more shells withstand a higher voltage bias than an MWCNT with fewer shells. For example, in Fig. 2.14, the one with 60 shells shows highest breakdown voltage of 45 V for a

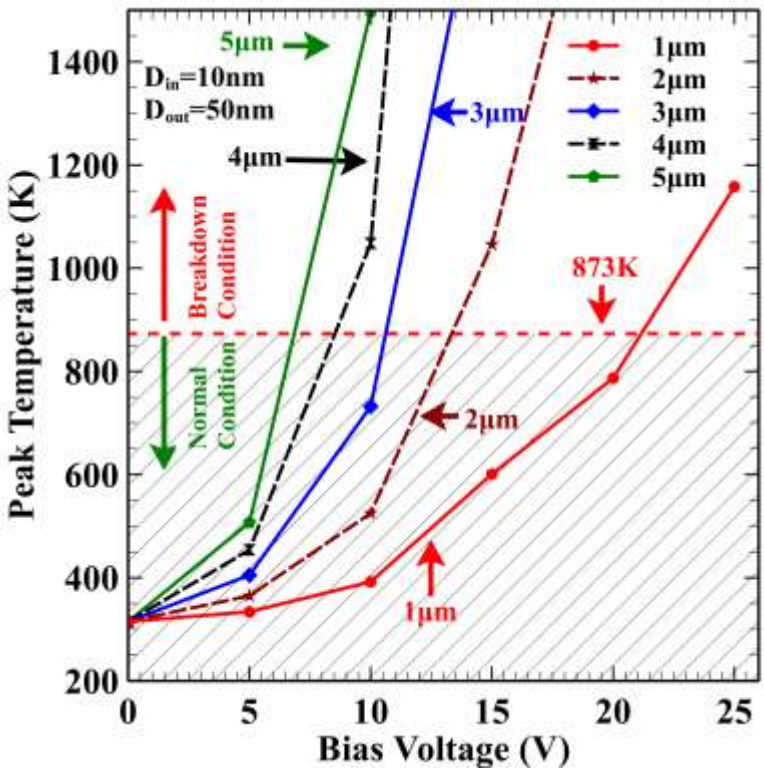

Figure 2.13: Peak temperature at different biasing voltages for 1 to 5 µm long MWCNTs.

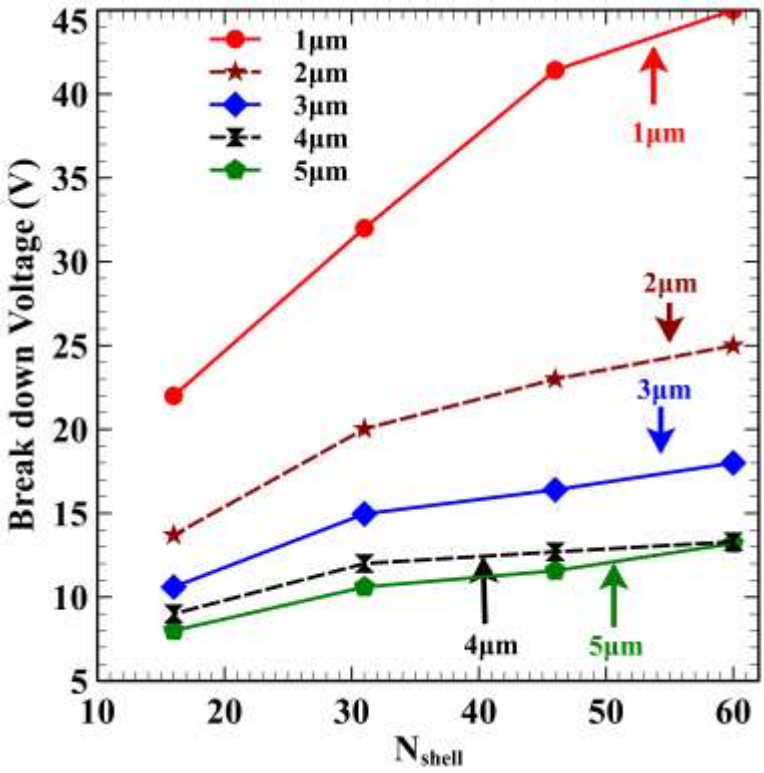

Figure 2.14: Breakdown voltages for 1 to 5 µm long MWCNTs of different number of shells.

1μm long interconnect. At the same time, a longer MWCNT which has to dissipate heat mostly in the radial direction cannot withstand higher voltages because of low thermal conductivity in the radial direction.

In Fig. 2.15, breakdown condition current density is presented. From this figure, we observed that comparatively, MWCNTs with fewer shells have slightly higher breakdown current density. Interestingly it is found that almost for all geometric configurations, breakdown current density is in the order of 10^8 Acm^{-2}. For an MWCNT with more number of shells, current density slightly decreases with the length. For comparison, breakdown power varies from 5.3 mW (1 μm long 7 nm outer diameter) to 33 mW (5 μm long 14 nm outer diameter) which supports having $1.234x10^8$ Acm^{-2} non-breakdown condition current in Li et al.'s work [80]. In a recent experiment, breakdown and Joule heating dynamics have been studied for an MWCNT filled with low vapor pressure material [78]. For an outer diameter of 120 nm, shell degradation occurred when current density was measured as $0.8x10^6$ Acm^{-2} which is of the same order as shown in Fig. 2.15.

In Fig. 2.16, intrinsic resistance versus bias current has been presented. The length is varied from 1 μm to 5 μm while the outer shell diameter is 50 nm and inner shell diameter is 10 nm. It is apparent that as the current bias increases, resistance increases nonlinearly. Once current through the interconnect reaches to the breaking point calculation for resistance is stopped. However, it is apparent that the thermal runway will increase the resistance until breakdown occurs. MWCNTs with high outer diameters show lesser resistance due to larger MFPs and more transport channels due to a large diameter [50]. Resistance in each line shows up to the breaking point. Above the breakdown point, resistance is infinite. Longer MWCNTs show higher resistance in per unit length because of the increased scattering.

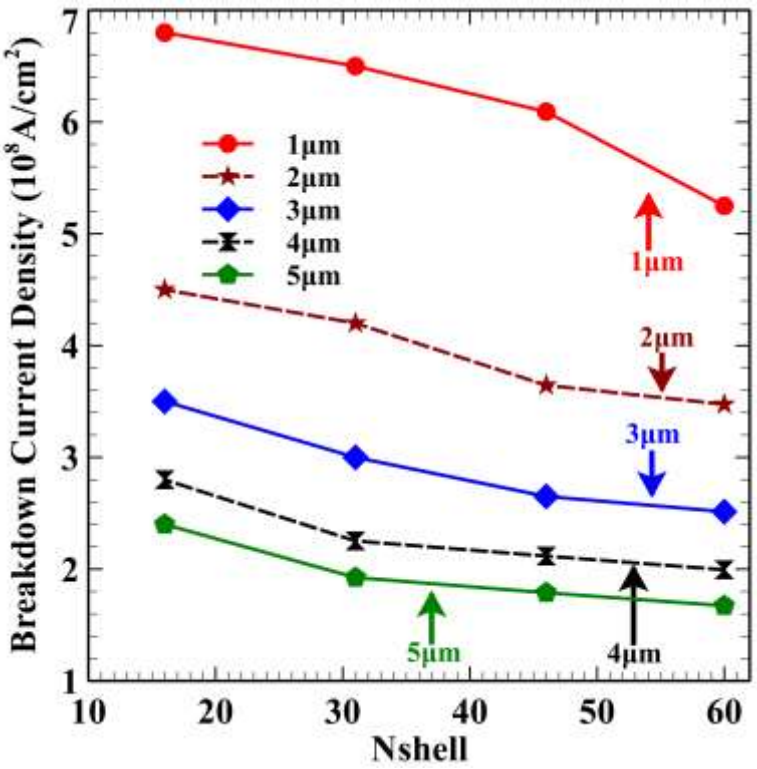

Figure 2.15: Breakdown current for 1 to 5 µm long MWCNTs of different number of shells.

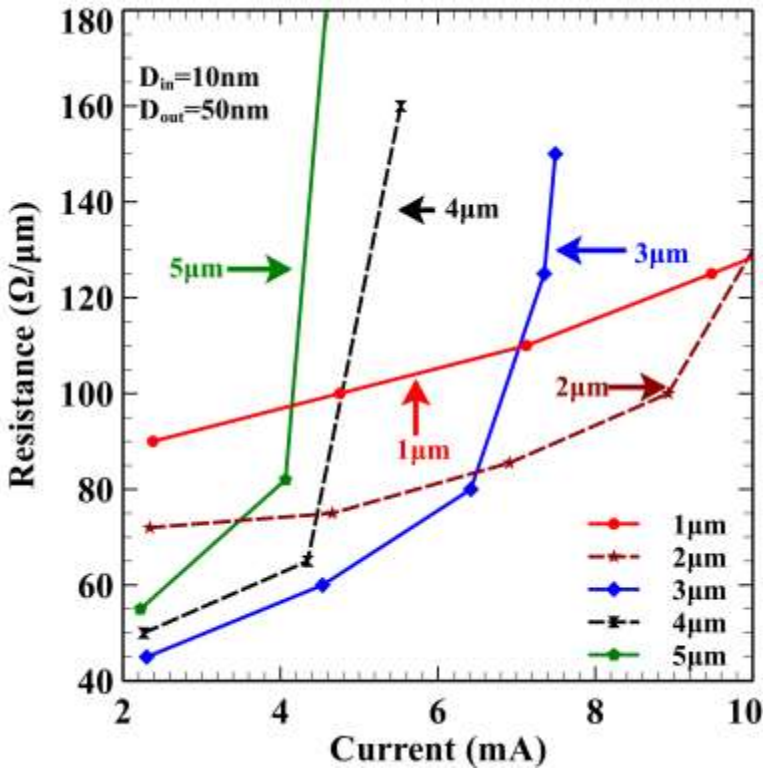

Figure 2.16: Resistance of 1 to 5 μm long MWCNTs of different lengths.

An MWCNT interconnect can be of any outer diameter up to 100 nm. However, each MWCNT with a fixed outer diameter can have many shells and many possible values for the inner diameter. To compare, we also have simulated geometries reported in other works [27, 80, 81].

For a 2 μm long MWCNT with a 10 nm outer diameter and a 3.88 nm inner diameter, the obtained resistance is 1.55 kΩ/μm and current density 5.9×10^7 Acm^{-2}. The actual highest limit of 1×10^9 Acm^{-2} for SWCNTs was obtained by Yao et al. [82]. The difference between our results and experimental results is due to mismatch of contact resistance and interlayer dielectric thickness which was not reported in those works. It is also assumed that one-third of the MWCNT shells are metallic and rest of them are semiconducting. Hence, total resistance can vary from experiment to experiment. In some of the previously mentioned experimental reports [80], the contact resistance was not explicitly mentioned, which limits this work for exact comparison. In Table 2.3, comparison of our results with previously reported work of Nihei et al. [81] and Li et al. [80] is shown.

Table 2.3: Comparison with earlier works

Ref.	L (μm)	D_{in} (nm)	D_{out} (nm)	R (kΩ/μm)	This work (kΩ/μm)
Nihei et al.[81]	2	3.88	10	1.60	
Srivastava and Yao [27]	2	3.88	10	1.90	1.55*
Mohsin et al. [51]	2	3.88	10	2.257	
Li et al., [80]	25	50	100	0.035	
Srivastava and Yao [27]	25	50	100	0.042	0.033**
Mohsin et al. [51]	25	50	100	0.02781	

*Computed at 50mV bias and **0.25V bias to compare with earlier works.

To summarize, electrical and thermal equations have been coupled and solved iteratively using the FEM to obtain temperature profile inside the MWCNT to study the breakdown condition of MWCNT interconnect at several biasing voltages and for different geometries. For resistance modeling, Landauer-Büttiker formalism is used and for the temperature, Fourier heat equation in the cylindrical coordinate system is considered. In heat calculation, anisotropic thermal conductivity of MWCNT is taken into account. An interlayer dielectric is also considered in heat equation. Considering anisotropic heat diffusion in a two-dimension allowed to model temperature distribution more accurately and a better estimation of breakdown voltages. We found that the longer interconnects withstand higher voltage biases than the shorter interconnects in the case of thick MWCNTs. Also, interconnect with larger diameters show a better thermal behavior. The resistance that is intertwined with the temperature highly depends on the bias current. In the low current limit, resistance is linear with the current but in high bias current, it is nonlinear. The linearity of resistance with the bias current improves for interconnects with the increase in diameter.

2.7. High Frequency Performances in terms of S-Parameters

Based on performance, different CNT based interconnects can be compared. Most importantly, resistance, inductance and capacitance of interconnect and high frequency response can be taken as performance parameters. Other performance matrices can be derived based on these basic parameters. The interconnect can be modeled as a two-port network as described in Section 2.2.5. Two ports network S_{11} and S_{21} parameters help understand the frequency response of an interconnect in terms of back scattering power and transmitted power. S_{11} is the ratio of

power reflected from the transmission line to the incident power while S_{21} is the ratio of power transmitted through the transmission line to the incident power.

$$S_{11} = 10\log\frac{P_{back}}{P_{incident}};\ S_{21} = 10\log\frac{P_{transmitted}}{P_{incident}} \tag{2.34}$$

For CNT interconnect, *S*-parameters calculations have been carried out with distributed elements and normalized by intrinsic impedance 50 Ω. Method described in [83] can be used for *S*-parameters calculation per unit values of resistances, inductances and capacitances described in Section 2.2. From Fig. 2.17, it is apparent that backscattering is high in high frequency range for SWCNT bundle and MWCNT based interconnects. In case of SWCNT, backscattering is low in high frequency range. SWCNT could be of a potential use in high frequency circuits. In MWCNT interconnect higher outer diameter suffers more backscattering than the lower one.

From Fig. 2.18, it can be concluded that in general power transmission is high at high frequencies in these three kinds of CNT based interconnects. Joule heating worsens the situation by reducing the transmission. Depending on application a particular type of interconnect material can be preferred over the other one. Fig. 2.19 is shows *S* parameters for 1μm, 2 μm and 5 μm long MWCNTs with D_{out}=10 nm and D_{in}=9 nm has been calculated considering the interlayer dielectric. For all these three lengths, S_{11} is less than 0.2 dB and for longest MWCNT it is minimum. Different bias voltages and Joule heating do not play significant role in S_{11}. However, S_{21} is sensitive to Joule heating induced scattering. For increased voltage, which increases Joule heating, induced scattering becomes worst. S_{12} parameters decrease for longer MWCNT. After 1 THz both of these *S* parameters start oscillating because at that frequency range the reactive

impedance dominates over the resistance. In Fig. 2.19, blue and green lines are normal operation and red line shows break down condition. Black line is for estimating temperature distribution if bias voltage exceeds breakdown voltage. As temperature increases with high biasing voltage, $|S_{21}|$ become worst. Beyond 1THz, $|S_{11}|$ and $|S_{21}|$ the value starts oscillating. Longer MWCNT suffers more scattering and $|S_{21}|$ become the worst.

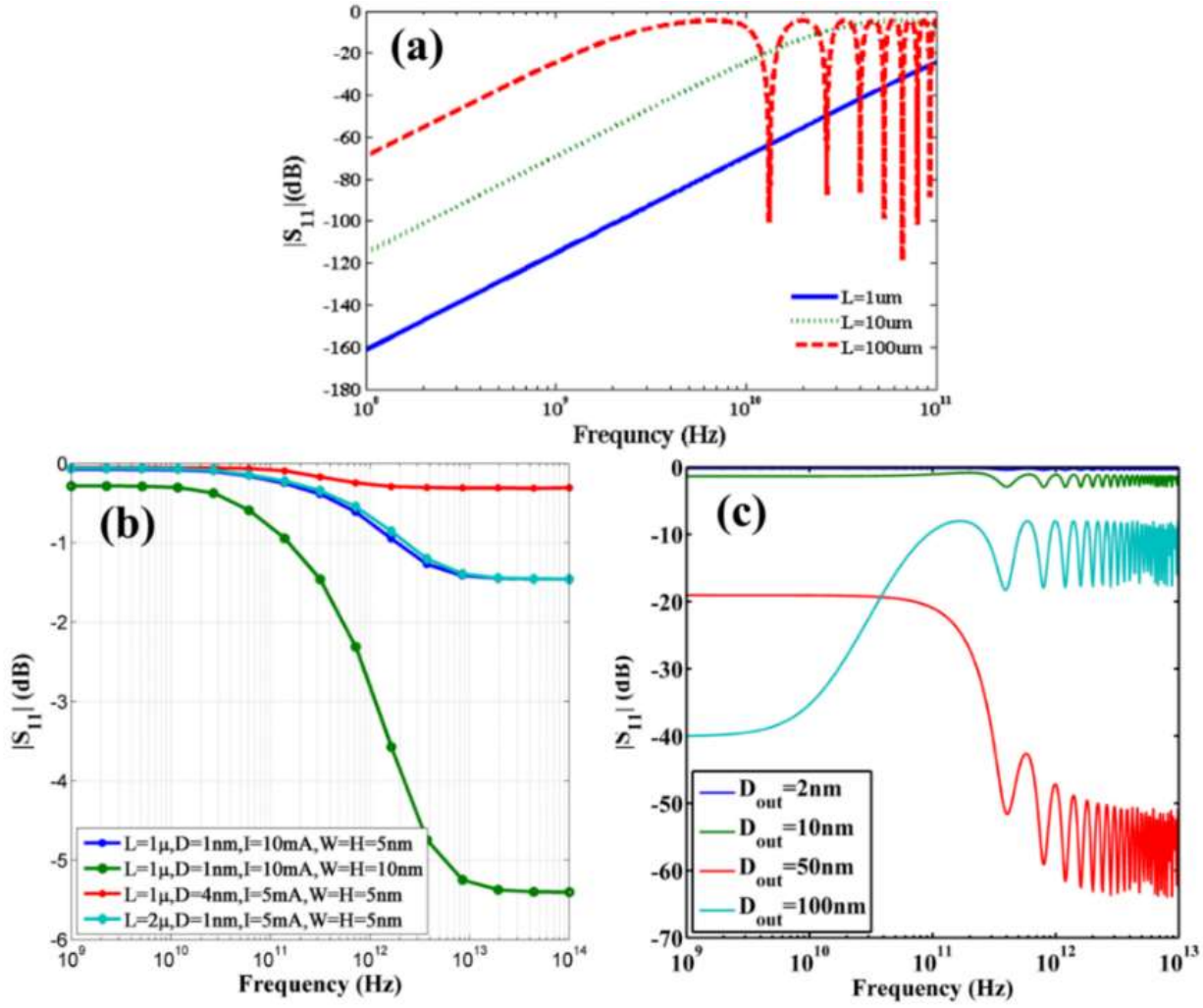

Figure 2.17: Scattering parameter S_{11} of various interconnects (a) SWCNT, (b) SWCNT bundle based and (c) MWCNT (without interlayer dielectric).

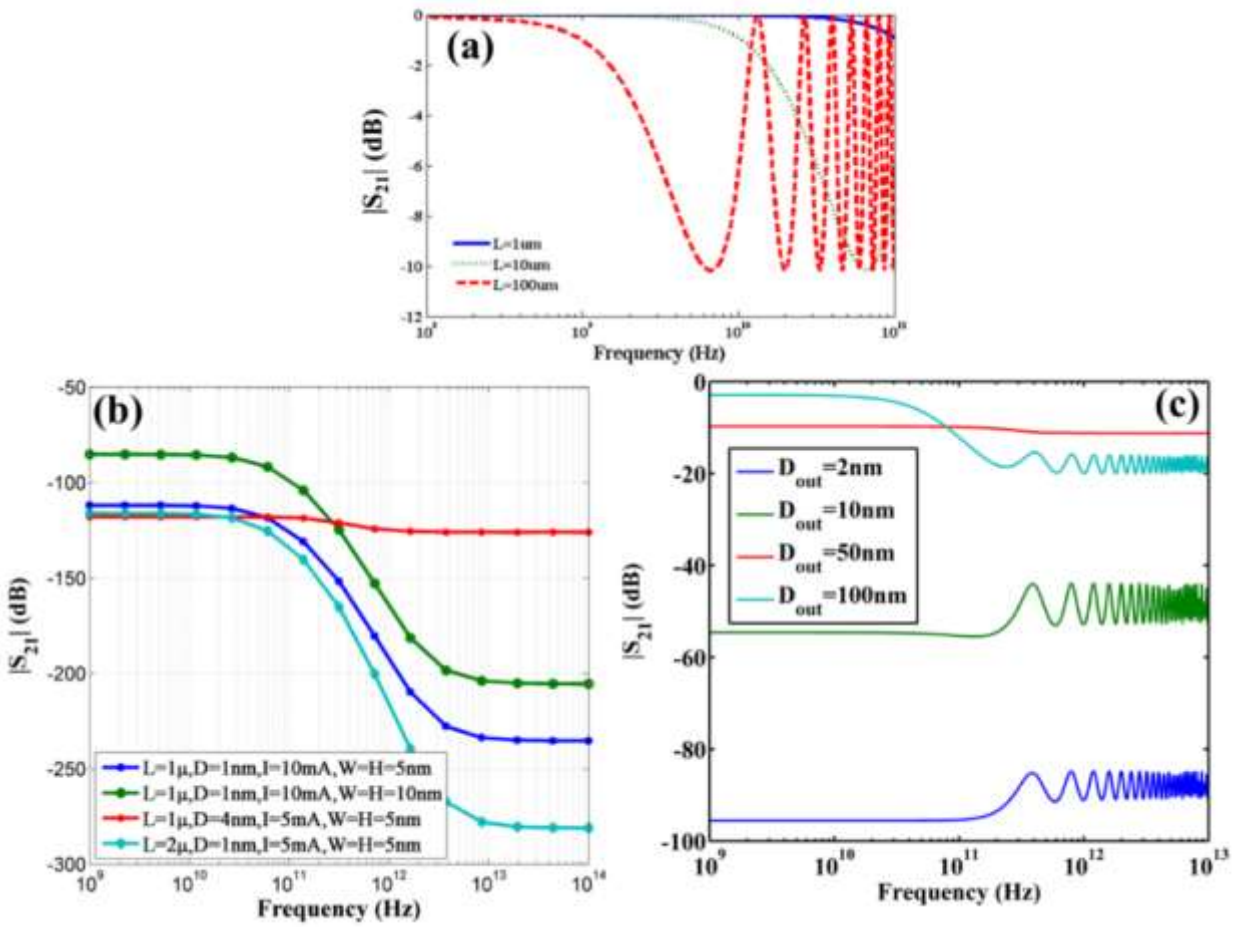

Figure 2.18: Scattering parameter S_{21} of various interconnects (a) SWCNT, (b) SWCNT bundle based and (c) MWCNT (without interlayer dielectric).

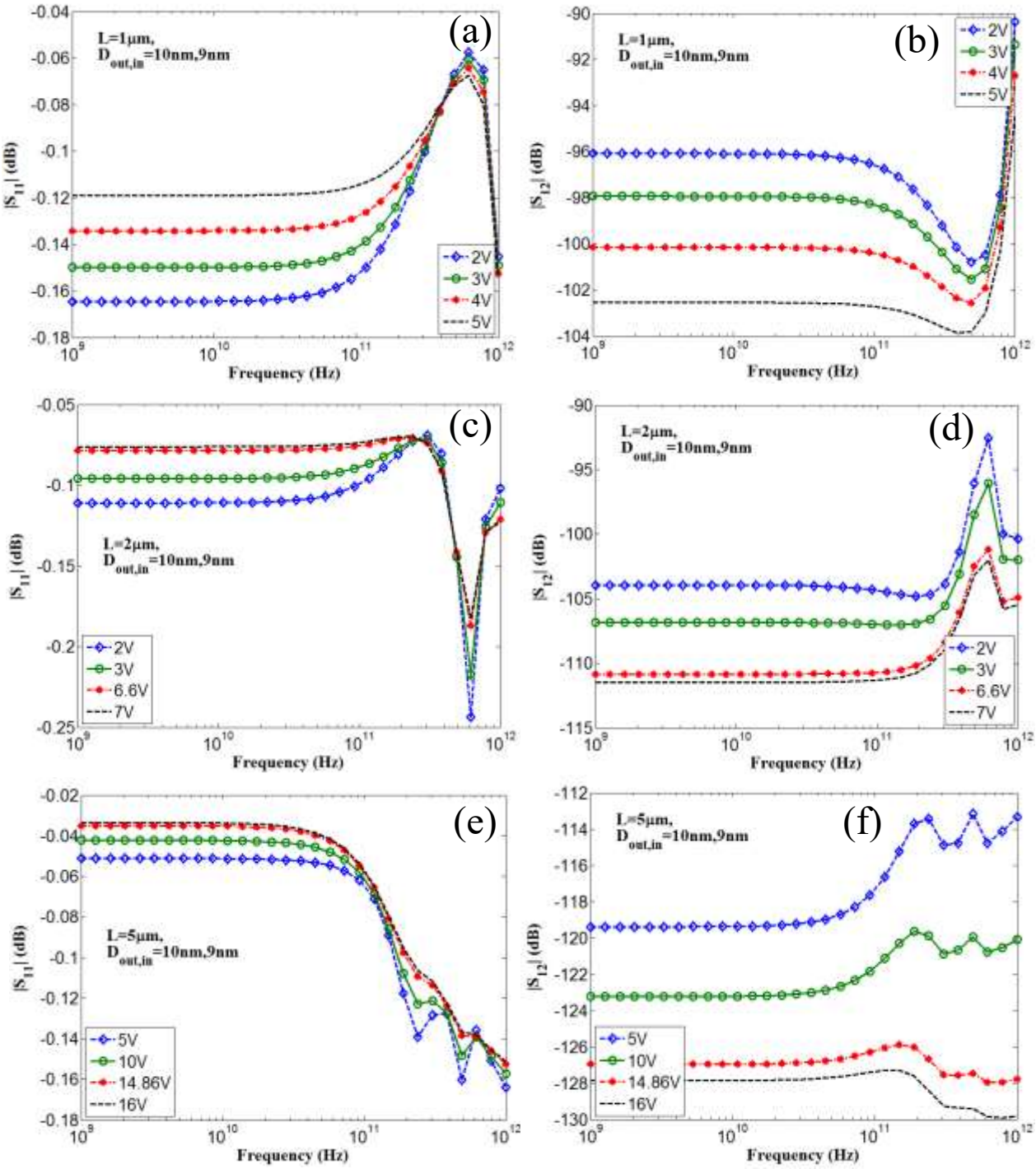

Figure 2.19: Scattering parameters $|S_{11}|$ and $|S_{21}|$ of MWCNT interconnect (modeled with interlayer dielectric effect) for different biasing voltages. MWCNT length in (a) and (b) is 1 μm, in (c) and (d) 2 μm. and in (e) and (f) 5μm. In each figure., D_{out}=10 nm, D_{in}=9 nm.

2.8. Conclusion

In this chapter, the study of various CNT based interconnects with Joule heating induced scatterings is presented. Electrical and thermal equations have been coupled and solved iteratively using the FEM to obtain temperature profile inside the CNTs to study the breakdown condition of interconnect at several biasing voltages and for different geometries. For resistance modeling, Landauer-Büttiker formalism is used and for the temperature, Fourier heat equation in the cylindrical coordinate system is considered. For the case of MWCNT, anisotropic thermal conductivity is taken into account. Among various CNTs MWCNT seems to be a better candidate for a VLSI interconnect. Hence, special attention is given to this variant of CNT and extended its model by including an interlayer dielectric. Considering anisotropic heat diffusion in a two-dimension allowed to model temperature distribution more accurately and a better estimation of breakdown voltages. It is found that the longer interconnects withstand higher voltage biases than the shorter interconnects in the case of thick MWCNTs. Also, interconnects with larger diameters show a better thermal behavior. The resistance that is intertwined with the temperature highly depends on the bias current. In the low current limit, resistance is linear with the current but in high bias current, it is nonlinear. The linearity of resistance with the bias current improves for interconnects with the increase in diameter. Transmission of power degrades with the high voltage bias due to increased scatterings for interconnect of the same geometry. On the other hand, backscattering is less sensitive to a bias voltage or Joule heating than the signal transmission.

The present study makes an attempt for the better understanding of thermal breakdown mechanism of MWCNT-based interconnects considering aligned non-defective shells. The work also assumes that all shells are conducting and make contact. As a future work, it is possible to

extend this work with second order corrections including missing shells and other non-ideal cases. However, this work would be useful to study electrothermal behavior of other emerging interconnects.

CHAPTER 3
MATERIAL SIMULATION WITH DENSITY FUNCTIONAL THEORY

3.1. Introduction

In this chapter, density functional theory (DFT) [84, 85] will be discussed in conjunction with simulating emerging materials, particularly their electronic structure and electronic properties. For any emerging electronic technology, it is very important to understand it's electronic and thermal properties. Beside experiments of materials growth and characterization it is also required to validate those experiments theoretically. Density functional theory has been widely used by the physicist, materials scientist and chemist as a method to understand a new materials' properties utilizing first principle approach. By principle, DFT is an exact method. However for the purpose of speeding up the calculations, approximation for electrons exchange function is commonly used within DFT.

More accurate *ab-initio* or first principle method is "wave function" based method which solves Schrödinger equation directly without any approximation. Unfortunately, "wave function" method is limited only to molecule consists of few tens of atoms. Even using modern supercomputing technology and massive parallel resources, it is quite impossible to simulate a large atomic cluster of few thousand atoms in the scale of few 10 nm. In most of the practical cases, technology nodes (~10 nm) which consists of few thousands of atoms is very expensive using "wave function" approach. In this chapter, a brief historical and theoretical background of

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* Portions of this research were conducted with high performance computing resources provided by Louisiana State University (http://www.hpc.lsu.edu). SuperMike-II and SMIC clusters were used in this work.

DFT are discussed followed by the discussion of the approach taken in this dissertation in simulating new materials.

3.2. History of DFT

DFT is a computational quantum mechanical modeling technique used in physics, chemistry and material science to investigate the electronic structure of materials in particular many body systems, atoms, molecules and condensed phases. Implementation of DFT is also extended to soft materials such as biological systems, liquids and amorphous materials. Recently, Electrical and mechanical engineering disciplines are using DFT increasingly for nanoscience and nano technological purposes.

In 1928, Hartree [86] introduced a procedure to calculate approximate wave functions and energies for atoms and ions, and this is called the Hartree function. In the same year, Thomas-Fermi [87] modeled multi-atoms system statistically, but that is not being used today because of inaccuracies. Later Fock and Slater [88], individually, proposed a self-consistent function (SCF) taking into account the Pauli principle [89], and the multi-electron wave function (Slater-determinant). This now is famous as Hartree-Fock (HF) method [84]. Around 1950, HF method became easier to apply because of approximate functional used to represent the electron-electron exchange correlation term. In 1964, Hohenberg and Kohn [85] published a paper, and thus made the foundation of the DFT which was known as HK theory then. In a material system with n electrons, there are $3n$ (x, y, z components) variables in electrons wave functions that need to be solved which is very complicated by HF method. However, using HK theory only 3 variables are required as it uses functional method.

Since HK theory is the basis of the present day DFT theory it is instructive to state the basic tends of the HK theory. The HK theory is summarized in two statements as follows:

1. Ground state energy of a material depends on the electron density distribution.
2. Ground state energy can be obtained by minimizing the total energy.

Therefore, HK theory becomes a minimization problem where one has to minimize electrons density functional to obtain minimum total energy of the system. In 1965, Kohn and Sham (KS) [90] simplified HK theory and made it applicable to multi electron system which is called as KS-DFT. Since there were no rigorous ways to solve KS-DFT, approximations were required. Series of developments went into finding different approximation techniques. The first and the simplest approximation is the Local-Density Approximation (LDA) [84] which by 1970 became popular and received popularity among solid state physics community. By 1990 more accurate approximations found their way into DFT which attracted quantum chemistry community who were skeptical about the accuracy of DFT from the inception. Now DFT is well accepted not only among academic researchers but also for the industrial research and development. It is now routinely used for investigating new materials and for validating experiments or to complement experimental results as a state of the art theory. In 1998, Nobel prize authority recognized this discovery of DFT by awarding Walter Kohn [90] which is the most prestigious prize in chemistry.

Still DFT lacks in modeling highly correlated systems and fails to explain superconductivity in several material systems. However, ongoing efforts are being made by the computational condensed matter physicist community to make it ever better.

3.3. DFT as a Theory

3.3.1. Schrödinger's Equation

In theory of solids the first goal of the most approaches is to find a solution of the time-independent, non-relativistic Schrödinger equation. For simplicity, all equations in this chapter are normalized with electron mass and charge.

$$\widehat{H}\psi_i = E_i\psi_i \tag{3.1}$$

$\widehat{H}$ is the Hamiltonian for a system consisting of M nuclei and N electrons. In operator notation Hamiltonian is as follows,

$$\widehat{H} = -\frac{1}{2}\sum_{i=1}^{N}\nabla_i^2 - \frac{1}{2}\sum_{A=1}^{M}\frac{1}{M_A}\nabla_A^2 - \sum_{i=1}^{N}\sum_{A=1}^{M}\frac{Z_A}{r_{iA}} + \sum_{i=1}^{N}\sum_{j>i}^{N}\frac{1}{r_{ij}} + \sum_{A=1}^{M}\sum_{B>A}^{M}\frac{Z_A Z_B}{R_{AB}} \tag{3.2}$$

Here, A and B are the indices for nuclei while i and j denote electrons in the system. The first term in Eq. (3.2) is the kinetic energy operator for electron and can be noted as follows,

$$\widehat{T_e} = -\frac{1}{2}\sum_{i=1}^{N}\nabla_i^2 \tag{3.3}$$

The second term in Eq. (3.2) is kinetic energy operator for nuclei.

$$\widehat{T_{nu}} = -\frac{1}{2}\sum_{A=1}^{M}\frac{1}{M_A}\nabla_A^2 \tag{3.4}$$

Here M_A denotes mass of the particular nuclei. The third term in Eq. (3.2) is attractive electrostatic energy in between electrons and nuclei.

$$\widehat{V_{e-nu}} = -\sum_{i=1}^{N}\sum_{A=1}^{M}\frac{Z_A}{r_{iA}} \tag{3.5}$$

In Eq. (3.5), Z_A is the atomic number and r_{iA} is the distance between the atomic center of A^{th} atom and i^{th} electrons orbit. The fourth term accounts for electron-electron repulsive energy. Considering all the electron-electron pairs, the total electrostatic repulsive energy can be obtained from Eq. (3.6).

$$\widehat{V_{e-e}} = +\sum_{i=1}^{N}\sum_{j>i}^{N}\frac{1}{r_{ij}} \tag{3.6}$$

The fifth term of Eq. (3.2) is the total electrostatic repulsive energy of all the nuclei pairs.

$$\widehat{V_{nu-nu}} = +\sum_{A=1}^{M}\sum_{B>A}^{M}\frac{Z_A Z_B}{R_{AB}} \tag{3.7}$$

In Eq. (3.7), Z stands for the atomic number and R counts inter distance of each pair. For example, R_{AB} is the distance between the atomic centers of atom A and B. Using Eqs. (3.3) to (3.7) one can rewrite Eq. (3.2) as follows which is exact Schrödinger equation in operator form.

$$\widehat{H} = \widehat{T_e} + \widehat{T_{nu}} + \widehat{V_{e-nu}} + \widehat{V_{e-e}} + \widehat{V_{nu-nu}} \tag{3.8}$$

The mass of a nuclei is thousand times more than the electron. Due to their masses, the nuclei move much slower than the electrons. For this reason, one can assume nuclei are not moving at all and they are sitting in fixed positions. In contrast, the electrons are moving in the field of fixed nuclei. Basically, this is a very important approximation to the Schrödinger equation called as Born-Oppenheimer approximation (BOA) [89].

3.3.2. Born-Oppenheimer Approximation

Due to this approximation, it is instructive to take kinetic energy of nuclei ($\widehat{T_{nu}}$) as zero. Since nuclei are sitting in a fixed position their electrostatic potential energy ($\widehat{V_{nu-nu}}$) is a constant. Removing these two terms from Eq. (3.8), electronic Hamiltonian reduces to the Eq. (3.9).

$$\widehat{H_{elec}} = \widehat{T_e} + \widehat{V_{e-nu}} + \widehat{V_{e-e}} \tag{3.9}$$

Due to BOA, the Schrödinger equation now reduces to Eq. (3.10).

$$\widehat{H_{elec}}\psi_{elec} = E_{elec}\psi_{elec} \tag{3.10}$$

Solution to this Schrödinger equation is ψ_{elec} and electronic energy is E_{elec}. The total system energy will be the sum of electronic energy and the constant nuclear repulsive energy.

$$E_{tot} = E_{elec} + E_{nu} \tag{3.11}$$

Here E_{elec} is the Eigen value of Eq. (3.10) and E_{nu} is the Eigen value of the operator mentioned in Eq. (3.7) and defined in Eq. (3.12).

$$E_{nu} = \sum_{A=1}^{M} \sum_{B>A}^{M} \frac{Z_A Z_B}{R_{AB}} \tag{3.12}$$

3.3.3. Variational Method for Ground State

So far, an approximate Schrödinger equation has been formulated above. Next part is to use variational method to find ground state energy. If an electronic system is in the state ψ, it's expectation value of the energy is,

$$E(\psi) = \frac{\langle \psi | \hat{H} | \psi \rangle}{\langle \psi | \psi \rangle}. \tag{3.13}$$

Here,

$$\langle \psi | \hat{H} | \psi \rangle = \int \psi^*(\vec{r}) \hat{H} \, \psi((\vec{r})) d\vec{r} \tag{3.14}$$

According to variational principle, the energy computed from a guessed ψ is an upper bound to the true ground-state energy (E_0). To obtain full minimization of the functional $E(\psi)$ with respect to all allowed N-electrons' wave functions are required. This full minimization will then give the true ground state, ψ_0 and energy (E_0). Here, expected energy ($as\ E(\psi_0) = E_0$) of the ground state is the minimum energy of the system.

$$E_0 = \min_{\psi \to \mathrm{N}} E(\psi) = \min_{\psi \to \mathrm{N}} \langle \psi | \widehat{H_{elec}} | \psi \rangle \tag{3.15}$$

Here in Eq. (3.15), Hamiltonian operator is already discussed and formulated in Eq. (3.9). If a material system has N electrons and given nuclear potential is V_{ext}, the variational principle formulates a procedure to obtain the ground-state wave function. In other words, the ground state energy is a functional of the number of electrons N and the nuclear potential V_{ext} as described by Eq. (3.16).

$$E_0 = \mathrm{E}[\mathrm{N}, \mathrm{V}_{ext}] \tag{3.16}$$

Once ground state wave functions are obtained, ground state energy can be calculated from the expected value of energy. From ground state wave functions, electron density of ground state and other related properties of the material can be calculated.

3.3.4. Electron Density

So far, a variational principle has been adopted to find system's ground state. However, complexity lies in defining wave function and finding exchange correlation term in Hamiltonian operator. For several decades, scientists came up with several approximations to this problem and are still looking for a better one. Hartree-Fock approximation is one of its kind from the very beginning. After implementing any of these approximation, electron density (ρ) is calculated. The electron density (ρ) is the most important quantity in DFT. The electron density (ρ) is the integral over the spin coordinates (s) of all electrons and over all but one of the spatial variables ($\vec{x} \equiv \vec{r}, s$).

$$\rho(\vec{r}) = N \int \dots \int |\psi(\vec{x_1}, \vec{x_2}, .., \vec{x_N})|^2 ds_1 \, d\vec{x_1} d\vec{x_2} .. d\vec{x_N} \tag{3.17}$$

Here $\rho(\vec{r})$ determines the probability of finding any of the N electrons within an infinitesimally small volume element $d\vec{r}$. The central part of any DFT calculation is $\rho(\vec{r})$ which is an observable or in other words, $\rho(\vec{r})$ is an experimentally measurable quantity. It is a non-negative quantity and its spatial integration over a certain volume counts number of electrons in that certain volume. At infinity $\rho(\vec{r})$ vanishes to zero. All the properties of the ground state can be determined from $\rho(\vec{r})$.

3.3.5. Functional Approximation for DFT

Once $\rho(\vec{r})$ of ground state is known, the kinetic energy $T[\rho(\vec{r})]$, the potential energy $V[\rho(\vec{r})]$, and the total energy $E[\rho(\vec{r})]$ can be written as,

$$E[\rho(\vec{r})] = T[\rho(\vec{r})] + V[\rho(\vec{r})]$$
$$E[\rho] = T[\rho] + E_{nu-e}[\rho] + E_{e-e}[\rho] \tag{3.18}$$

In Eq. (3.18), the total energy is the sum of kinetic energy and potential energy. Because of high masses of nucleus their velocity is negligibly small in comparison to electrons. This is why in Eq. (3.18), $E_{nu\text{-}nu}$ is omitted. Potential energy consists of two electrostatic potential energy terms. First one is due to attraction energy in between nuclei and electron. Second one is electron-electron repulsive energy. First one can be calculated using Eq. (3.19) as follows,

$$E_{nu-e}[\rho] = \int \rho(\vec{r}) V_{nu-e}(\vec{r}) d\vec{r} \tag{3.19}$$

Here $V_{nu-e}(\vec{r})$ is the electrostatic attractive potential in between electron and nuclei. Now electrons kinetic energy is taken into account and electrostatic repulsive energy, F_{HK} can be expressed as,

$$F_{HK}[\rho] = T[\rho] + E_{e-e}[\rho] \tag{3.20}$$

The total energy becomes,

$$E[\rho] = F_{HK}[\rho] + \int \rho(\vec{r}) V_{nu-e}(\vec{r}) d\vec{r} \tag{3.21}$$

Here first term in Eq. (3.21) is the central idea of using DFT calculation. Second term, only depends on the numerical calculation and can be calculated exactly without any approximations. However, first term of Eq. (3.21) is not known to be solved exactly and this is why one has to use approximations. First approximation to be discussed here will be the first Hohenberg-Kohn (HK) theorem [85].

Functional expressed in Eq. (3.20) is a universal functional which is completely independent of the material system at hand. This is why it applies equally well to the hydrogen atom as to gigantic molecules of few hundreds of atoms such as protein or a DNA cell. Explicit form of both of these two terms of Eq. (3.20) still remains in dark and still remains as a challenge in DFT. First term of Eq. (3.20) which is the kinetic energy term and the second term of Eq. (3.20) can be expressed as follows:

$$E_{e-e}[\rho] = \frac{1}{2} \int \int \frac{\rho(\vec{r_1}) \rho(\vec{r_2})}{r_{12}} d\vec{r_1}\ d\vec{r_2} + E_{non_classical} \tag{3.22}$$

Here in Eq. (3.22) first term is the classical electron-electron interaction and it is known. In future, this first term will be noted as $J[\rho]$. The second part is non-classical component which includes following interactions:

1. Self-interaction correction
2. Exchange interaction
3. Coulomb interaction.

Functional mentioned in Eq. (3.20) attains its minimum value with respect to all allowed densities if and only if the input density is the true ground state density. Using variational principle, the minimum value of this functional is obtained. However, this variational principle is limited to the ground state only and not applicable for an excited sate. A higher level of theory is required beyond HK theory.

3.3.6. Kohn-Sham Equations

Rewriting Eq. (3.15) for the minimum energy in terms of electron density instead of wave functions and energy in terms of functional,

$$E_0 = \min_{\rho \to N} \left(F[\rho] + \int \rho(\vec{r}) V_{nu-e}(\vec{r}) d\vec{r} \right) \tag{3.23}$$

Here, the universal functional $F[\rho]$ accounts for contributions of the kinetic energy, the classical Coulomb interaction and the non-classical portion. Eq. (3.20) can be rewritten with the help of Eq. (3.22) as,

$$F[\rho] = T[\rho] + E_{non_classical} + J[\rho] \tag{3.24}$$

Only the third term of Eq. (3.24) is known. Finding first two terms is a challenge here. Thomas- and Fermi (TF) [87] modeled those first two terms but because of accuracy issues they were not very useful. To solve this problem Kohn and Sham (KS) in 1965 [90] proposed a new theory which is the basis of present day DFT. Kohn and Sham suggested to calculate the exact kinetic energy of a non-interacting reference system with the same density as the real, interacting one. Non-interacting kinetic energy and density can be calculated as in Eq. (3.25) and Eq. (3.26):

$$T_S = -\frac{1}{2}\sum_{i=1}^{N}\langle\psi_i|\nabla^2|\psi_i\rangle \tag{3.25}$$

$$\rho_S(\vec{r}) = \sum_{i=1}^{N}\sum_{s}|\psi_i(\vec{r},s)|^2 = \rho(\vec{r})\,. \tag{3.26}$$

Here, $\psi_i(\vec{r},s)$ are the orbitals of the non-interacting system and T_S is not the true kinetic energy of the system. Kohn and Sham accounted for that by introducing the following separation of the functional $F[\rho]$,

$$F[\rho] = T_S[\rho] + E_{XC}[\rho] + J[\rho] \tag{3.27}$$

The second term is called as exchange-correlation and defined as follows in Eq. (3.28),

$$E_{XC}[\rho] \equiv (T[\rho] - T_S[\rho]) + (E_{e-e}[\rho] - J[\rho]) \tag{3.28}$$

Now everything unknown is absorbed by E_{Xc} functional. The challenge now is reduced to answer the question how can one uniquely determine the orbitals in a non-interacting reference system.

In other words, how can a potential V_S will be defined such that it provides with a Slater determinant [88] which is characterized by the same density as the real system. To solve this problem, one can write down the expression for the energy of the interacting system in terms of the separation described in Eq. (3.27). Rewriting total energy equation from Eq. (3.18) in terms of exchange-correlation functional,

$$E[\rho] = T_S[\rho] + J[\rho] + E_{nu-e}[\rho] + E_{XC}[\rho] \tag{3.29}$$

To explicitly mention, all the terms have been plugged in to Eq. (3.29) from Eqs. (3.25), (3.22) and (3.19).

$$E[\rho] = -\frac{1}{2}\sum_{i=1}^{N}\langle\psi_i|\nabla^2|\psi_i\rangle + \frac{1}{2}\int\int\frac{\rho(\overrightarrow{r_1})\rho(\overrightarrow{r_2})}{r_{12}}d\overrightarrow{r_1}\ d\overrightarrow{r_2} + \int\rho(\vec{r})V_{nu-e}(\vec{r})d\vec{r} + E_{XC}[\rho] \tag{3.30}$$

All the terms in Eq. (3.30) are explicit except the last term which accounts for exchange-correlation. To obtain wave function dependency, all the density terms can be replaced by wave functions as following,

$$E[\rho] = -\frac{1}{2}\sum_{i=1}^{N}\langle\psi_i|\nabla^2|\psi_i\rangle + \frac{1}{2}\sum_{i}^{N}\sum_{j}^{N}\int\int\left|\psi(\overrightarrow{r_1})\left|\frac{1}{r_{12}}\right|\psi(\overrightarrow{r_2})\right|^2 d\overrightarrow{r_1}\ d\overrightarrow{r_2} - \sum_{i}^{N}\int\sum_{A}^{M}\frac{Z_A}{r_{1A}}|\psi(\vec{r})|^2 d\vec{r} + E_{XC}[\rho] \tag{3.31}$$

Using variational principle now the problem is to minimize Eq. (3.31) under the constrain of wave function property $\langle\psi_i|\psi_j\rangle = \delta_{ij}$. From this minimization, resulting equations are the KS equation.

KS equation looks like Schrödinger equation but is an approximate to the true Schrödinger equation. KS equation is described by the Eq. (3.32) as follows,

$$\left(-\frac{1}{2}\nabla^2 + \left[\int \frac{\rho(\vec{r_2})}{r_{12}} d\vec{r} + V_{XC}(\vec{r_1}) - \sum_A^M \frac{Z_A}{r_{1A}}\right]\right)\psi_i = \left(-\frac{1}{2}\nabla^2 + V_S(\vec{r_1})\right)\psi_i = \epsilon_i \psi_i. \quad (3.32)$$

Therefore in DFT instead of going after true Schrödinger equation, KS equation is solved to find exact same electron density with approximate wave functions. Any properties that only depends on the electron density can be explained with same accuracy.

Once one knows the various contributions in Eq. (3.32), potential V_S can be obtained which one needs to insert into the one-particle equation, which in turn determine the wave functions and hence the ground state density and the ground state energy employing Eq. (3.31). Here, it is to be noted that V_S depends on the density, and therefore the KS equations have to be solved iteratively which frequently referred as self-consistent field (SCF) calculation. Several approximate functional came to realize exchange-correlation term. To name few of them, local density approximation (LDA), amd generalized gradient approximation (GGA) are very popular. Advanced and hybrid functional are also continuously under development. If one knows the exact functional one could solve KS equations exactly. However, for the purpose of this dissertation where metal, insulator and semiconductor are the primary focus, DFT serves its best. This is why in this dissertation DFT has been taken as primary tool to further investigate new emerging materials. Other relevant advanced theories have also been used and will be discussed in future chapters.

3.3.7. Implementation of DFT

To solve Kohn-Sham (KS) equation for a given material system, QUANTUM ESPRESSO [91] has been used which is a FORTRAN code based with standard input and output options. Through text based input and output materials system has to be defined and passed through standard input for the DFT engine to produce KS wave functions and densities. Later on, standard programming language has been used for the purpose of post processing other properties of the materials. A typical work flow and selection of tools is shown in Fig. 3.1. QUANTUAM ESPRESSO and Wannier90 has been implemented using supercomputers. Code development, testing and input/output generation were done in desktop computer.

In Fig. 3.1, desktop icon and supercomputer icon have been shown to illustrate which segment of simulation went into which kind of physical computing machine along with which tools. This following simulation flow is one of the many calculations which particularly shows I-V characterization of a new material with a finite width and length in quantum ballistic transport regime. In Fig. 3.2, the DOS of graphene using DFT calculation and tight binding (TB) model are compared. It shows that DFT is much more accurate even in the higher energies while TB predicts very smooth DOS.

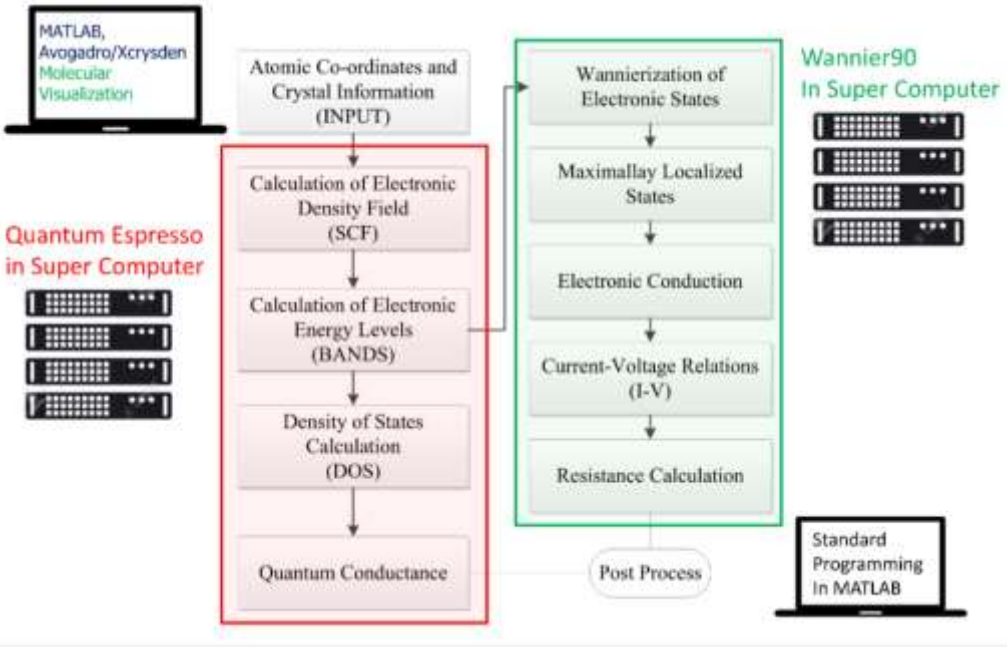


Figure 3.1: Material simulation flow using various software and programming tools across various computational platforms.

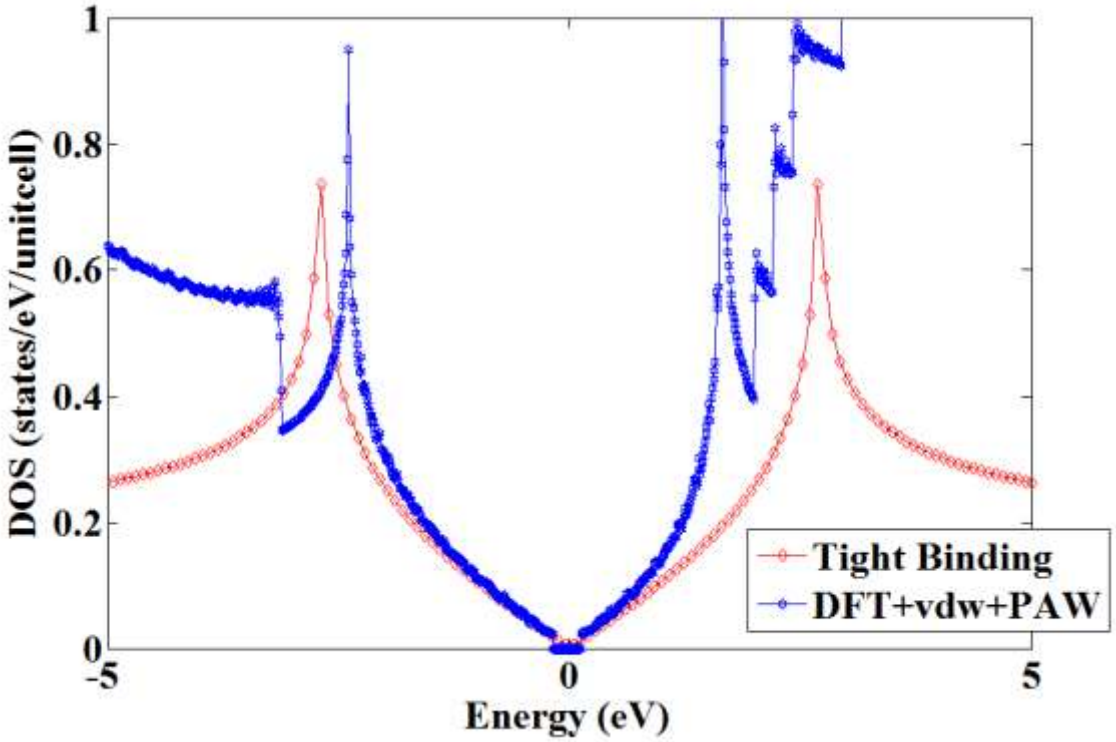


Figure 3.2: Comparison of tight binding model and DFT. Here DFT accuracy has been increased by considering the Van der Waals correction (vdw) along with using plane augmented wave (PAW) implementation.

3.3.8. Conclusion

DFT is presently the most successful computational technique and the most useful approach to compute the electronic structure of materials. Its application ranges from atoms, atomic clusters, molecules and solids to nuclei and quantum and classical fluidic phase of matter. In terms of geometry, its applicability ranges from 3D bulk material, 2D material, one dimensional structure, surface and interfaces. The DFT also provides the ground state properties of a system along with ground state electron density. The ground state electron density plays a central role in any electronic properties of the material. Electron energies are typically in the range of few eV which is equivalent to few thousands of Kelvin degrees. Since electronic applications are designed for room temperature electrons are always in the ground state for all practical purposes. In Chemistry, DFT estimates a great variety of molecular properties: molecular structures, vibrational frequencies, atomization energies, ionization energies, electric and magnetic properties, chemical reaction paths, etc. Reaction simulation enables scientist and engineers to develop material growth dynamic and process simulation. The original density functional theory has evolved over many decades and has been generalized to deal with many different sophisticated situations like spin polarized systems, multicomponent systems such as nuclei and electron hole droplets, free energy at finite temperatures, superconductors with electronic pairing mechanisms, relativistic electrons, time-dependent phenomena and excited states, bosons, molecular dynamics, etc. The methodology and codes developed in this chapter will be implemented for the rest of the dissertation to explore emerging nano-materials for VLSI interconnect application.

CHAPTER 4
GRAPHENE/COPPER HYBRID INTERCONNECT: RESISTIVITY

Recent studies have shown superior thermal transport of graphene on copper as a potential candidate for the next generation interconnects. Using density function theory (DFT) current transport of graphene/copper (G/Cu) hybrid-nano wire interconnect system is studied and compared the electrical characteristics with other two-dimensional counterparts along with graphene. From the first principle calculations, band structure and density of states have been calculated. Using Landauer-Buttiker (LB) formalism, electrical transport is calculated and explained why G/Cu hybrid interconnect shows more conductivity than the graphene only interconnects with the help of phase space argument. As graphene on copper system has more available density of states near the Fermi level it offers more states than graphene for conduction.

4.1. Introduction

In very large-scale integration (VLSI), application of emerging nano-electronic devices demands compatible interconnect solution to meet challenges of ever-shrinking technology nodes. In scaled CMOS technology nodes, traditional copper based interconnect is facing challenges due to low scalability, electromigration, void formation, high resistivity and many other performance

[*] Portions of this research were conducted with high performance computing resources provided by Louisiana State University (http://www.hpc.lsu.edu). Part of the work is reported in the following publication:

1. K. M. Mohsin, A. Srivastava, A. K. Sharma, C. Mayberry, and M. S. Fahad, "Temperature sensitivity of electrical resistivity of graphene/copper hybrid nano ribbon interconnect: A first principle study," ECS Journal of Solid State Science and Technology, vol. 6, no. 4, pp. P119-P124, 2017.
2. K. M. Mohsin, A. Srivastava, A. K. Sharma, C. Mayberry, and M. S. Fahad, "Current transport in graphene/copper hybrid nano ribbon interconnect: A first principle study," ECS Transactions, vol. 75, no. 13, pp. 49-53, Aug 25, 2016.
3. K. M. Mohsin, A. Srivastava, M. S. Fahad and M. A. Khan, "Quantum capacitance of graphene copper hybrid nanoribbon," ECS Journal of Solid State Physics. Accepted on Oct., 2017.

limitations [7]. In search of emerging materials and for replacement of copper interconnect in nanometer CMOS technology nodes, graphene (G) and carbon nanotubes (CNT) have been studied intensively for a decade. Due to high electrothermal conductivities of different variants of carbon nanotube (CNT) and graphene, research has advanced further to explore potential of these nano-materials as future VLSI interconnect [24-27, 29, 30, 49, 51, 92-94]. Because of high thermal conductivity, CNT interconnects can quickly drain out heat to make interconnect more thermally stable [25, 40]. However, CNT wafer scale alignment in between contacts is still very challenging [95]. Whether a CNT is metallic or not, depends on chirality and that is why it requires separating CNT of particular chirality from the growth media system. This selective growth and etching of CNT or separation of particular chirality remains an open challenge [96].

Scalability of length is very crucial for interconnect technology from modeling and implementation perspective. In recent years, graphene nanoribbon (GNR) has received more attention due to ease of graphene (G) growth by chemical vapor deposition (CVD) and patterning using e-beam lithography. Although bulk two-dimensional graphene is semi-metallic with zero density of states at Dirac point, its one-dimensional counterpart GNR is not metallic always. As an interconnect material, it needs to be metallic. As the width of GNR decreases, band gap opens up which makes this material not suitable for interconnect application. From chirality point of view, only zigzag edge (toward transport direction) is always metallic regardless of GNR width. On the other hand, armchair could be metallic or semiconducting depending on chirality. Therefore, metallic nature of GNR also becomes selective to chirality. Beside CNT and graphene, both of these materials share the same challenge of contact resistance, which limits overall performance of interconnect significantly [97, 98]. This motivates the scientific community to

look for the hybrid material system to obtain metallic properties out of GNR while not losing greater thermal stability and mechanical strength. There is an ongoing research to find hybrid materials with better thermal and electrical conductivity [99].

Recent studies found that graphene on copper might be a possible solution for lowering the temperature of interconnects [99, 100]. Reduction in peak temperature by 27% has been observed in graphene encapsulated copper wires [100]. This reduction in temperature eventually reduces resistance and RC delay that increases data transfer by 15% from its copper nanoribbon counterpart. Previously graphene coated copper was reported for having excellent thermal property and attributed to copper nanoribbon not because of graphene [99]. Graphene deposition on copper requires temperature around 1200 K while Cu annealing occurs and Cu grain size becomes larger. Larger grain of copper nanoribbon reduces resistivity by increasing electron's mean free path (MFP) [101]. In addition, graphene works as a barrier layer for a copper ion preventing diffusion into the dielectric. This is why it was believed that excellent electrical transport and thermal properties are inherent to copper; graphene is only assisting by providing heat-spreading path to copper nanoribbon. Although internal dynamics requires more confirming experimental reports, it is also necessary to investigate this material system theoretically from the perspective of VLSI interconnect. Previously graphene growth dynamics [102] and interfacial structure [103] have been studied theoretically using first principle calculations. Using molecular dynamics (MD), thermal transport of graphene on copper has also been studied [104]. However, for G/Cu system there is little theoretical study from the point of view of electrical transport with a special focus on interconnect applications. In this work, G/Cu structure for bulk (2D) and for

one-dimensional nanoribbon (1D) as a potential material for next generation interconnect applications are investigated theoretically.

In this chapter, the band structure of G/Cu hybrid system and temperature dependent resistance of nano interconnects are examined to understand theoretically how this hybrid material system outperforms graphene only interconnect at temperatures higher than the room temperature (RT). Here density of states (DOS), current-voltage (I-V) relation and resistance (R) of G/Cu nano ribbon interconnects at different temperatures are calculated to understand G/Cu system. From temperature dependent resistance, temperature coefficient of resistivity (TCR) is calculated. It was found to be constant at low biases. Following this introduction, in Section 4.2, methods of calculations are presented. In Section 4.3, results are presented with discussion. At the end, future prospects and limitations of this work are addressed.

4.2. Simulation Method

For simulation, three atomic layers of copper are considered and arranged in such a way that <111> crystal plane is aligned along the Z-axis. Therefore, flat surface of copper is <111> plane. On top of this flat surface of copper, graphene monolayer is placed. Graphene monolayer was placed in such a way that graphene edge is zigzag towards the transport direction, which is X-axis in this case. Since Cu <111> plane is a hexagonal lattice with almost similar lattice constant like graphene (2% mismatch), graphene atoms are placed on <111> planes of Cu. Unit cell of bulk two-dimensional G/Cu system consist of three copper atoms in three different atomic layers along with two carbon atoms sitting on the top most copper layer. Lattice constant and lattice vectors are shown in Fig. 4.1. For electrical transport studies, one-dimensional hybrid G/Cu

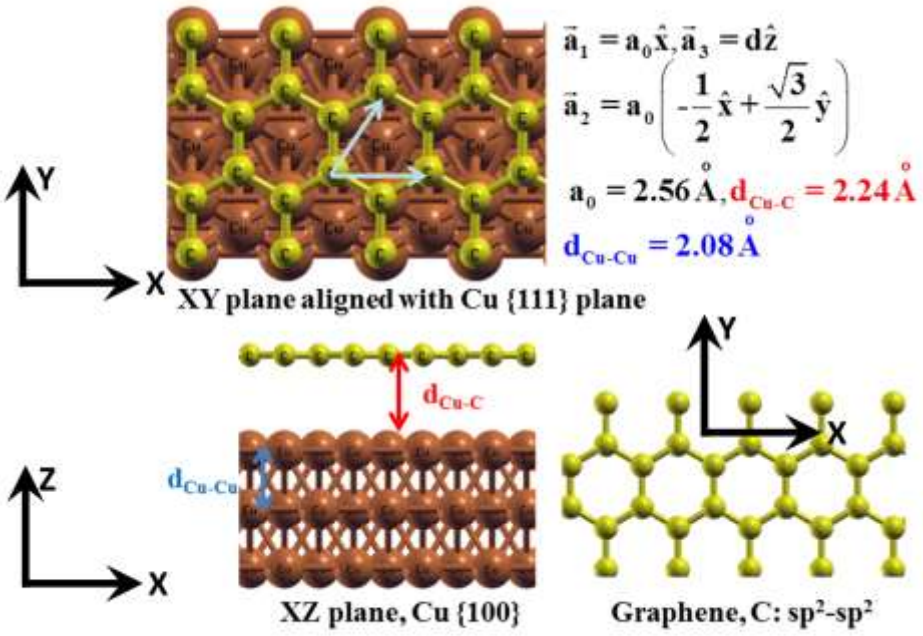


Figure 4.1: Atomic structure of graphene on copper hybrid nano-interconnect in XY plane (top) and in XZ plane (bottom). Cu <111> plane is towards Cartesian Z-axis (which is XY plane). Lattice vectors for this system are shown on top right. Scale for the top, bottom and bottom-right are not same.

nanoribbon of width 0.6 nm, height 0.8 nm is considered. For a finite length, atomistic simulation up to 10 nm of interconnect length is considered here.

Density functional theory (DFT) is implemented to study electronic band structure within Quantum-Espresso (QE) code [91]. For exchange correlation (XC), local density approximation (LDA) is used specifically developed by Perdew-Zunger [105]. Projector augmented-wave [106] type pseudo-potential which was used to obtain relativistic correction was also used to consider contribution of core electrons. For atomic structure optimization, fixed cell relaxation calculation method was used. Then relaxation calculation was performed by fixing bottom layer of Cu atoms in their bulk position as reference plane.

In relaxation calculation, atoms in the top two Cu layers and graphene layer were allowed to move in finding minimum energy position for the whole system in equilibrium. Relaxation calculation started with atomic positions calculated from their bulk system. Later on, updated atomic positions obtained from the relaxation calculation are used. Inter-planar distance for Cu <111> planes is 2.08 Å, which is calculated from the bulk copper lattice constant in <100> plane (3.6149 Å). The distance between top Cu layer and graphene layer is 2.24 Å [103]. We began relaxation calculation with lattice constant 2.56 Å and obtained atomic positions of top two layers (two layers of Cu and one layer of graphene) by minimizing force up to 0.05 $eV \cdot Å^{-1}$. Because of relaxation, we found that C-Cu interlayer distance increases slightly. Relaxation calculation optimizes co-ordinates for all atoms in the system for finding the minimum energy state. From the calculation of an optimized structure, we found that three atomic layers of copper can best describe the properties under study. It is for this reason we have limited the study to 3-layers of

copper only. Using these optimized atomic positions, we then performed self-consistent field (SCF) calculation.

In each SCF cycle, it calculates electron density field. Using variational method, this SCF calculation is a minimization technique for electron density function. It tries to minimize overall system energy for a particular electron density distribution. When the difference of system total energies of two consecutive SCF cycles reached as small as 10^{-9} eV we stop SCF calculation. SCF calculation took 41 iterations to converge with a tolerance of 10^{-9} eV. In SCF calculation, energy cut off 40 Rydberg (Ry, 1Ry=13.6 eV) was used to limit wave functions tails. During SCF calculation, we sampled Brillouin Zone (BZ) uniformly with 32x32x1 K-grids using Monkhorst-Pack (MP) method [107] for 2D bulk system. For one-dimensional nanoribbon, we used 128x1x1 K-grids. MP method ensures generation of special points in the BZ for facilitating efficient integration of periodic functions of the wave vector over entire BZ. Total overall system energy from SCF calculation was -1977 Ry for a one-dimensional system and -658 Ry for a 2D bulk system. Total energy for 2D bulk is for five atoms basis while for nanoribbon number of atoms is fifteen. That is why total system energy is higher in nanoribbon case.

Electron density obtained from SCF calculation was used for another round of calculation for finding energy levels for each point of a densely sampled BZ. We used 64x64x1 k-grids for BZ sampling using the MP method for 2D bulk and 256x1x1 for nanoribbon. From this calculation, we obtained electronic band structure and electrons occupations in those energy states. We performed band structure calculation for 80 energy levels and obtained 0.7179 eV Fermi energy for the bulk case and -3.9858 eV for the hybrid nanoribbon. Later on, for all other calculations, we adjusted these Fermi energies to 0 eV when necessary for comparison or for

transport calculations. From SCF calculation, we constructed band structures and calculated density of states (DOS) of this hybrid system within QE code. For DOS calculation, energy levels are adjusted in such way that the Fermi energy becomes 0 eV. Energy spectrum is sampled with a resolution of 10 meV.

We used Wannier90 code [108] for transport study based on the Bloch states obtained from SCF calculations. First step is to transform Bloch waves into Wannier Function and then finding maximally localized Wannier Wave Function (MLWF). Rest of the transport properties depend on MLWF. From MLWF, we have computed current voltage relation (I-V). Since the length of this interconnect is very short, we had to decide the right theory for transport. Typical electronic MFP of copper is 40 nm and few microns for graphene. We assumed for this hybrid system electrons MFP to be greater than 40 nm and smaller than 1000 nm. If this is the case for the MFP then this hybrid interconnect transport should be ballistic in nature for any given interconnect length less than 40 nm. Hence, to compute current-voltage relation at different temperatures we adopted Landauer-Buttiker (LB) formalism implemented in Wannier90 code [108],

$$I = \frac{2e^2}{h} M \frac{\mu_1 - \mu_2}{e} \tag{4.1}$$

Here e is magnitude electronic charge and h is Planck constant. M counts the number of transport modes for a conductor, μ_1 and μ_2 are electrochemical potentials of left and right contacts. Wannier90 code uses Bloch States obtained from QE code to obtain MLWF and construct system Hamiltonian. After obtaining Hamiltonian, Wannier90 uses Non-Equilibrium Green Function (NEGF) for the transport calculation and transmission coefficient. In Landauer-Buttiker (LB)

formalism, by definition the transmission coefficient is QC. Due to high computational cost for first principle study, we have limited our study to a 10 nm long wire, which represents a short local interconnect and a good example of ballistic transport. For ballistic transport, one should not use Fuchs-Sondheimer (FS) and Mavadas-Shatzkes (MS) models [101] for resistivity estimation. Therefore, in ballistic transport regime, instead of FS and MS theories we have used LB formalism. In NEGF method, temperature variation was taken into account by manipulating value of thermal broadening (~$3.5K_BT$). From current voltage characteristics at different temperatures, we have calculated temperature dependent resistance. We use the following equation for TCR calculation,

$$\alpha = \frac{1}{R_0}\frac{\delta R}{\delta T} \tag{4.2}$$

where α is *TCR* at 300 K and R_0 is resistance at *300 K*.

4.3. Results and Discussion

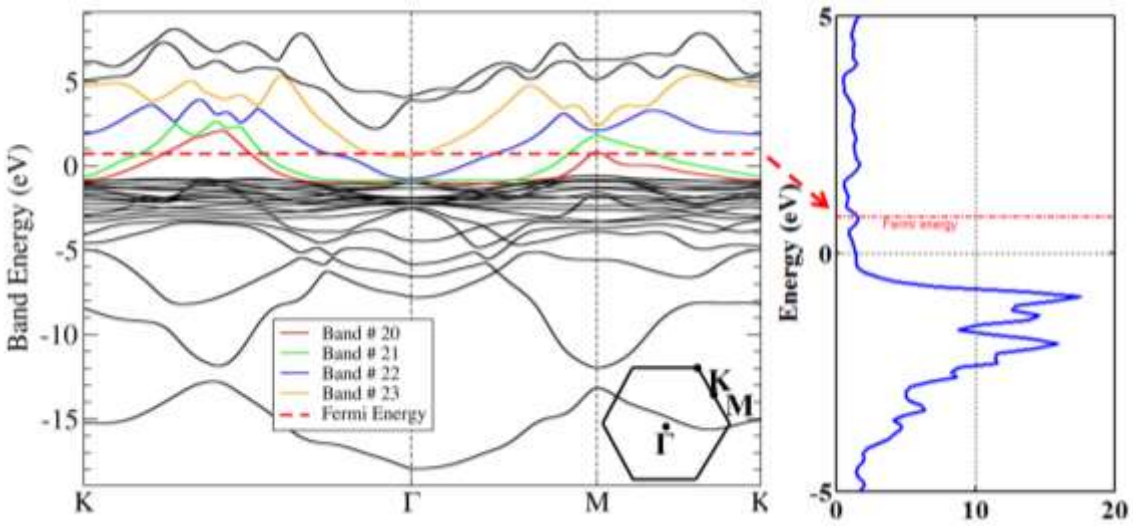
Electronic band structure of G/Cu hybrid system for bulk (2-D) and nanoribbon (1-D) are shown in Fig. 4.2 and in Fig. 4.3 respectively. From band structure of bulk 2D system, it is apparent that four bands are crossing Fermi level (0.7179 eV). Those Fermi level crossing bands are highlighted with red, green, blue and orange color in Fig. 4.2(a) in the order of their energy from low to high energy. We counted band index from the lowest energy one as first (near - 15 eV). With this counting, bands with indices 20 to 23 are contributing in constructing the Fermi surface. For a metallic system, this multiple band crossing is expected. DOS of G/Cu bulk system is shown in Fig. 4.2(b). Being an infinite two-dimensional system, DOS is continuous. Most

importantly DOS is continuous and non-zero near the Fermi energy. Just below 0 eV, there is a dense crowd of bands that is consistent in DOS also.

For G/Cu nanoribbon, band structure and DOS are shown in Fig. 4.3(a) and Fig. 4.3(b), respectively. Unlike GNR, there is a non-zero DOS at Fermi level for G/Cu nanoribbon. In case of nanoribbon, DOS is discrete due to one-dimensional confinement of the electron. In this hybrid system because of Cu, more states are available in an energy window near the Fermi energy. Fig. 4.3(b) shows the density of states (DOS) comparison of graphene and G/Cu material system. This difference of DOS in these two material systems causes their difference in current transport. Density of states near the Fermi energy do not change significantly with increasing the number of copper layers. Increasing the number of copper layers will increase absolute number of DOS and charge carriers as well as the electrical conductance. However, the electrical conductivity which depends on per unit volume does not change because as we increase the number of copper layers we are also increasing the total volume. Therefore, near the Fermi energy, three layers of copper best describe the structure which is computationally less expensive than a structure with the higher number of copper layers. According to transport theory, if there are no available electronic states in the transport media for a given energy window, no transport will happen for electrons of that particular energy window. In Fig. 4.4(a), graphene current-voltage relation has been compared with G/Cu system. For any biasing voltages, in between -1.34 V and 1.34 V, I-V curve is flat for graphene and linear for G/Cu system.

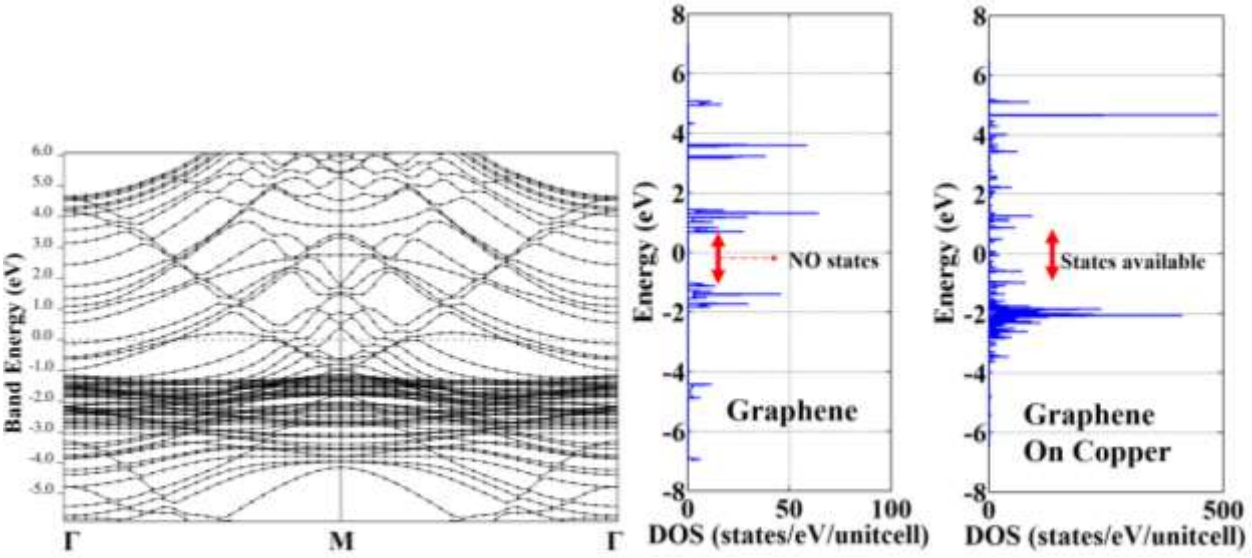
In the energy window -1.34 eV to 1.34 eV, there is no electronic transport for graphene. However, for G/Cu there is electronic conduction in a broad energy window because of availability of electronic states as shown in Fig. 4.3(b). This is why at low biasing G/Cu is a better

conductor than graphene nanoribbon. Because of quantum confinement, graphene nanoribbon behaves like a semiconductor rather than a conductor.



(a) (b)

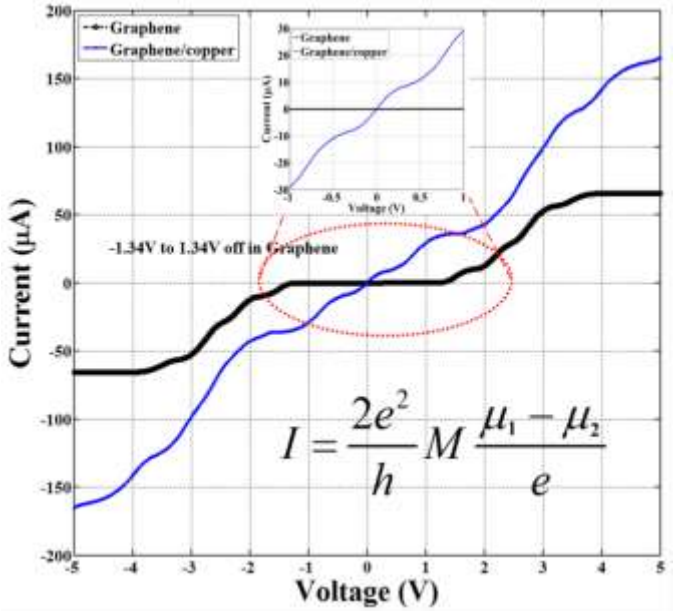
Figure 4.2: (a) Band structure of G/Cu bulk system. Bands contributing to contstruct Fermi surface are high lighted with color. Fermi Energy is 0.7179 eV shown in red dashed line. At the bottom left corner of the band strucuture plot BZ special points are shown. (b) Density of States (DOS) from -5 eV to 5 eV are shown. Fermi energy is marked in DOS plot seperately with red dashed line. Unit of bulk DOS is states/eV/atom.



(a) (b)

Figure 4.3: (a) Electronic band structure of G/Cu nanoribbon. Fermi level at - 4.08 eV (b) Density of states of graphene interconnect are compared with graphene/copper interconnect. Fermi energy is set to 0 eV in (a) and (b) for the purpose of comparison of two different material systems. Near the Fermi energy, there are no states available for the graphene interconnect.

(a)



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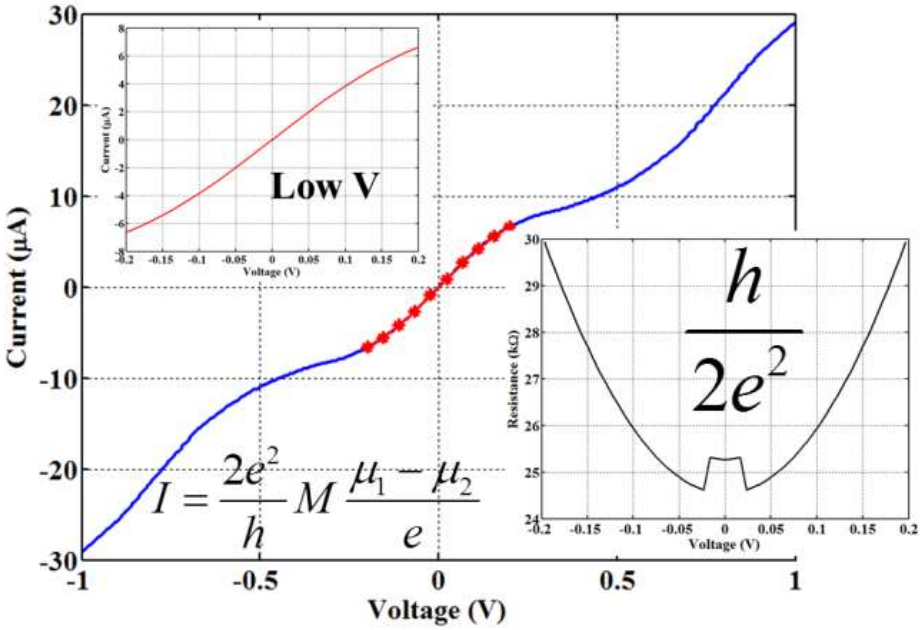

Figure 4.4: (a) Current voltage (I-V) characteristics of G/Cu nanoribbon interconnect compared with graphene only interconnect. For graphene, no current is observed between -1.34 V to 1.34 V because of not having available states in that energy window. However, for graphene on copper is still conductive in this window. (b) I-V characteristics of G/Cu with lower bias voltage. Top inset shows linear region near zero bias and lower inset shows resistance versus voltage relations.

In Fig. 4.5, current versus voltage (I-V) characteristics are shown at different temperatures. This will be further confirmed by low TCR values for this interconnect material system. Plateaus are shown in inset of Fig. 4.5. Due to lateral confinement, energy levels are discrete and so is quantum capacitance (QC) spectra as in quantum well. Due to discrete QC, these plateaus are observable. I-V characteristics of Fig. 4.5 have been used to compute resistance versus current at different temperatures in Fig. 4.6. Slope of I-V curve changes near a plateau and ends up with oscillation in resistance. We have shown temperature dependent resistance in Fig. 4.6 for low bias current. Resistance increases with the temperature, which is expected for positive TCR materials. This is in contrast to graphene interconnect case where resistance quenching happens at high temperatures [109]. Interestingly, resistance decreases with increase of biasing current. This is due to plateau as mentioned earlier. At 300 K, the resistivity of the hybrid structure is calculated as 125 μΩ-cm whereas Cu bulk resistivity is 1.72 μΩ-cm [110]. As estimated by the MS-FS theory [101], MPF of Cu will decrease for width below 40 nm which will increase wire resistivity significantly. Experimentally 180 nm G/Cu nanowire has been tested and measured resistivity is 5 μΩ-cm which is in good agreement with MS-FS theory [100]. Bellow 180 nm, G/Cu nanowire structure is yet to be measured experimentally.

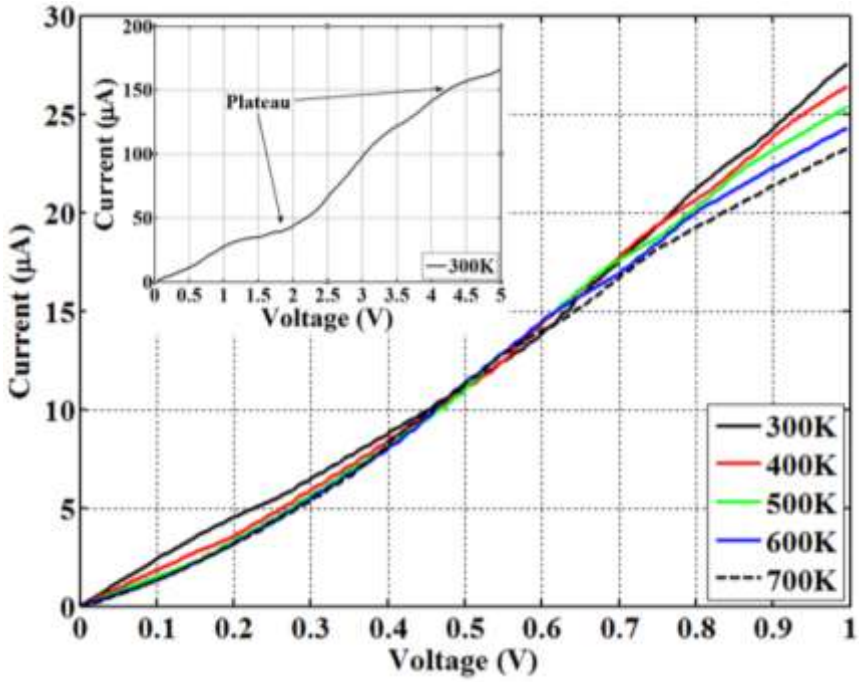

Figure 4.5: I-V characteristics of G/Cu interconnect at different temperatures. Inset shows I-V characteristics for 0 to 5V bias with several plateaus.

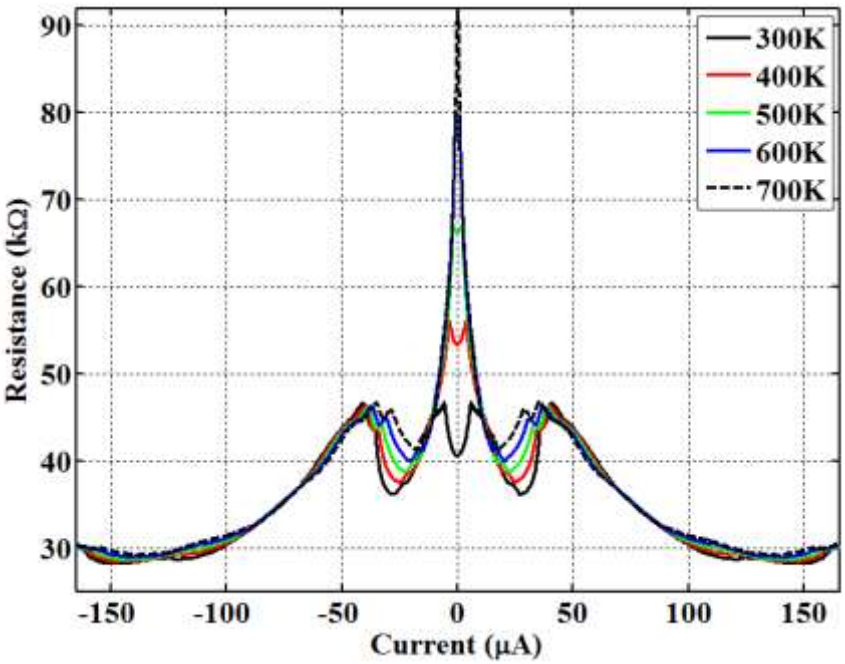

Figure 4.6: Resistance versus current at different temperatures.

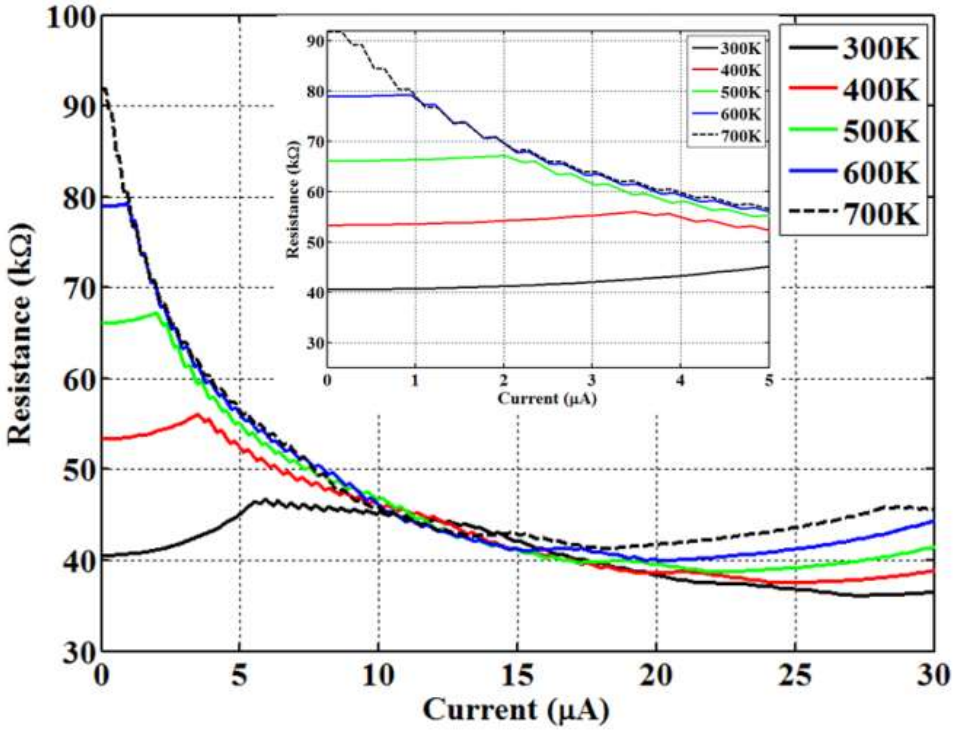

Figure 4.7: Resistance versus current at low bias current.

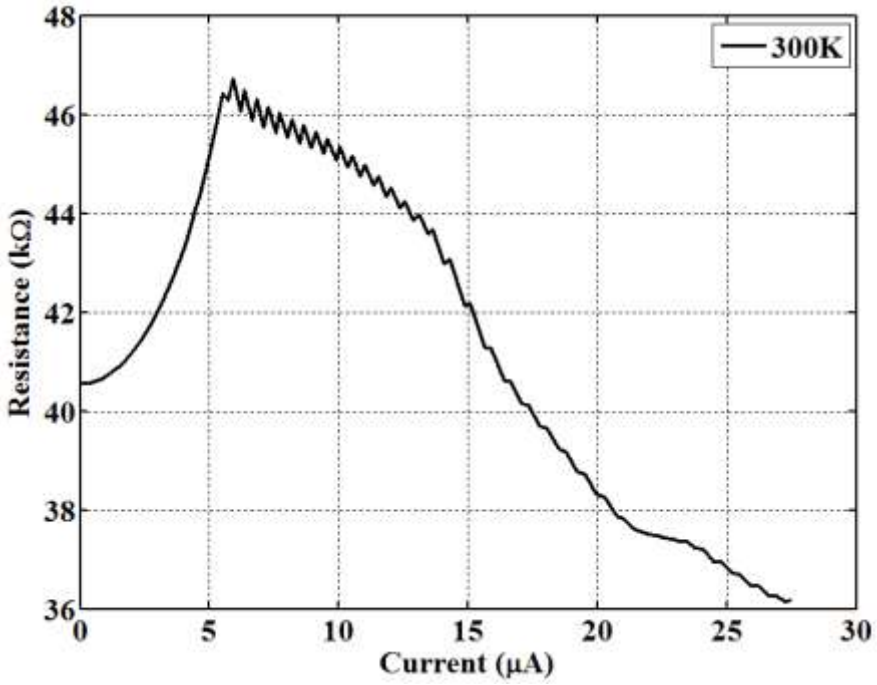

Figure 4.8: Resistance versus current variation at room temperature. Resistance decreases with increase in biasing current due to plateau in I-V characteristics.

In Fig. 4.7, it is shown that at 300 K the resistance increases up to 6 μA and then starts decreasing. Since in higher energies far from the Fermi level there is more DOS hence denser QC brings the resistance down. Fig. 4.8 shows how resistance varies at different current bias at room temperature. Fig. 4.9 shows the differential resistance. There is a sharp jump in differential resistance around 48 μA. It is also apparent in Fig. 4.6 that around 48 μA resistance begins to oscillate. Again, beyond 48 μA resistance decreases monotonically. In Fig. 4.10, temperature dependent resistances are shown at different bias voltages. We limit bias voltage from few tens of mV to 200 mV keeping in mind that next generation low power interconnect will not suffer that high bias stress. On the other hand, interconnect might suffer from high current stress but not voltage stress.

It is apparent that in all biasing voltages, resistance increases linearly with the temperature at least around normal semiconductor operational range (300 to 370 K). This infers to have constant positive TCR which we present in Fig. 4.11. At 50 mV bias, calculated TCR is 0.00315 K^{-1} which is lower than the bulk TCR values of other commonly used interconnect materials. For instance, at 300 K TCR for bulk copper, silver and aluminum are 0.00386 K^{-1}, 0.0038 K^{-1}, and 0.00429 K^{-1}, respectively. If we would estimate TCR for nanoribbon of these materials, it would be more than their bulk values because of size effect. Therefore, one can expect that this G/Cu nanoribbon interconnect will be having less TCR than any pure metallic nanoribbon made of any known metal of interest. Low values of TCR indicate that resistance in this G/Cu hybrid system is less sensitive to temperature fluctuation in the chip. Due to self-heating, there are always several high activity regions in the chip, which are called hot spots. Near the hot spot, temperature is elevated over the normal chip operating temperature. An interconnect with high TCR will not be

a suitable choice because of its sensitivity to temperature. It is important to have a uniform clock pulse and uniform RC delay across the chip. To have uniform RC delay, resistance needs to be less sensitive to temperature variation. Interestingly, G/Cu shows negative slope of TCR with increase of bias voltage and it is due to plateau behavior in I-V characteristics.

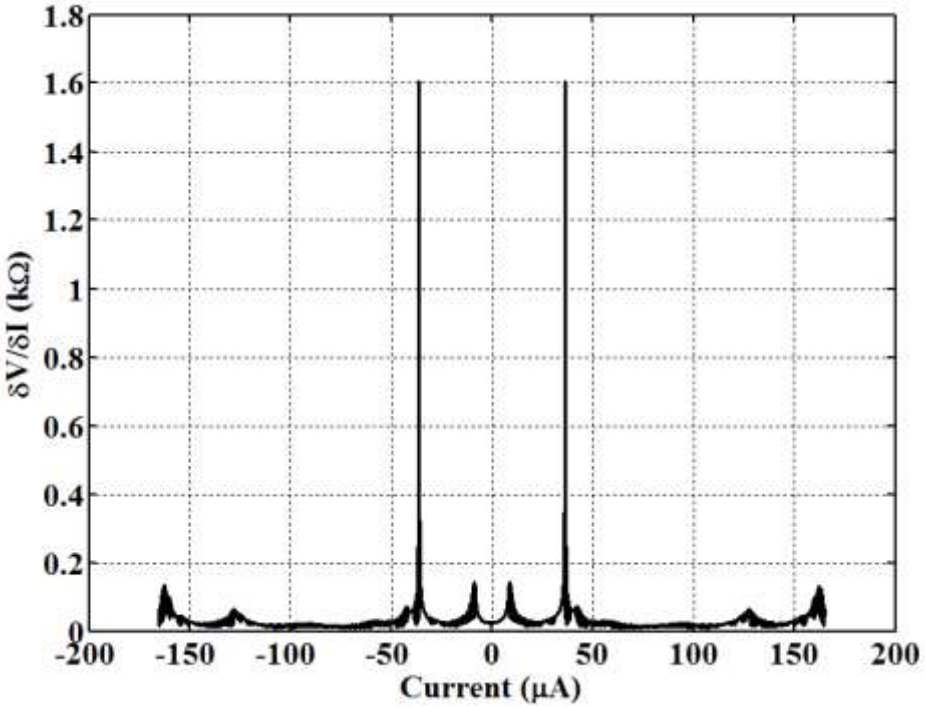

Figure 4.9: Differential resistance versus current.

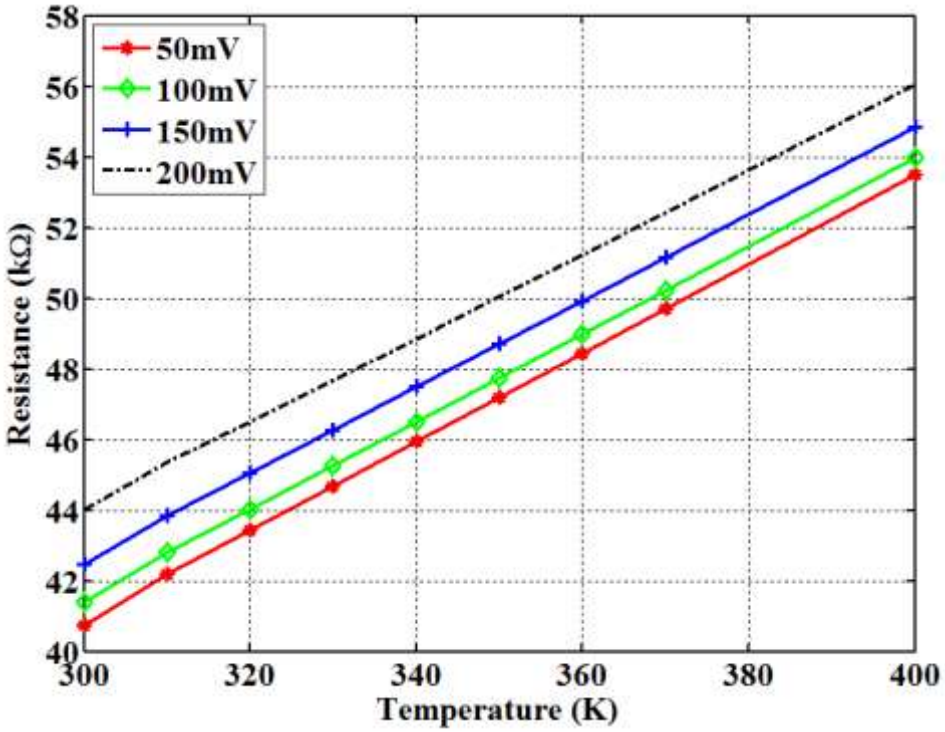

Figure 4.10: Temperature dependent resistance at different bias voltages.

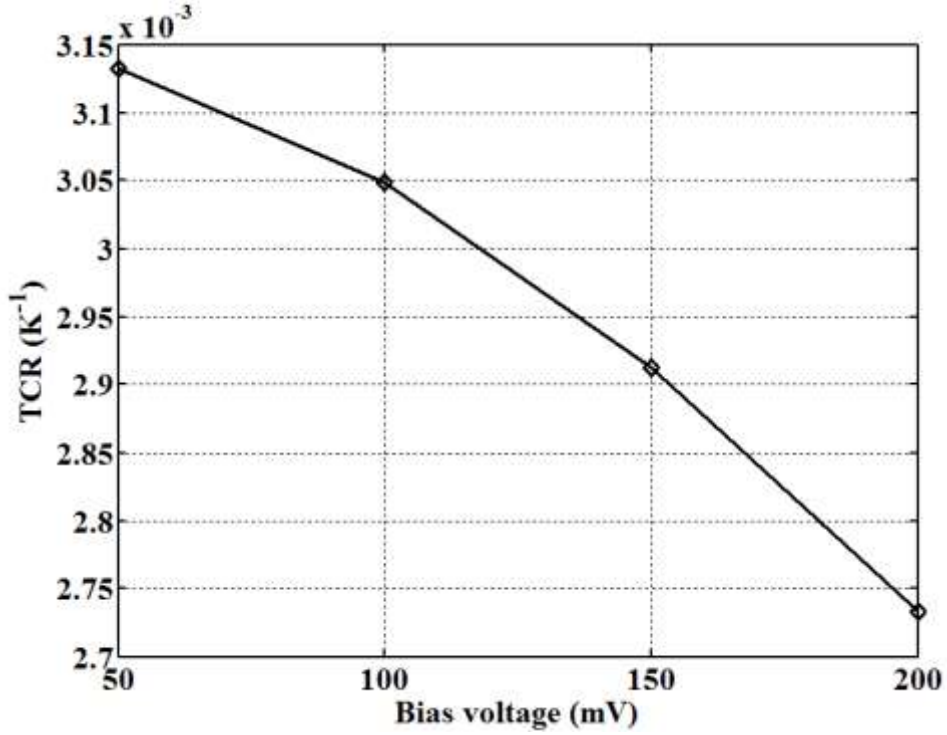

Figure 4.11: Temperature coefficient of resistance change with bias voltage.

4.4. Conclusion

In this chapter, we have simulated a graphene on copper nano-interconnect using DFT code. In addition to I-V characteristics, we studied temperature dependent electrical resistivity and temperature coefficient of resistance (*TCR*). Calculated *TCR* at room temperature is found to be lower than the commonly used other metals such as copper and aluminum. Several plateaus in I-V characteristics are observed for this hybrid interconnect system. The hybrid structure shows better conductivity at low bias than graphene only interconnect. Graphene only nanoribbon might perform better for the device but not for interconnect. Further study is needed in understanding of frequency response characteristics, reliability and integration with the existing CMOS technology. The work can be used in advancing an understanding of electrical performances of other nanostructures for possible interconnect materials.

CHAPTER 5
GRAPHENE/COPPER HYBRID INTERCONNECT: CAPACITANCE

5.1. Introduction

In this chapter, we report density of states (DOS) and the quantum capacitance of (C_Q) of G/Cu nanoribbon interconnect as a continuation of previous chapter. Growth thermodynamics [102], structure [103], thermal properties, capacitance [111, 112] of graphene on copper has been studied theoretically in its pristine and doped [113] forms. Because of computational complexity, most of these theoretical studies were limited to the two-dimensional infinite sheet. In most of the previous works little light had been shed on finite size effect which is necessary for applications such as interconnect, sensor as well as energy storage devices. In this work, with density functional theory (DFT) we have investigated quantum capacitance (C_Q) and related properties of G/Cu nanoribbon (G/Cu-NR) with a finite lateral size (1~5 nm). We have compared our results and found good agreement with previously reported two-dimensional calculations of pristine graphene [113], graphene on copper [112] and experiments [114, 115]. To the best of our knowledge, we are not aware of any prior reported DFT or first-principle based calculation on G/Cu-NR capacitance in one-dimension.

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* Portions of this research were conducted with high performance computing resources provided by Louisiana State University (http://www.hpc.lsu.edu). *Part of this work is reported in the following publications:

1. K. M. Mohsin, A. Srivastava, A. Sharma, and C. Mayberry, "Capacitance of graphene/copper hybrid nano ribbon interconnect - a first principle study," 231st ECS Meeting, New Orleans: Graphene and Beyond: 2D Materials, ECS Trans., vol. 77, no 11, pp. 645-650, June 1, 2017.
2. K. M. Mohsin, A. Srivastava, M. S. Fahad and M. A. Khan, "Quantum capacitance of graphene copper hybrid nanoribbon," ECS Journal of Solid State Physics. Accepted on Oct. 2017.

5.2. Computational Model and Method

We started with the same material system reported in Chapter 4 (Fig. 4.1). We first perform self-consistent field calculation (SCF) by solving the Kohn-Sham (KS)[84, 90] equations within density functional theory (DFT) [84, 85] framework to study electronic structure using Quantum ESPRESSO (QE) package [91] with Van der Waals density functional [18, 116-119]. For exchange correlation (XC) we used local density approximation (LDA) [84] specifically developed by Perdew-Zunger [105]. Projector augmented-wave [106] type pseudo-potential were used to obtain relativistic correction and also to consider contribution of core electrons. For atomic structure optimization, we used fixed cell relaxation calculation. Details of relaxation calculations are reported in Section 4.2. Relaxation calculation optimizes co-ordinates for all atoms in the system for finding minimum energy state. Using these optimized atomic positions, we then performed self-consistent field (SCF) calculation for 2D case. For one-dimensional system, we used supercell of 1x5x1, 1x9x1, 1x14x1, 1x18x1, 1x23x1 which represents 1, 2, 3, 4, and 5 nm of width of G/Cu hybrid materials. For each of these structures, relaxation calculation was followed by SCF calculation.

For 1x5x1 structure, SCF calculation took 41 iterations to converge with a tolerance of 10-9 eV. In SCF calculation, energy cut off 40 Rydberg (Ry, 1 Ry=13.6 eV) was used to limit wave functions tails. During SCF calculation, we sampled Brillouin zone (BZ) uniformly with 32x32x1 K-grids using Monkhorst-Pack (MP) method [42] for 2D bulk system. For one-dimensional nanoribbon, we used 128x1x1 K-grids. MP method ensures generation of special points in the BZ for facilitating efficient integration of periodic functions of the wave vector over entire BZ. Total overall system energy from SCF calculation was -1977 Ry for one-dimensional system (1x5x1)

and -658 Ry for 2D bulk system. Total energy for 2D bulk is for five atoms basis while for nanoribbon number of atoms is fifteen. That is why total system energy is higher in nanoribbon case.

Electron density obtained from SCF calculation was used for another round of calculation for finding energy levels for each point of a densely sampled BZ. We used 64x64x1 K-grids for BZ sampling using MP methods for 2D bulk and 256x1x1 for nanoribbon. From this calculation, we obtained electronic band structure and electrons occupations for those energy states. we performed band structure calculation for 80 energy levels and obtained Fermi energy value was 0.7179 eV for bulk case and -3.9858 eV for hybrid nanoribbon. Later on, for all other calculations, we adjusted these Fermi energies to 0 eV when necessary for comparison or for transport calculations. From SCF calculation, we constructed band structures and calculated density of states (DOS) of this hybrid system within QE code. For DOS calculation, energy levels are adjusted in such way that Fermi energy becomes 0 eV. Energy spectrum is sampled with a resolution of 10 meV. DOS was used to find quantum capacitance.

5.3. Calculation of Quantum Capacitance

From DFT calculations we calculate quantum capacitance. Quantum capacitance of graphene can be defined as Eq. (5.1).

$$C_Q = \frac{d\sigma}{d\phi_G} \tag{5.1}$$

Here, σ is charge density and ϕ_G is local potential of graphene. If E is the relative energy to Fermi energy than excess charge density (σ) can be calculated as,

$$\sigma = e\int_{-\infty}^{+\infty} D(E)[f(E) - f(E - e\phi_G)]dE \tag{5.2}$$

Here, Fermi-Dirac distribution,

$$f(E) = \frac{1}{\left[\exp\left\{\frac{(E - E_F)}{K_B T}\right\} + 1\right]} \tag{5.3}$$

After taking derivative on excess charge density with respect to graphene local potential Eq. (5.1) yield as,

$$C_Q = e^2 \int_{-\infty}^{+\infty} D(E) F_T(E - e\phi_G) dE \tag{5.4}$$

Here, $F_T(E)$ is thermal broadening function defined as in Eq. (5.5).

$$F_T(E) = -\frac{df}{dE} = \frac{1}{4K_B T} \operatorname{sech}^2\left(\frac{E}{2K_B T}\right) \tag{5.5}$$

Eq. (5.5) will be used for estimating thermal broadening at finite temperature for the calculation of quantum capacitance. However, for low temperatures, calculation becomes far easier. At absolute zero temperature, F_T can be assumed as a delta function and then C_Q will be simply $e^2D(E)$. However, for all numerical calculations in this work we have taken temperature (T) as 300 K and solved the above equation numerically.

5.4. Results and Discussion

For the purpose of the validation of carried computation, we have compared our 2D results in Fig. 5.1, with previously reported DFT calculation of reference in [112] and experimentally measured quantum capacitances data referred in [115]. The first experiment on quantum capacitance of graphene was reported in [114] which was later on substantiated with subsequent

work in [115] shows little off from the analytical model of pristine graphene's quantum capacitance. The reason for this deviation near the charge neutrality point, which is referred in Fig. 5.1 as zero voltage is that in real experiments density of states is non-vanishing at Dirac point, as it is supposed to be for pristine graphene. Due to charge impurity induced states near Dirac point, there is always a finite carrier density which results in non-vanishing quantum capacitance near charge neutrality point. Obtaining vanishing density of states near Dirac point from a DFT calculations largely depends on the choice of different approximations for the exchange correlation and the choice of functions. In Fig. 5.1, our calculation for graphene shows a vanishing density of states near the Dirac point while other DFT calculation in [112] could not. However, away from Dirac point they are within reasonable agreement. Again, this difference is observed due to the choice of DFT functions in different works. For G/Cu two-dimensional system, calculation presented in [27] and in this work agreeably suggest enhancement in capacitance of graphene system in contact with Cu. Experimentally DOS of G/Cu in 2D system has been measured [120] and suggests good agreement with this present work.

In Fig. 5.2, we have shown the DOS calculated for different width of G/Cu-NR from 1 nm to 5 nm. For the purpose of comparison of different DOS, we have forced charge neutrality point to be at 0 V in Fig. 5.2. Since we are comparing G/Cu-NR of different lateral sizes, we have shown DOS in per unit area. DOS of graphene increases in contact with copper and it increases with decrease of width. In all of the cases, we have found a non-vanishing DOS near the Dirac point, which is $E\text{-}E_F=0$ in Fig. 5.2 except for graphene (G) in 2D. As G/Cu-NR width increases DOS becomes more like a 2D G/Cu system. Without any curve fitting, we have calculated quantum capacitance using this DOS which is from the direct result of DFT calculation. Calculated

quantum capacitance is shown in Fig. 5.3. For all G/Cu-NR under this study, we have found non-vanishing quantum capacitance because of non-vanishing DOS near Dirac point. With increase of graphene potential, quantum capacitance also increases as more charge accumulates in graphene layer. In other words, in all cases quantum capacitance is minimum near Dirac point. For all G/Cu-NR, it is also common to find asymmetry of quantum capacitances in positive biasing and negative biasing. This asymmetry is also observed in experiments [114] and it is due to the shift of charge neutrality point. At different widths of G/Cu-NR, this shift is different and that is why magnitude of asymmetry is also different. Width 3 nm and above shows capacitance below 30 $\mu F/cm^2$ near charge neutrality point while for smaller width quantum capacitance increases significantly.

The 3 nm width is critical in applications using G/Cu hybrid structure. For energy storage devices, higher specific quantum capacitance is desirable. In contrast to this, for interconnect application, lower specific quantum capacitance is preferable to reduce *RC* delay inside the chip. Because of extensive computational resource requirement, we limited this study up to 5 nm. However, from Fig. 5.3 it is apparent that as the width increases, quantum capacitance approaches towards its 2D values. To be specific, quantum capacitance for 5 nm wide G/Cu-NR shows almost a similar pattern like 2D G/Cu. Only difference is observed in the vertical shift. The most important insight from Fig. 5.3 is that, with the decrease of G/Cu-NR width, quantum capacitance per unit area significantly increases. Reason of this increase in quantum capacitance with decrease in width can be explained with the help of macroscopically averaged potential at the Cu and graphene junction.

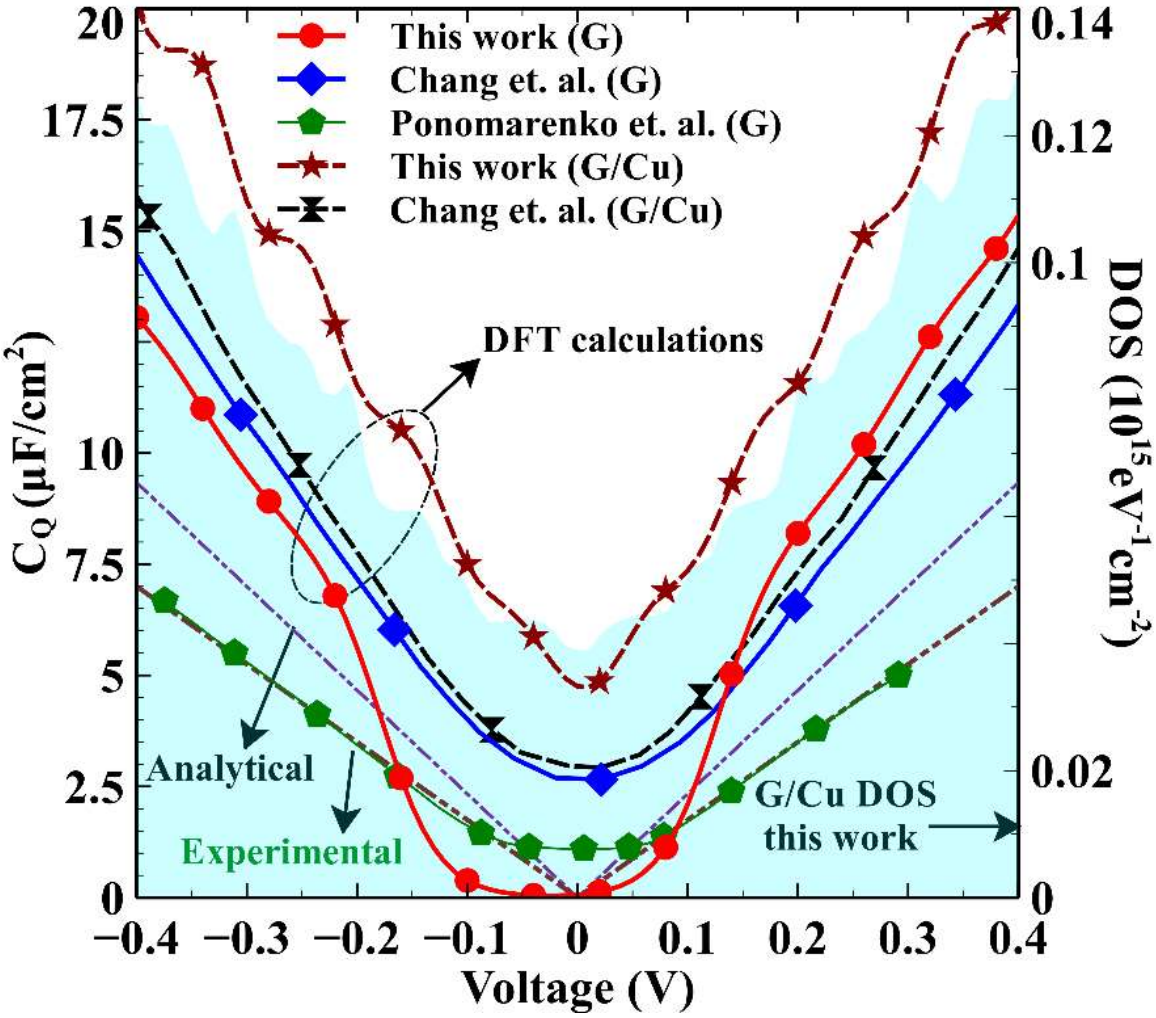

Figure 5.1: Comparison of quantum capacitances (C_Q) of graphene (G) and graphene on copper (G/Cu) in 2D systems in between this work and earlier works. Shaded area is DOS of G/Cu in 2D (scale is in the right side of this plot).

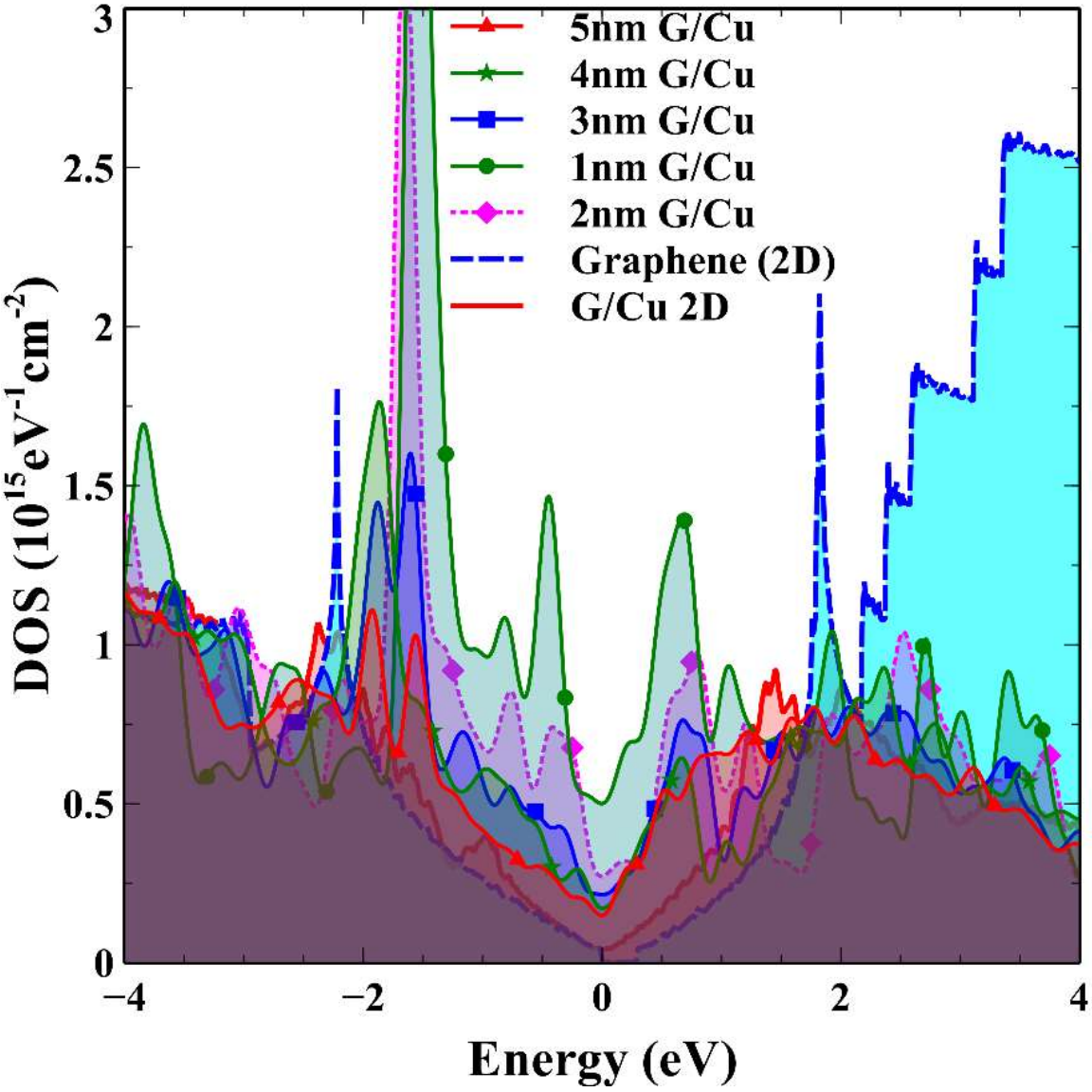

Figure 5.2: Density of states of graphene (G) and graphene/copper nanoribbon (G/Cu-NR) for various width are shown for comparison. Scales for all these subfigures are different.

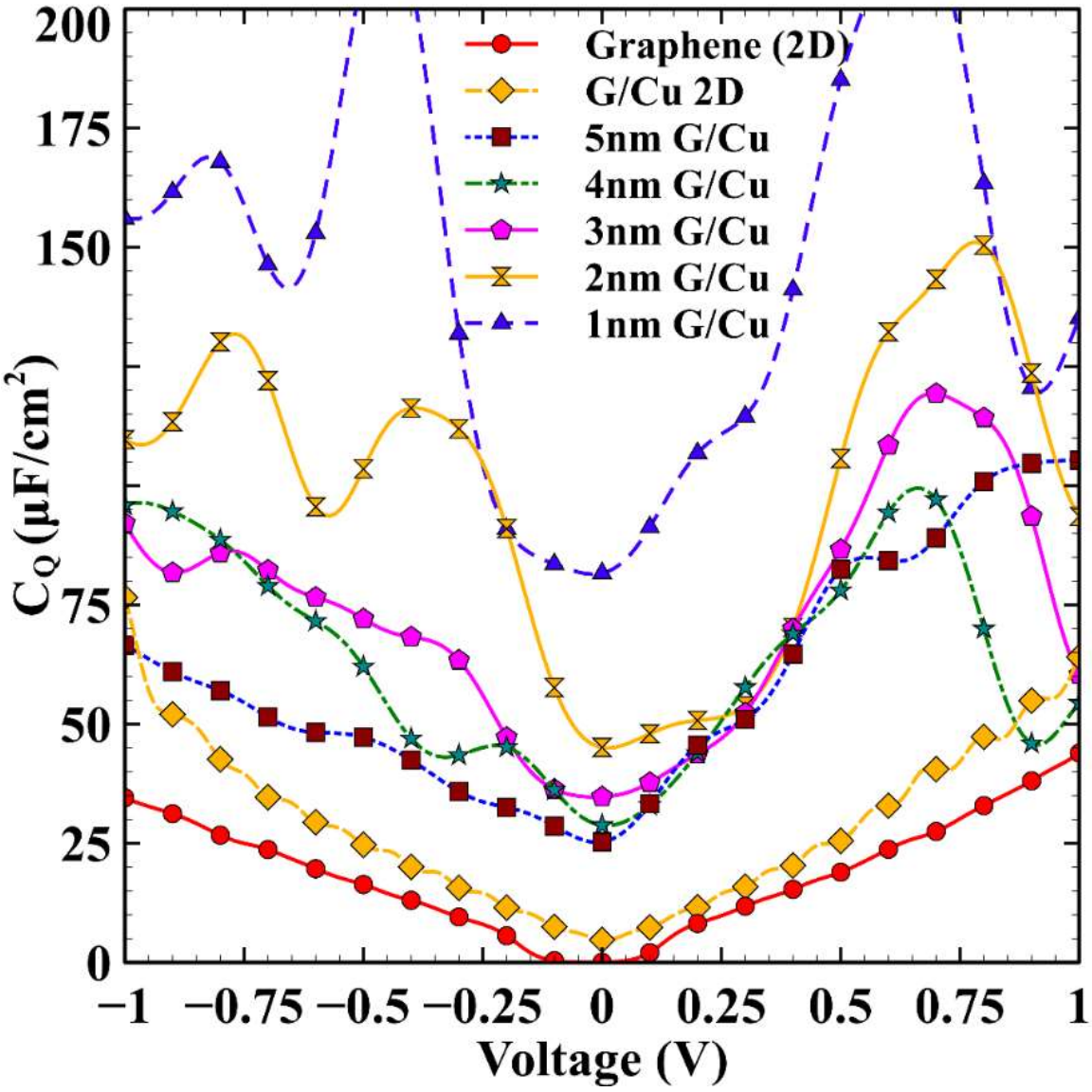

Figure 5.3: Calculated quantum capacitances at different potentials of graphene.

In Fig. 5.4 and Fig. 5.5, macroscopically averaged plane potential of two cases has been presented, one in 2D case and the other one in 1D case. Three layers of copper and top graphene layer are shown in inset of Fig 5.4. Although potential plot is in voltage unit but barrier height is shown in eV unit. For a 2D case, built-in junction potential height is 0.263 eV where for 1nm case it is 0.164 eV. This height of built-in junction potential is basically a potential wall for electrons and it controls the tunneling of electrons from a Cu layer to a graphene layer. As height lowering is happening for thinner G/Cu-NR since more electrons are tunneling from electron rich side (Cu) to the graphene. Since quantum capacitance (C_Q) is directly proportional to the electron DOS, we see an increase of C_Q with the decrease in width. Further in Fig. 5.4 and in Fig. 5.5, beyond the graphene layer, we have plotted macroscopically averaged plane potential up to 20 Å of vacuum. Finite slope in a potential in vacuum suggests existence of a macroscopic electric field. Reversal of field direction is related with the critical width 3 nm. Width above 3 nm slope of potential towards vacuum is positive. Slope of potential in vacuum decreases with the decrease in width and below 3 nm it becomes negative.

5.5. Quantum Capacitance Modeling:

For disorder free intrinsic graphene, 2D free electron gas model predicts quantum capacitance to be [121],

$$C_Q = \frac{2e^2 k_B T}{\pi(\hbar v_F)^2} \ln\left[2\left(1 + cosh\frac{eV_{ch}}{k_B T}\right)\right] \tag{5.6}$$

where $\hbar$ is reduced Planck constant, e is the magnitude of electronic charge, T temperature and k_B Boltzmann constant. Fermi velocity $v_F \approx 10^6 m/s$. $V_{ch} = E_F/\mathrm{e}$, is graphene potential. At very low

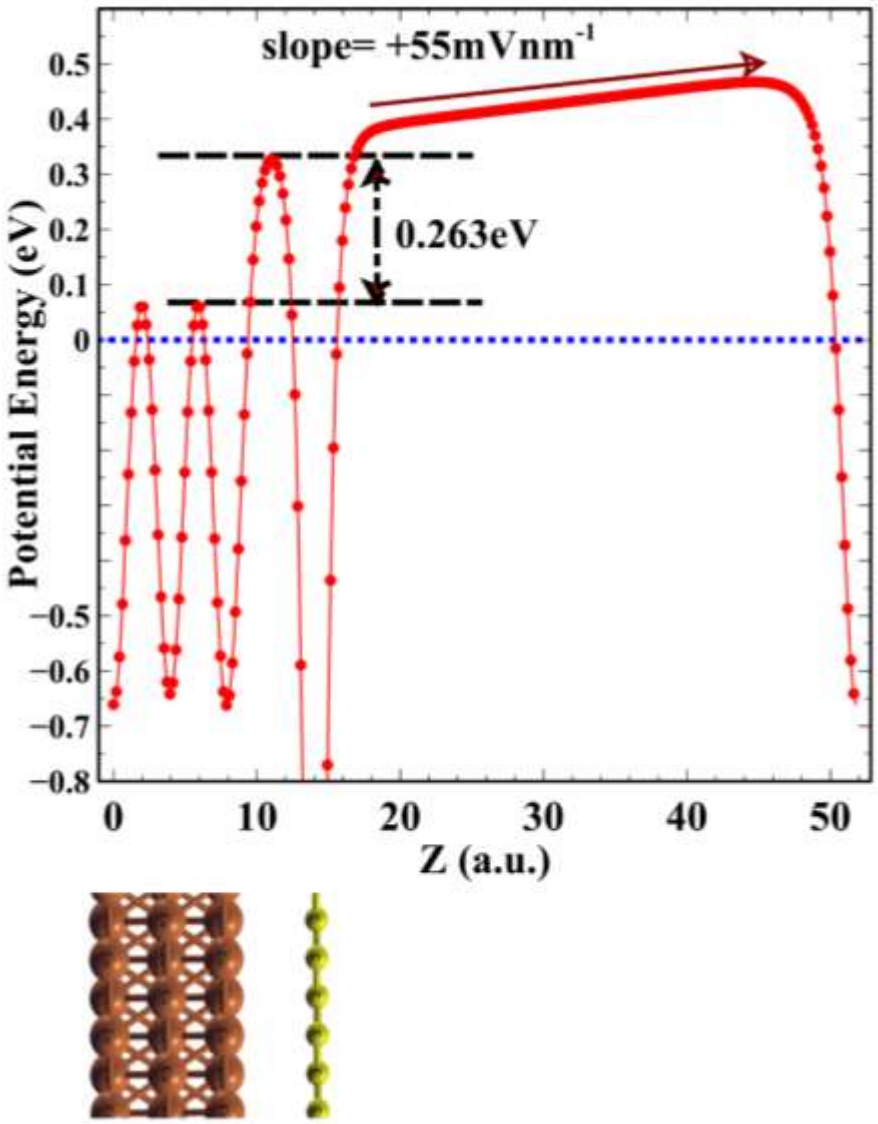

Figure 5.4: Macroscopically averaged plane potential at graphene-copper junction of 2D. Note: 1 atomic unit (a.u) =0.529 Å.

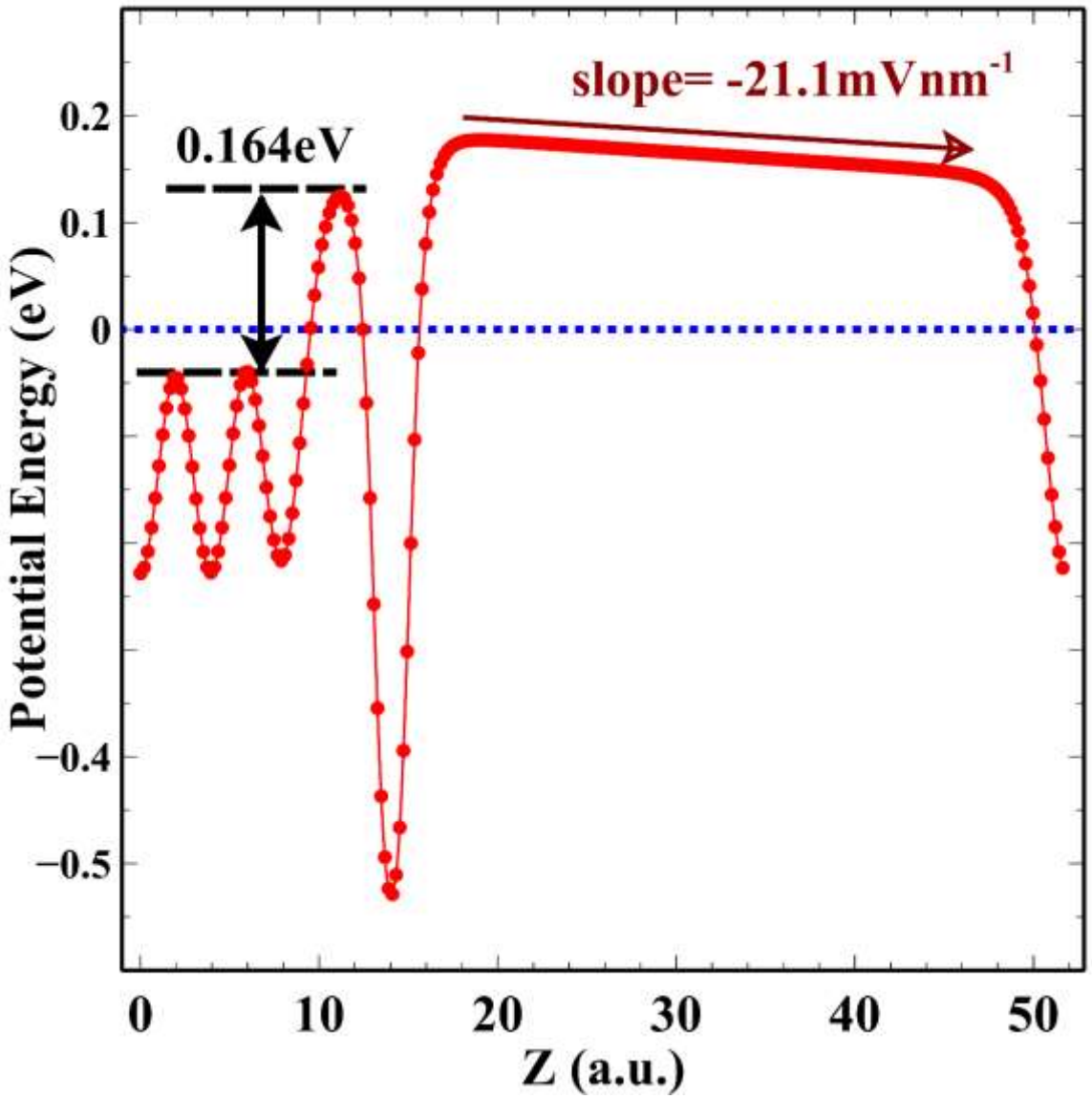

Figure 5.5: Macroscopically averaged plane potential at graphene-copper junction of 1nm width G/Cu-NR. Note: 1 atomic unit (a.u) =0.529 Å.

temperature $V_{ch} \gg K_B T$ and above equation reduces to, $C_Q \approx \frac{2e^2}{\pi(\hbar v_F)^2}(\mathrm{eV_{ch}}) = \frac{2e^2}{\sqrt{\pi}\sqrt{\pi}\hbar v_F \hbar v_F}(\mathrm{eV_{ch}}) = \frac{2e^2}{\sqrt{\pi}\hbar v_F}\frac{\mathrm{eV_{ch}}}{\sqrt{\pi}\hbar v_F}$. Since carrier density depends on gate voltage by [122],

$$n_G = \left(\frac{\mathrm{eV_{ch}}}{\sqrt{\pi}\hbar v_F}\right)^2 \tag{5.7}$$

Then quantum capacitance can be expressed in terms of charge density as, $C_Q \approx \frac{2e^2}{\sqrt{\pi}\hbar v_F}\sqrt{n_G}$. Including charge transferred from Cu to graphene (n_T) ,we can obtain,

$$C_Q \approx \frac{2e^2}{\sqrt{\pi}\hbar v_F}\sqrt{|n_G| + |n_T|} \tag{5.8}$$

We are not considering charge impurities for a pristine system we did not include charge impurities induced carriers. Here non-vanishing quantum capacitance originates from the carrier tunneling from copper to graphene after crossing built-in junction potential wall. In presence of n_T, quantum capacitance is non-zero even at zero gate bias. we have fitted DFT data with this above equation to explain results with the help of few fitting parameters.

Graphene is described by an effective field theory. The Fermi velocity in graphene increases when electron-electron (e-e) interactions increase [123]. Fermi velocity modulation ranges from 300% of Dirac fermion velocity ($3\text{x}10^6$ m/s) [124] to 85% ($0.85\text{x}10^6$ m/s) [125] from the strongest e-e interaction to the weakest one. Fermi velocity modulation was studied by placing metal planes close to graphene which is actually a process of weak e-e interactions [126, 127]. Because of Cu planes near to graphene, Fermi velocity modulation is happening in this G/Cu-NR structure. Decrease in Fermi velocity is eventually increasing DOS as well as quantum capacitance as it is shown in previous equation of C_Q. Now naturally a question comes how this

decrease in Fermi velocity is happening. By placing metal planes, we are allowing electrons to tunnel from a metal plane to a graphene plane. This phenomenon increases carrier density in graphene plane and contributes to the weakening of e-e interaction. This weakening is causing Fermi velocity to decrease. From the observation of DFT calculation, we can phenomenologically say that with decrease in width, e-e interaction is getting weaker. Weaker e-e interaction is causing Fermi velocity go further down. As the potential plot (Fig. 5.5 and Fig. 5.6) at the junction of graphene and copper also suggests this fact of potential barrier lowering argument. Therefore, with decrease of G/Cu-NR width potential barrier lowers which eventually causes electron tunneling probability to increase. To incorporate Fermi velocity modulation, we have considered the following relation,

$$\nu_F = \nu_{DF}\nu \tag{5.9}$$

Where ν_{DF} is velocity of Dirac fermion (10^6 m/s). Fermi velocity (ν_F) depends on a velocity modulation parameter (ν) which varies with the width of G/CuNW. Graphene's intrinsic carrier density (n_G) can be obtained as follows,

$$n_G = \left(\frac{\mathrm{eV_{ch}}}{\sqrt{\pi}\hbar\nu_F}\right)^2 \tag{5.10}$$

Extra carrier density (n_T) can be obtained from following equation,

$$n_T = n_0\left(V_{ch} - V_{shift}\right)t \tag{5.11}$$

Here n_0 is carrier density at zero bias due to built-in potential, V_{shift} is shift in charge neutrality potential, t is another fitting parameter which depends on the width. DFT results can be explained with the above-mentioned equation with these four parameters (ν, V_{shift}, t, n_0).

Table 5.1: Model parameters for different sizes of G/Cu

	n_0 (10^{15}/cm^2)	v	V_{shift} (V)	t	Error (r.m.s.)
2D	0.0393	0.70	-0.8	0.0784	4.50
5nm	0.1480	0.49	-0.4	0.5625	3.44
4nm	0.1704	0.45	-0.45	0.4356	2.52
3nm	0.2143	0.41	0.85	0.1600	8.51
2nm	0.2711	0.35	0.56	0.2916	29.91
1nm	0.4990	0.25	0.45	0.2116	17.00

Note: v and t are unit less parameters**.** Error is in the unit of capacitance. Width less than 3 nm shows Vshift value positive and width above 3 nm shows negative value of $V_{shift.}$

Velocity modulation parameters are well understood by e-e interaction weakening effect. Shift in charge neutrality is due to the built-in potential which is due to the work function difference. Work function varies with the varying width of G/Cu-NR. Offset charge carrier at charge neutrality point is also understood by zero-biased DOS which is directly calculated from the DFT. C_Q model parameters of different widths of G/Cu-NR are as in Table 5.1.

From this table, it is also apparent that 3 nm is a crucial width because v_{shift} reverses its sign here. Bellow 3 nm it is positive and above it is negative. There is a negative correlation in between n_0 and v. With increase of width n_0 decreases, however, v decreases. In Fig. 5.6, we present validity of above model with the deviation error from DFT calculation. Error bar shows the model error. Error increases significantly for 1nm and 2 nm cases, i.e., below 3nm. For other geometries, error is minimal (<5%). This model is limited up to a voltage 0.3V above or below 0V. In high biasing regime, linearity of band structure is not preserved. This is why in high biasing regime, fitting to any physics based model is not possible except in higher order polynomial

fitting. Error for G/Cu-NR C_Q is less than 5% for 3~5 nm cases, however, it increases for 2 nm and 1 nm cases. This model predicts C_Q with increasing accuracy for wider G/Cu-NR. With this limitation, still this model can be used as a quick estimation of C_Q for this technologically very important structure in cases of width ≤5 nm. As mass production of electronic chip technology is approaching to 7 nm node, the choice of 5 nm in this work is very relevant and significant.

The enhancement of quantum capacitance is a desirable phenomenon for energy storage devices, however, its promises are limited for interconnect applications. For interconnect, increased quantum capacitance reduces the overall capacitance as it is in series with the electrostatic capacitance $\left(C_{eqv}^{-1} = C_E^{-1} + C_Q^{-1}\right)$. Since the large overall capacitance (C_{eqv}) increases signal transmission delay $(\tau \propto RC)$, this enhanced quantum capacitance needs to be compensated with a very small electrostatic capacitance having a low-k dielectric for a practically allowed signal transmission delay. Hence, a practical application of G/Cu interconnect with width less than 3 nm is not that desirable. On the other hand, this unique combination of materials is very promising for energy storage devices below this 3 nm critical width. For energy storage devices where increasing quantum capacitance is the goal, it may be desirable to use several nano-strips running in parallel instead of a wide one. In contrast, for electronic interconnect application where the goal is to reduce capacitance it is desirable to use wider nanowire and this conflicts with scaled-down technology nodes. In this case, a trade-off in between nanowire width and allowable capacitance is required.

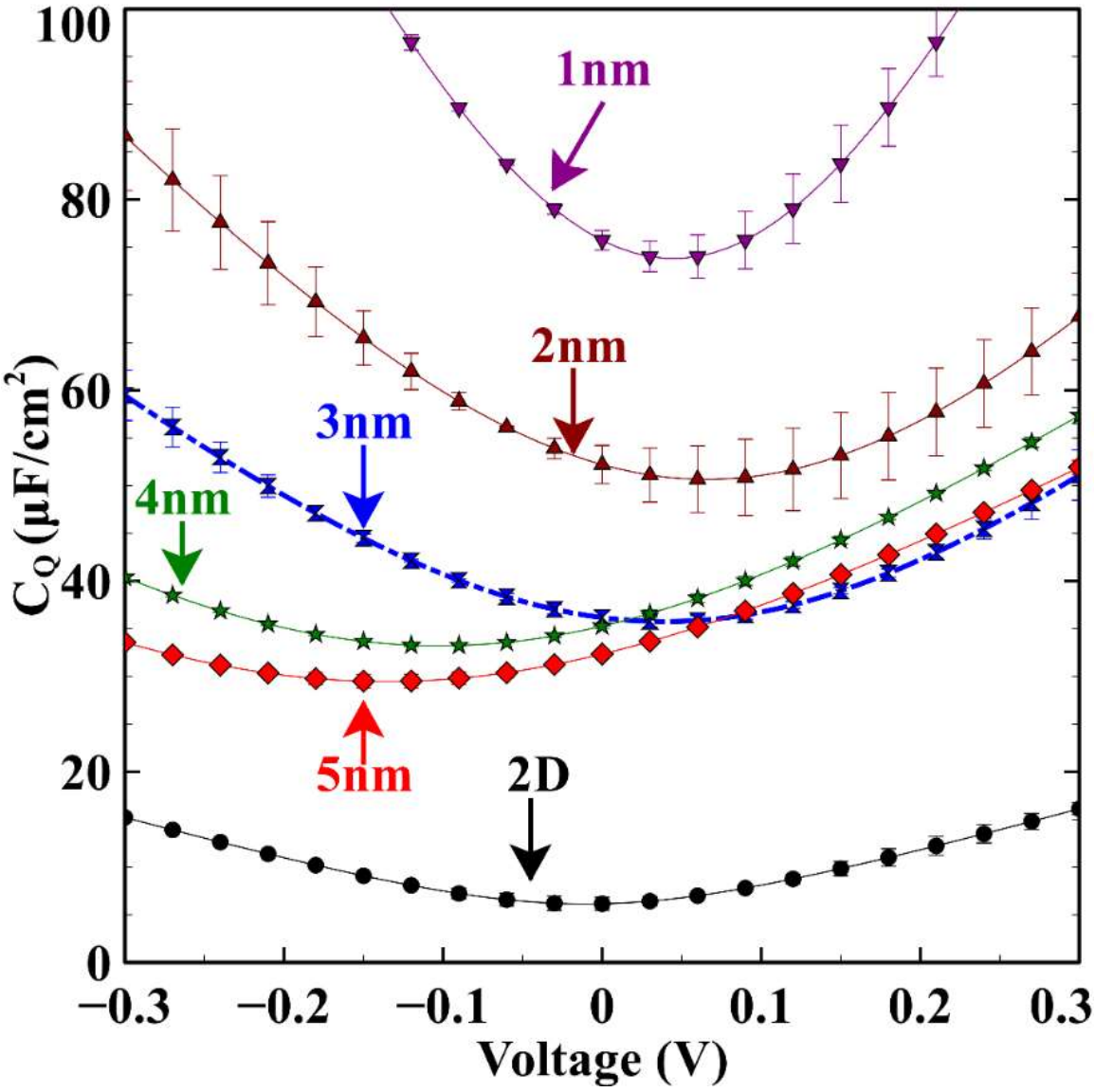

Figure 5.6: Quantum capacitance calculated from the proposed model.

5.6. Conclusion

Graphene on copper is a promising hybrid heterostructure material for electronic applications because of its enhanced electro-thermal conductivity. In this work, we studied electronic structure and quantum capacitance of a hybrid G/Cu nanoribbon using density functional theory (DFT). We have studied the possible application of this nanostructure for interconnect technology and have addressed its alternative applications for energy storage devices. Possible application of this nanostructure largely depends on the width of the hybrid G/Cu nanoribbon structure. We have found a critical width, 3 nm below which quantum capacitance behavior changes drastically and favors energy storage devices. The width above 3 nm favors use as an interconnect. Quantum capacitance which is proportional to electron density of states, increases as the width decreases. Reason for the decrease is due to the lowering of junction potential barrier as the width decreases and as a consequence electron tunneling probability from Cu to graphene increases. We have explained the reason of this enhancement with Fermi velocity modulation which is as a consequence of increased carrier density and weak electron-electron interaction in graphene layer. We have also proposed an analytic model which estimates quantum capacitance near the charge neutrality point. The calculation will help in finding quantum capacitance and choosing the critical device dimension for a given application. The proposed analytic model is semi-empirical in nature and will be useful in quick estimation of quantum capacitance of this nanomaterial system.

CHAPTER 6
APPLICATION DEMONSTRATION IN HYBRID CMOS IC

6.1. Introduction

The application of an interconnect is to connect different devices as a signal pathway. In this chapter, an application demonstration of emerging interconnects has been presented in hybrid CMOS IC. Interconnects discussed in this dissertation have been placed in between a CMOS inverter pair for the purpose of studying interconnect performances. For CMOS, BSIM 7.0 level model have been used along with SPICE compatible model for interconnects. Beside SPICE compatible model finite difference time domain (FDTD) method has been implemented for delay analysis. The purpose is to demonstrate the proposed interconnects and compare with current Cu/low-k technology.

6.2. Circuit

In Fig. 6.1 a CMOS inverter pair has been connected with an interconnect of 1 μm long. SPICE based RLC model has been used to model the interconnect. Here 1-10 GHz square pulse with 50% duty cycle has been used as input to the first inverter. In Fig. 6.1 this input node has been named as node “A”. Node “B” is the output of the first inverter. As signal travels through the interconnect, after a certain delay it will reach the input of the second inverter at node “C”. Node “D” is the output of the second inverter. As signal travels from node “A” to node “D” it accumulates three delays. First delay is associated with the inverter on the left. This is because of CMOS gate switching delay. Second delay, is due to the interconnect in between node “B” and “C”. Third delay is due to the CMOS gate switching delay of the second inverter. In this chapter,

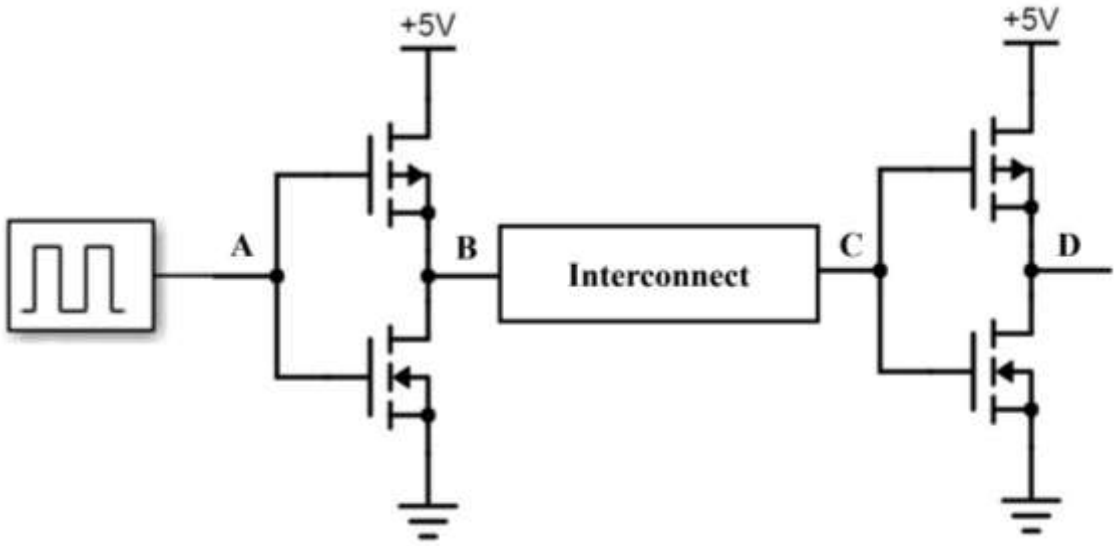

Figure 6.1: Inverter pair with an emerging interconnect in between.

we will focus on the delay associated in between node “B” and “C” which is due to the interconnect. Spice compatible model parameters for MOSFET used in this chapter have been obtained from [128]. Few key parameters for NMOS and PMOS are listed in the table 6.1 and 6.2 bellow,

Table 6.1: NMOS model parameters

Parameters (NMOS)	Value
Gate Width (w)	0.5 µm
Gate length (l)	0.5 µm
Gate oxide thickness (t_{ox})	13.9 nm
Temperature (T)	300 K
Threshold voltage (VTN0)	0.591 V
Channel Surface doping concentration (NCH)	$1.7x10^{17}$ cm^{-3}
Drain/Source Junction Depth (XJ)	150 nm
Drain/Source sheet Resistance (RSH)	84 Ω/square

Table 6.2: PMOS model parameters

Parameters (PMOS)	Value
Gate Width (w)	1.0 µm
Gate length (l)	0.5 µm
Gate oxide thickness (t_{ox})	13.9 nm
Temperature	300 K
Threshold voltage (VTP0)	-0.92 V
Channel Surface doping concentration (NCH)	1.7e17 cm^{-3}
Drain/Source Junction Depth (XJ)	150 nm
Drain/Source sheet Resistance (RSH)	107.2 Ω/square

6.3. Interconnect parameters

Since, all the proposed interconnects will be compared with the current interconnect technology it is necessary to discuss the electrical parameters of Cu. Resistance, R, of Cu can be obtained from the fundamental definition of resistance using the following equation,

$$R = \frac{\rho_{cu} L}{WH}. \tag{6.1}$$

Where, ρ_{cu} is the resistivity of Cu and L, W and H are the length, width and height of the interconnect. Bulk resistivity of Cu is 1.76 $\mu\Omega$-cm [101]. However, as Cu interconnect width (W) becomes less than 100 nm, resistivity deviates from its bulk value. From the Cu resistivity scaling law [101], we have calculated, the resistivity of Cu as shown in table 6.3. This scaling law takes the Cu grain boundary scattering and the surface scattering into account in calculating the most accurate values for Cu resistivity.

Table 6.3: Resistivity of Cu

Cu Interconnect width, W, (nm)	Cu Resistivity, ρ_{cu}, (μΩ-cm)
50	2.2
10	17.6
5	35.2

Using Eq. (6.1) with Cu resistivity value from table 6.3, we have calculated the resistance of Cu interconnect for delay study as described in Fig. 6.2. Inductance and capacitance (line to ground) of a Cu line can be obtained from Eq. (6.2) and Eq. (6.3) respectively [129, 130].

$$L = \frac{\mu_0 L}{2\pi}\left[ln\left(\frac{2L}{W+H}\right) + \frac{1}{2} + \frac{0.22(W+H)}{L}\right] \tag{6.2}$$

$$C = \epsilon\left[\frac{W}{H} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77}\left(\frac{H}{H+4.53H}\right)^{0.07}\right] \tag{6.3}$$

Where in Eq. (6.2), μ_0 is the magnetic permeability of free space. In Eq. (6.3), ϵ (=2.2) is dielectric permittivity of ILD, s is the spacing between two interconnect which is 100 nm, h is the distance between interconnect center and the ground plane. Here, we took h to be 200 nm. In table

6.4, all the interconnect parameters have been tabulated from the all previous chapters along with Cu. For the purpose of comparison all the interconnects have been taken unity aspect ratio (*W*=*H*) and the same dimension. This is why instead of SWCNT, we will be using SWCNT bundle to match width and height of Cu and other interconnect under study. For MWCNT, outer diameter will be matched with the width of the interconnect. SWCNT bundle, MWCNT and G/Cu-NR parameters are obtained from the model discussed in chapters 2, 4 and 5 and also from our earlier work in [51, 92, 131].

Table 6.4: Interconnect parameters for various materials

Interconnect Material	W (=H) (nm)	R (Ω/μm)	L (nH/μm)	C (fF/μm)
Cu	50	8.8	0.0011	0.013
SWCNT bundle		233	0.017	0.025
MWCNT		62.83	0.0704	0.022
G/Cu-NR		6.2	0.0012	0.013
Cu	10	1760	0.0014	0.00894
SWCNT bundle		7000	0.0046	0.03
MWCNT		1433	0.0135	0.012
G/Cu-NR		1173	0.0017	0.00894
Cu	5	14080	0.0016	0.00804
SWCNT bundle		26592	0.0017	0.009
MWCNT		3200	0.08	0.00193
G/Cu-NR		625	0.0019	0.00804

6.4. Delay Analysis

Using the parameters mentioned in tables 6.1, 6.2 and 6.4, we have simulated the circuit show in Fig. 6.2 for various widths of interconnect across different materials.

6.4.1. SPICE Based Model with Lumped RLC

Simple SPICE implementation of the circuit (Fig. 6.1) is as shown in Fig. 6.2 with lump RLC parameters. In this study, length (L) of interconnect is taken as 1 μm. At 1 GHz of operating frequency, width 50 nm there is not that much significant difference in delays across different interconnect materials. However, as interconnect dimension shrink down to 10 nm delay becomes more apparent across materials. As interconnect width becomes as small as 5nm, G/Cu-NR shows the best performance in terms of delay. Fig. 6.3 shows the output signals from various interconnect materials at 10 GHz. In Fig. 6.3, the red marked line is for ideal case where the interconnect block is an ideal interconnect with zero resistivity and infinite capacitance to ground. For better comparison, we have shown the delay associated with different interconnect in Fig. 6.4. Apparently from Fig. 6.4, G/Cu-NR is showing the best performance followed by MWCNT interconnect in terms of delay. From Fig. 6.4, at 2.5 V we have estimated the signal propagation delay for various interconnects.

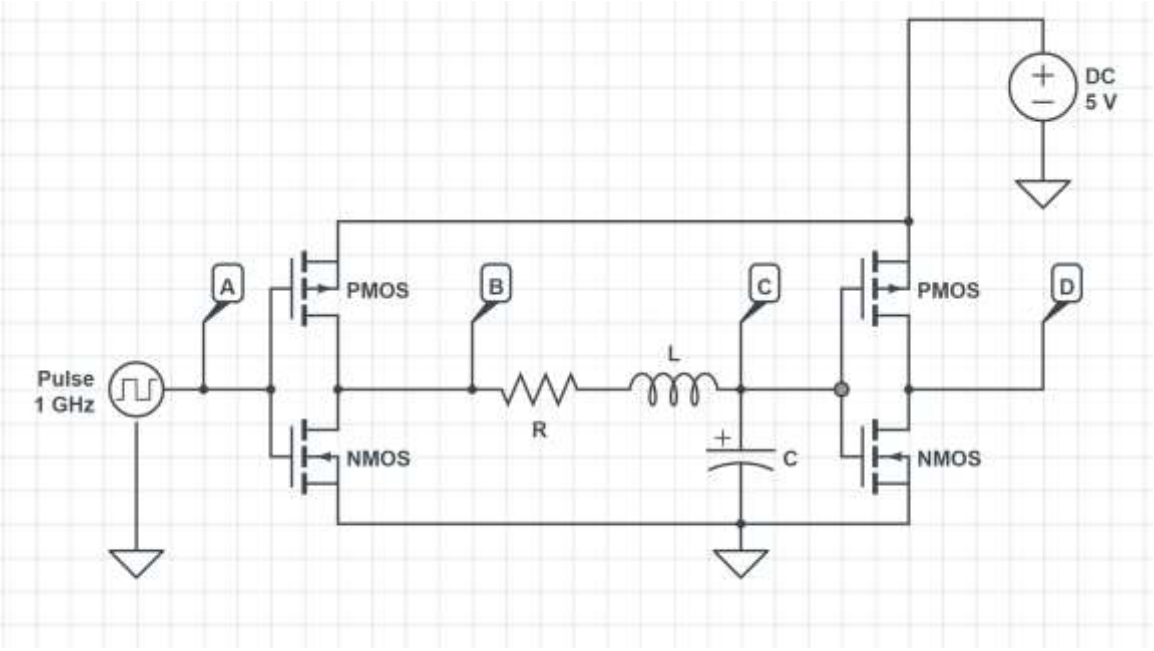

Figure 6.2: SPICE Implementation of CMOS inverter pair with interconnect in between.

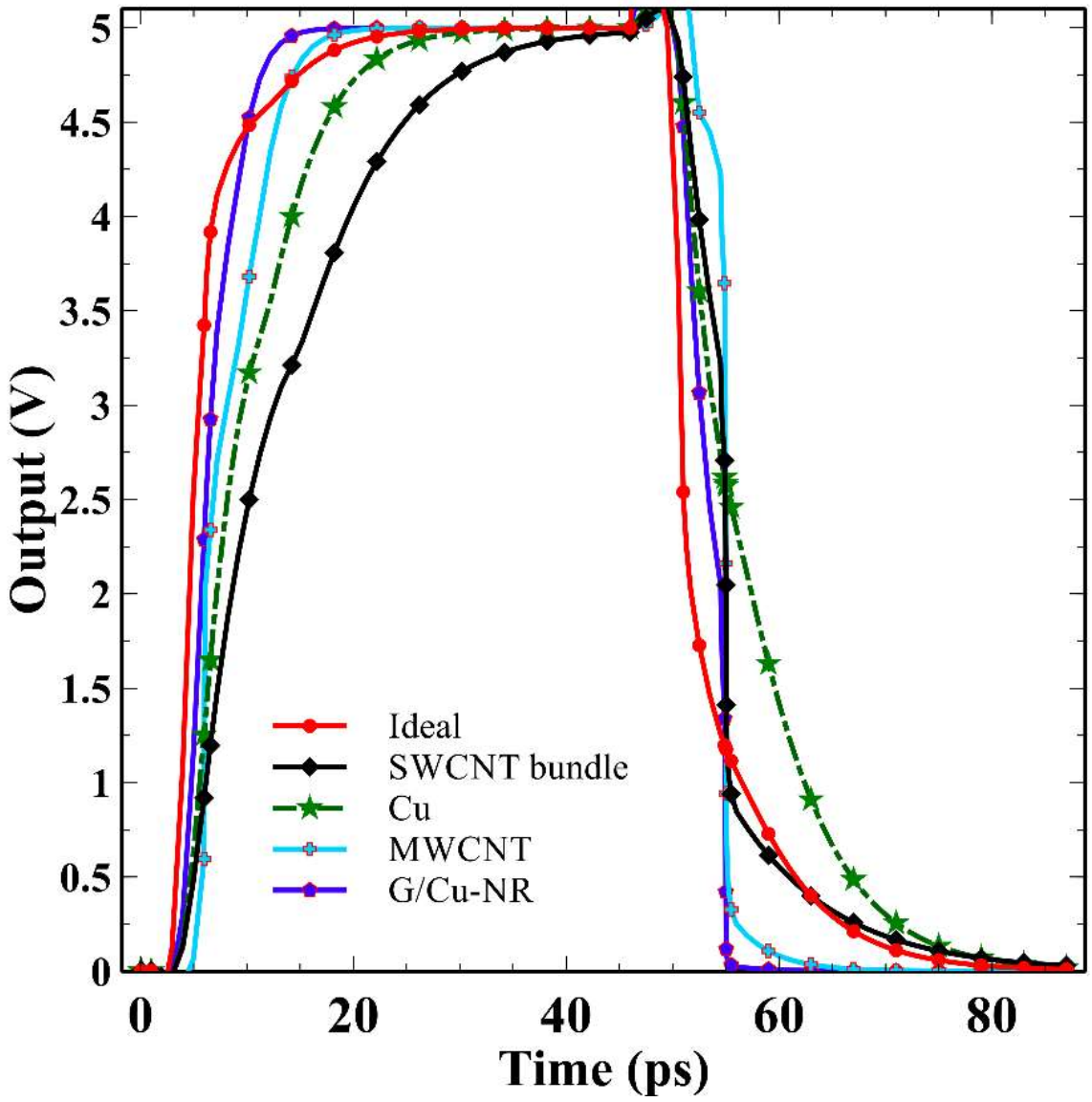

Figure 6.3: Output voltage measured at C, of the first inverter with 1μm long interconnect of various materials.

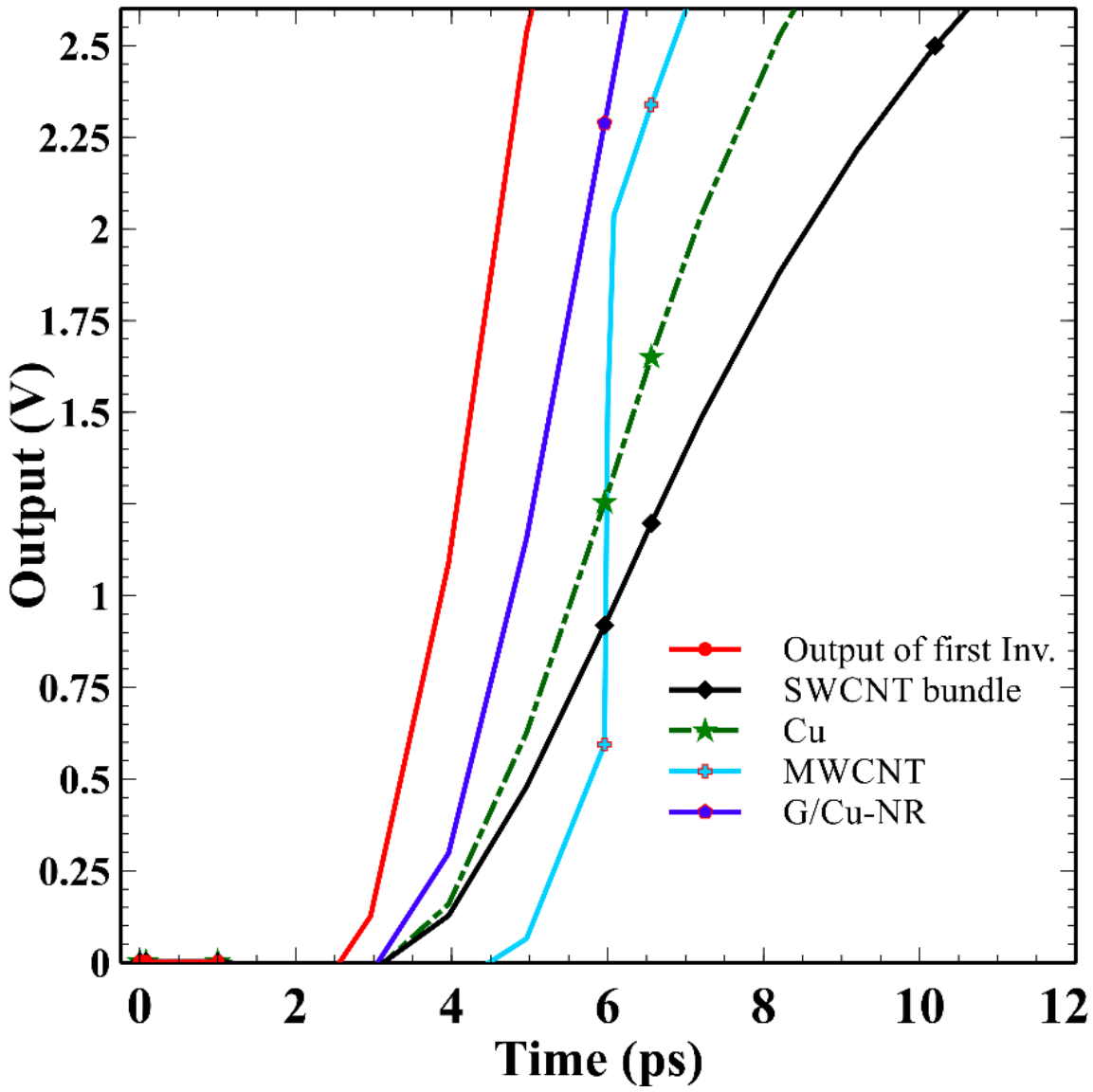

Figure 6.4: Estimation of delay at 2.5V level of signal.

6.4.2. FDTD Simulation for Coupled Interconnect Lines

For accurate analysis of delay and signal propagation coupled interconnect lines need to be considered where beside delay there will be cross talk between interconnect due to the parasitics. In a real IC, two parallel running interconnects will be coupled through the electric field and magnetic field due to the parasitic capacitors and inductors, respectively. This is why SPICE based simple lumped RLC model is not adequate to estimate the signal propagation delay with integrity without a detailed modeling, especially for very high frequency applications. In this section, interconnect delay will be analyzed using the finite difference time domain (FDTD) method [132].

For simulating coupled interconnect lines, we have taken two adjacent interconnect lines as show in the Fig. 6.5. Both of these interconnects are coupled by coupling capacitance (C_C) and mutual inductance (M) of these lines. In Fig 6.5, the end of line is terminated with a R of 50 Ω and a capacitor of 30 fF to simulate the load impedance of the second inverter. The direction of power propagation through interconnect is toward +X direction. In Fig 6.5, length discretization of the interconnect is also shown. At any point of space (X) and time (t), telegraphic equation for transmission line is as following equations,

$$\frac{\partial V(x,t)}{\partial x} + L\frac{\partial I(x,t)}{\partial t} + RI(x,t) = 0 \tag{6.4}$$

$$\frac{\partial I(x,t)}{\partial x} + C\frac{\partial V(x,t)}{\partial t} + GV(x,t) = 0 \tag{6.5}$$

Where, $V(x, t)$ and $I(x, t)$ are the current and voltage at time t and space coordinate x. Since, we are solving coupled interconnect lines problem, here this V and I are a vector with two elements corresponding to the values for the first line and the second line. In Eqs. (6.4) and (6.5),

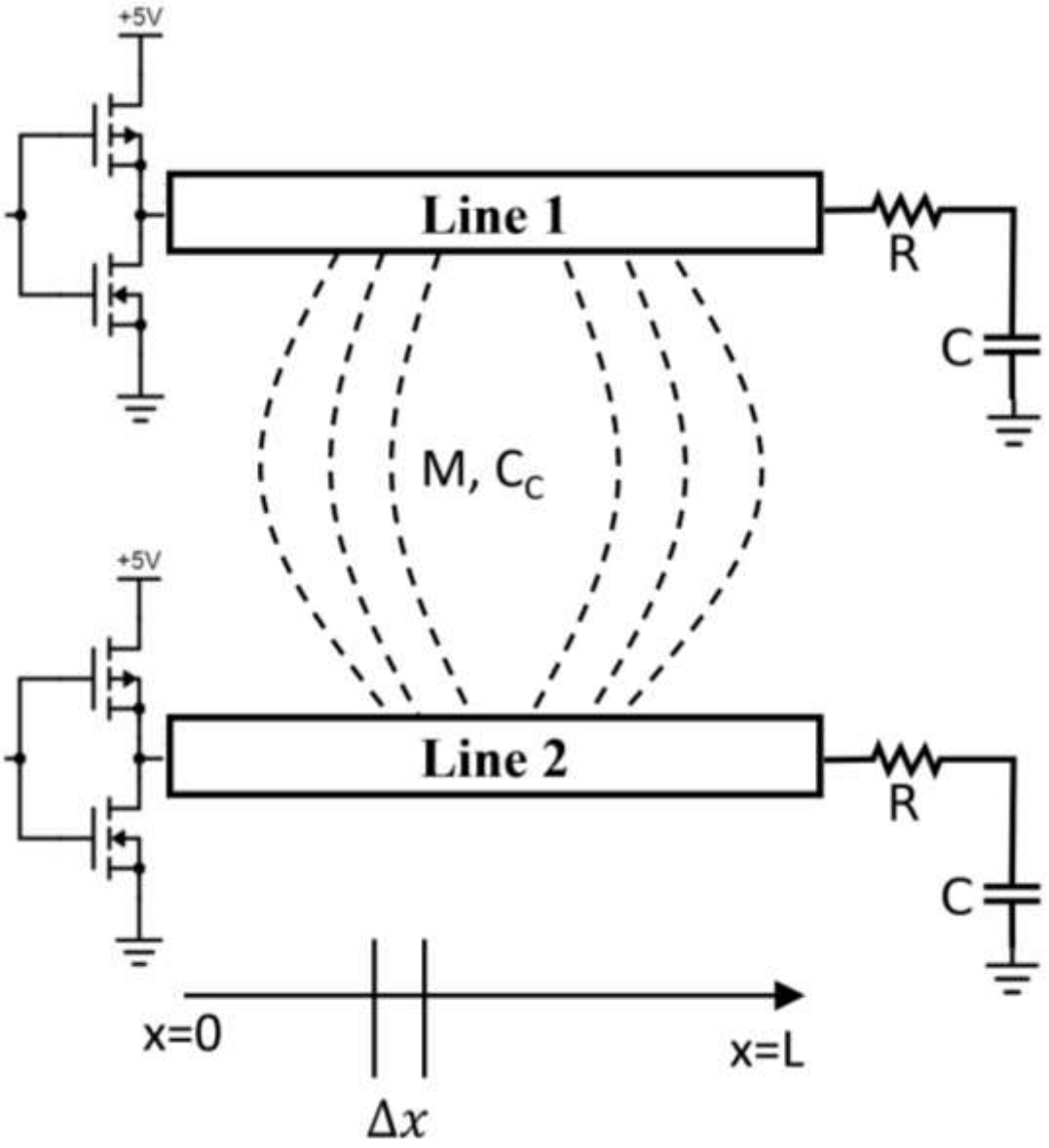

Figure 6.5: Coupled interconnect lines with mutual inductance (M) and coupling capacitance.

R, L, C and *G* are resistance, inductance, capacitance and the conductance of the transmission line. Here, *G* is the conductance in parallel with the capacitance. To solve this coupled equation, we have implemented the FDTD method described in the work of Sharma et. al. [133] using MATLAB scripting. To implement FDTD it is required to discretize Eqs. (6.4) and (6.5).

$$\frac{V_{k+1}^{n+1} - V_k^{n+1}}{\Delta x} + L\frac{I_k^{n+\frac{3}{2}} - I_k^{n+\frac{1}{2}}}{\Delta t} + \frac{R}{2}\left[I_k^{n+\frac{3}{2}} + I_k^{n+\frac{1}{2}}\right] = 0 \tag{6.6}$$

$$\frac{I_k^{n+\frac{1}{2}} - I_{k-1}^{n+\frac{1}{2}}}{\Delta x} + C\frac{V_k^{n+1} - V_k^{n}}{\Delta t} + \frac{G}{2}[V_k^{n+1} + V_k^{n}] = 0 \tag{6.7}$$

These equations have been solved using the mutual inductance (*M*) and the coupling capacitance (C_C) for the length of interconnect lines under consideration, M = 5.6 nH, , C_C = 256 fF [133]. The FDTD calculation steps starts with initializing the discretization parameters. Time step Δt is taken to be 0.01 ps to give better resolution in estimating delays. Space discretization, Δz is taken as 1 nm. Using the methodology reported in [133], Eqs. (6.6) and (6.7) can be further reduced to following equations for the purpose of implementation.

$$V_k^{n+1} = A_1A_2V_k^n + \frac{A_1}{\Delta z}\left[I_{k-1}^{n+\frac{1}{2}} - I_k^{n+\frac{1}{2}}\right], 2 \le k \le Nx \tag{6.8}$$

$$I_k^{n+3/2} = B_1B_2I_k^{n+1/2} + \frac{B_1}{\Delta z}[V_k^{n+1} - V_{k+1}^{n+1}], 1 \le k \le Nx \tag{6.9}$$

Where,

$$A_1 = \left[\frac{C}{\Delta t} + \frac{G}{2}\right]^{-1},\ A_2 = \left[\frac{C}{\Delta t} - \frac{G}{2}\right] \tag{6.10}$$

$$B_1 = \left[\frac{L}{\Delta t} + \frac{R}{2}\right]^{-1},\ B_2 = \left[\frac{L}{\Delta t} - \frac{R}{2}\right] \tag{6.11}$$

Where, R, L, C are resistance, inductance and capacitance for the interconnect in per unit length. These values are tabulated in Table-6.4. The implementation step for FDTD technique is shown in Fig. 6.6. For modeling the source, we have used a pulse source with parameters tabulated in Table 6.5.

Table 6.5: Model of voltage pulse source for FDTD study.

Frequency	1 GHz	10 GHz
Low level voltage	0.1 V	0.1 V
High level voltage	4.9 V	4.9 V
Rise time	10 ps	5 ps
Fall time	10 ps	5 ps
Duration of on time	480 ps	45 ps
Period	1 ns	100 ps

We have calculated signal delays due to the interconnect for the circuit shown in Fig. 6.5. Simultaneously solving for Eq. 6.8 and Eq. 6.9 gives the current and voltages of the whole length of interconnect for each time step. From these information, signal delay has been analyzed. Fig. 6.6 and 6.7 show delay calculated using FDTD technique up to 2.5 V at 1 GHz and 10 GHz. Fig. 6.7 and Fig. 6.8 show the strong frequency dependence in delays. For 1 GHz delay across different material is not as prominent as for the 10 GHz case. At 1 GHz frequency, Cu, SWCNT and G/Cu-NR based interconnects seem better than MWCNT. Delay across these materials are not very different. However, at 10 GHz applications there is significant difference between all these different materials.

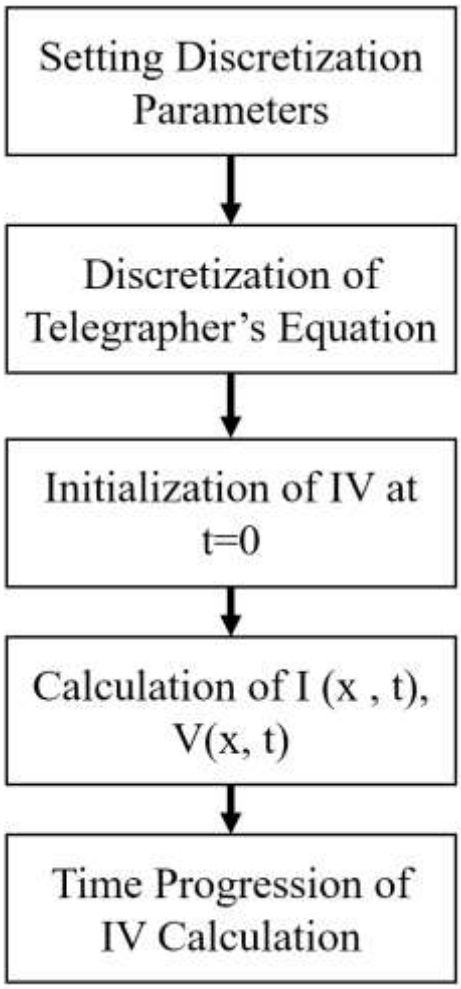

Figure 6.6: Implementation step for FDTD technique.

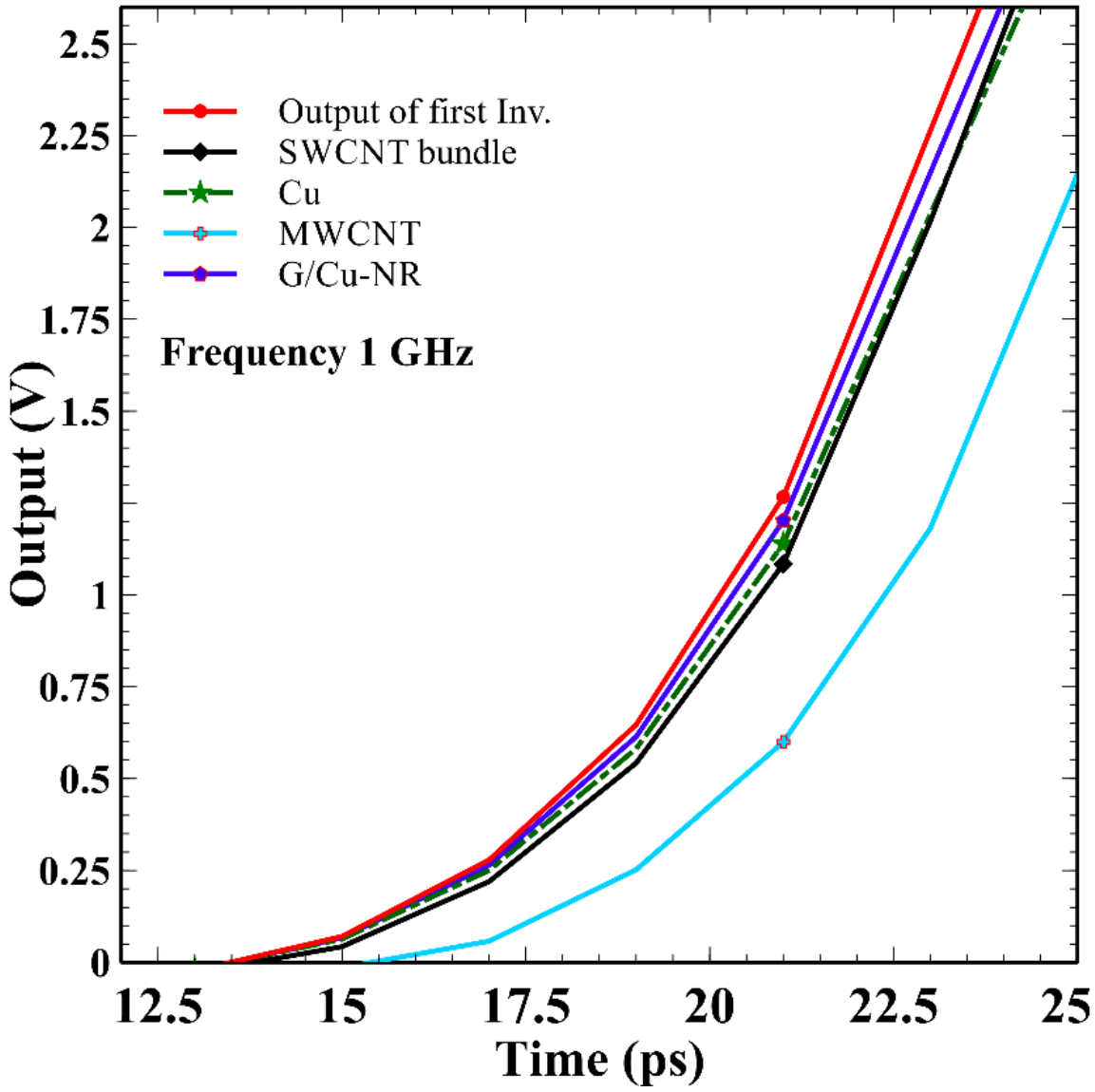

Figure 6.7: FDTD delay of a 1 μm long interconnect with a 5 nm by 5 nm cross section in between pair of inverters at 1 GHz frequency.

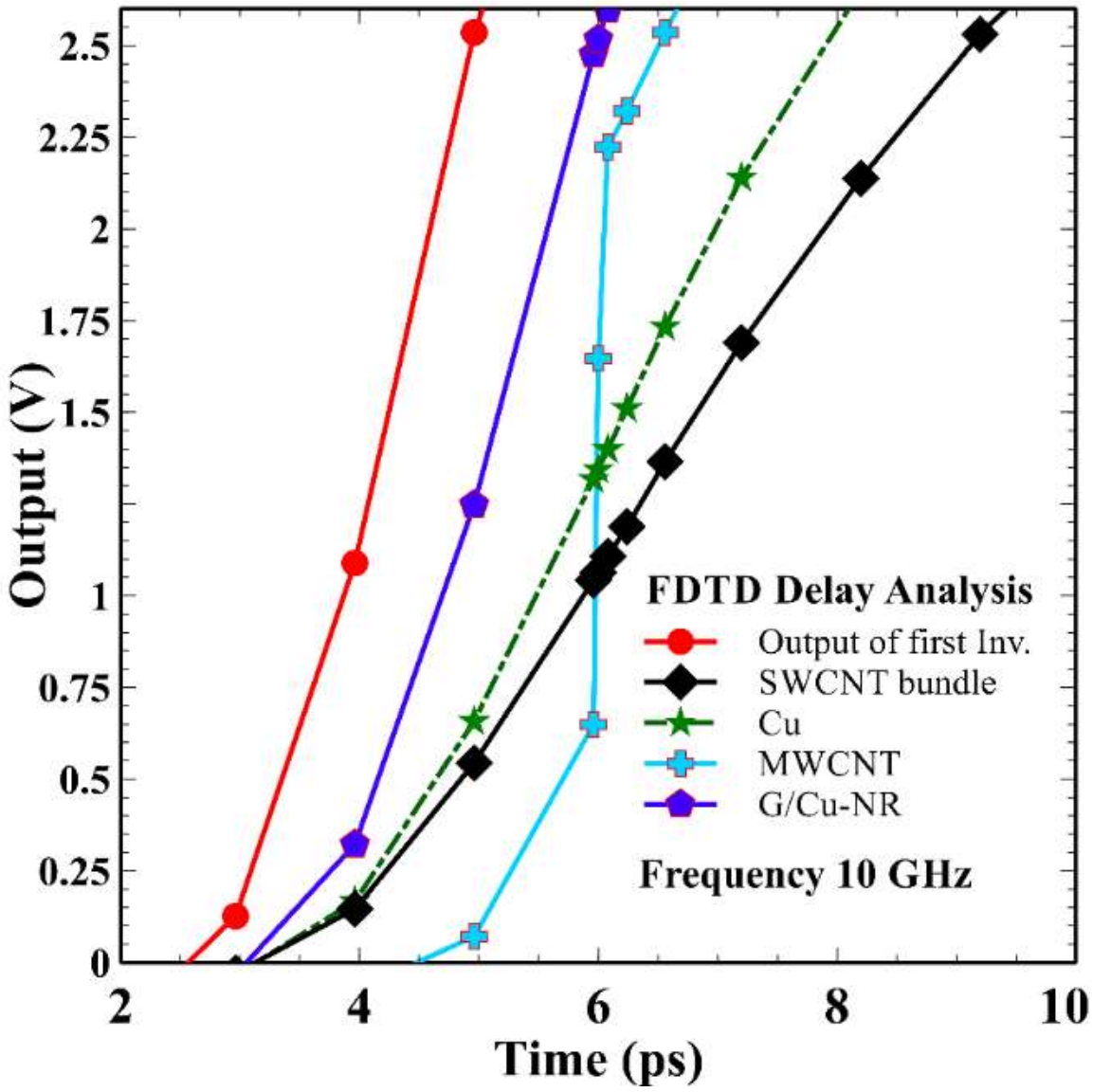

Figure 6.8: FDTD delay of a 1 μm long interconnect with a 5 nm by 5 nm cross section in between pair of inverters at 10 GHz frequency.

Taking the output of the first inverter as reference gives delays shown in table 6.6.

Table 6.6: Delay for different interconnect materials at 10 GHz.

Interconnect Material	Delay (ps) from SPICE	Delay (ps) from FDTD
Cu	3.45	3.60
SWCNT bundle	5.10	4.50
MWCNT	2.00	1.80
G/Cu-NR	1.25	1.30

From table 6.6, it is conclusive that Graphene on Cu nanoribbon (G/Cu-NR) shows the lowest delay of 1.3 ps. Cu performs better with a width more than 10 nm. Because of resistivity deviation from its bulk resistivity due to the grain boundary scattering and surface scattering Cu offers more resistive interconnect and eventually RC delay increase. However, graphene offers more conductive channel to reduce the resistivity and that is why the resistivity scales down drastically from the original Cu resistivity. After G/Cu-NR, it appears that MWCNT performs better followed by Cu. If we take FDTD calculation as more accurate estimation for delay, then G/Cu-NR reduces the delay by ~60% from the Cu interconnect at 10 GHz for a cross section of 5 nm x 5nm. Among all these different variants, SWCNT bundle shows the most of delay.

For the purpose of performance analysis beside the delay it is essential to estimate power dissipation inside the interconnect. Total power is dissipated in the resistive branches of interconnect and is summed over the length. Within FDTD framework, the total dissipated power (P_d) is obtained from the following equation.

$$P_d = \sum_{i=1}^{N} I_i^2 R_i \tag{6.12}$$

Where, N is total discrete section on interconnect, I_i and R_i are the current and resistance of i^{th} resistive branch in the interconnect.

In Fig. 6.9 and 6.10 power is shown for 1 GHz and 10 GHz. Maximum power for 1 GHz is 0.5mW which is approximately 0.72mW for 10 GHz. Although for high frequency peak power dissipation is more but the overall shape for 10 GHz is narrower than 1 GHz. Which implies that area under the curve for 10 GHz will be less than the 1 GHz power dissipation curve. For 1 GHz, power dissipation with time is very similar for different interconnect materials. Interconnects based on Cu, SWCNT, and G/Cu-NR are showing almost similar pattern. Only MWCNT curve is slightly shifted rightward. While the peak for MWCNT is occurring approximately at 30 ps, for rest of the interconnect it is occurring at 26 ps. This observation is in agreement with the signal propagation delay (~4 ps) for MWCNT as shown in Fig. 6.7. Overall power dissipation pattern is similar for all the interconnects studied for 1 GHz. Therefore, concerning the power dissipation G/Cu-NR or any CNT will not give any advantages over Cu based interconnect at this frequency. However, for 10 GHz advantage of using different interconnect materials is visible from Fig. 6.10. G/Cu-NR based interconnect is showing the highest power dissipation peak followed by MWCNT, Cu, and SWNCT bundle. However, the width of this dissipation pattern is not same as before in Fig. 6.9.

For 10 GHz, G/Cu-NR power dissipation is the narrowest followed by MWCNT, Cu and SWCNT bundle based interconnects. This different width and peak for power dissipation pattern makes it challenging to draw conclusion about the best interconnect in terms of power dissipation at 10 GHz. That is why the area under the curve of different power dissipation pattern is taken into account by integrating the power versus time curve. This actually gives better estimation of energy dissipation for different materials based interconnects.

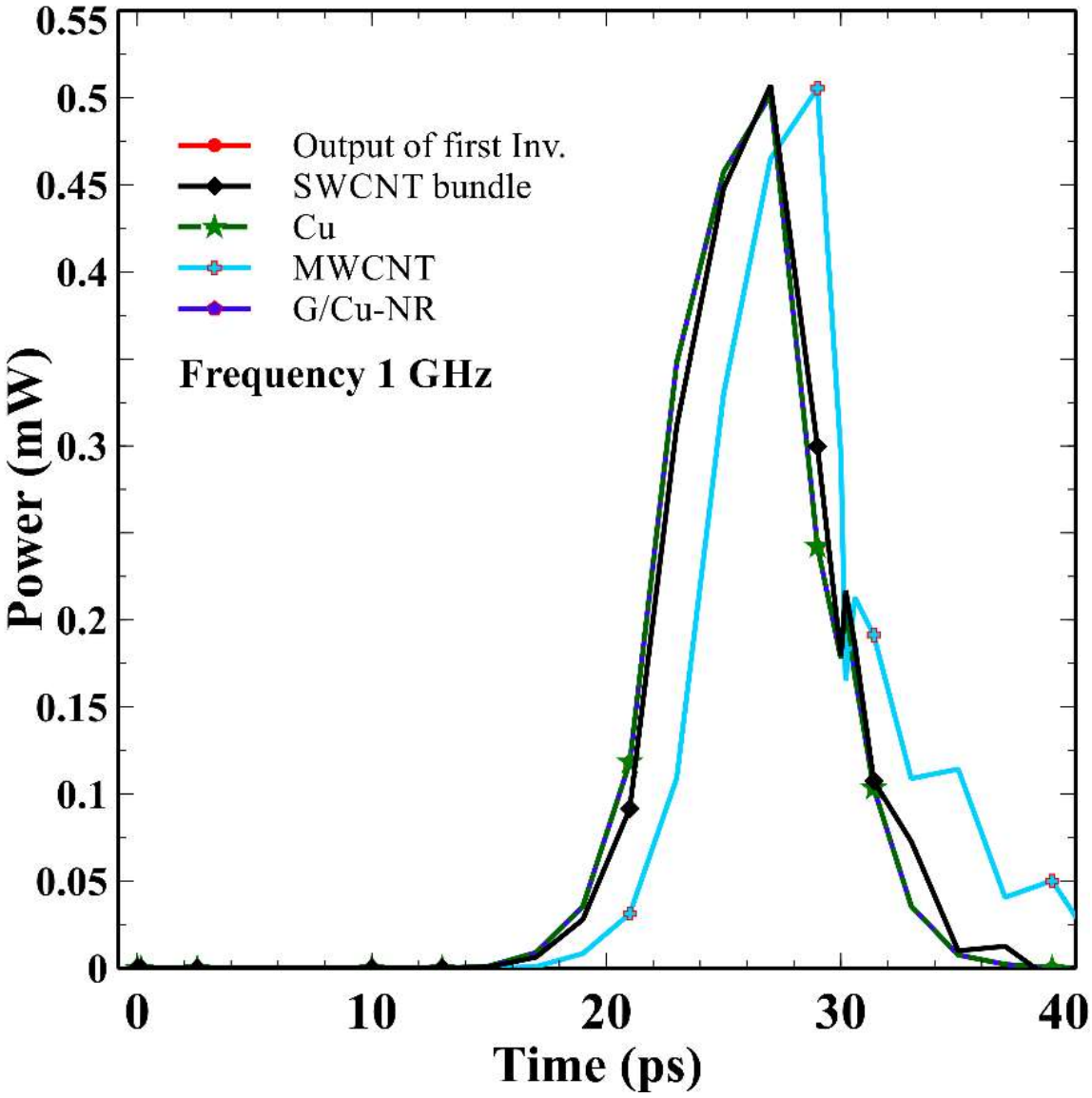

Figure 6.9: Power dissipation with time for different interconnects at 1 GHz.

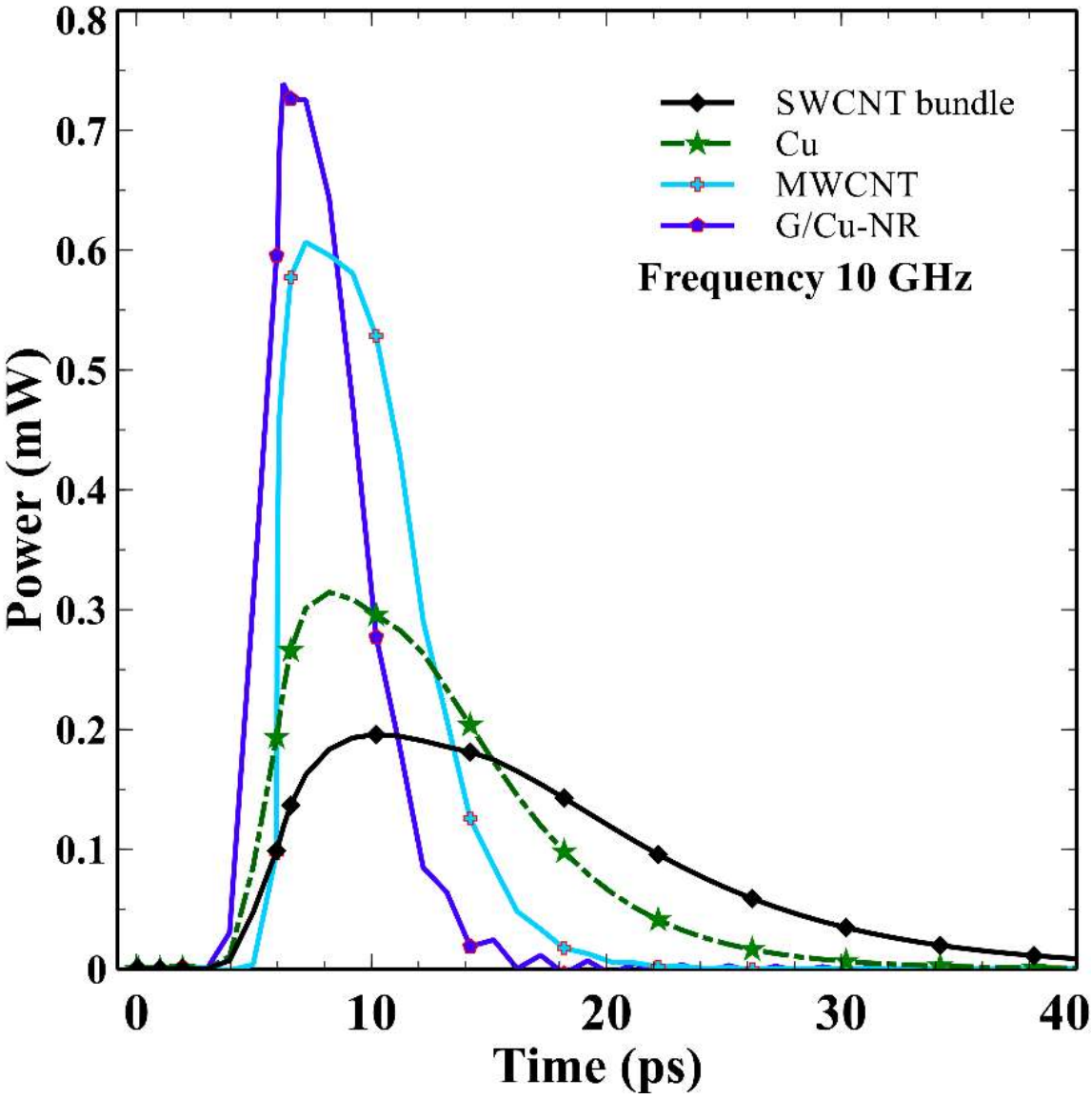

Figure 6.10: Power dissipation with time for different interconnects at 10 GHz.

In the following table, total energy dissipation for different interconnects are tabulated at 1 GHz and at 10 GHz.

Table 6.7: Energy dissipated in interconnects

Interconnect Material	Energy Dissipation (fJ)	
	1 GHz	10 GHz
Cu	4.085	0.48
SWCNT bundle	3.978	1.898
MWCNT	3.134	3.065
G/Cu-NR	4.088	1.76

From table 6.7, it seems that Cu shows the less energy dissipation than any other interconnect materials. However, G/Cu-NR still shows least power dissipation among all other alternatives. Since energy dissipation is not the only parameter to compare across interconnect materials we have chosen to study the energy delay product (EDP) as a better figure of merit. In the following table EDP is tabulated for different interconnect materials for 10 GHz. For the best interconnect materials EDP should be lowest. Table 6.8 gives better ground for the comparison of different alternatives to the present interconnect technology. While Cu shows the lowest energy dissipation it is not the option for the lowest delay. That is why the EDP gives better number to compare Cu against G/Cu-NR. Even with the EDP Cu seems a better alternative than G/Cu-NR. If one does not take electro-migration in consideration then there is no better alternative to Cu interconnect. However, with 10 times [134] more electromigration resistance (EMR), G/Cu-NR is only 32% more in EDP then Cu looks the better alternative than any other materials tabulated in table 6.8. To consider the final figure of merit (FOM) we have used the following formula,

$$FOM = Delay * \frac{Energy}{EMR} \quad (6.13)$$

Table 6.8: Energy delay product of various interconnects at 10 GHz.

Interconnect Material	Delay (ps)	Energy (fJ)	EDP (/10-27 J.s)	FOM
Cu	3.6	0.48	1.728	1.728
SWCNT bundle	4.5	1.898	8.541	-
MWCNT	1.8	3.065	5.517	-
G/Cu-NR	1.3	1.76	2.288	0.228

*Electromigration resistance (EMR) is unknow for SWCNT bundled and MWCNT.

It is noteworthy that in table 6.8, after considering the EMR, G/Cu-NR has the lowest FOM. While drawing this conclusion there is no available experimental data for EMR for SWCNT bundle and MWCNT. Here, EMR for Cu is taken as 1.0 for this comparison. Even if SWCNT and MWCNT shows 10 times more EMR than Cu, FOM for these two materials would be 0.8 and 0.5 which are at least more than 200% of G/Cu-NR.

6.5. Conclusion

All the studied interconnects' model parameters have been listed in this chapter for the purpose of an application demonstration in a hybrid CMOS IC. In between inverter pairs interconnect block has been placed and associated delays have been studied in this chapter. It is found that graphene on copper based hybrid interconnect outperforms all other interconnect in terms of delay. A 5nm width case at 10 GHz suggest this conclusion. For an interconnect of width more than 10 nm, it appears that Cu still outperforms all other materials. However, below 10 nm, Cu suffers from grain boundary scattering and surface scattering. Due to theses scatterings Cu

resistivity increases logarithmically with decrease of width. Therefore, G/Cu-NR could be the best contender to Cu beside MWCNT for upcoming technology nodes.

CHAPTER 7
CONCLUSION

As an emerging alternative to present interconnect, various CNTs and graphene/copper hybrid interconnect materials have been studied in this dissertation. For the case of CNTs, semi-classical approach has been taken within closed analytic form to explain electrothermal transport phenomena. A new emerging interconnect material, graphene on copper hybrid material system has been systematically explored using density functional theory (DFT). So far, material's structural parameters, electrical resistivity and capacitance behavior have been explored.

In this dissertation, it has been concluded that among the different variants of CNTs MWCNT is more thermally stable and SWCNT bundle is more electrically conductive. A selective use of both may be beneficial for post-CMOS interconnect solution with the challenge of process integration. However, another route to overcome the integrational challenge of CNT is to use Cu as interconnect channel material along with graphene. Graphene will serve as a good conductor and also a better thermal conductor along with Cu. At the same time graphene serves as the thinnest Cu diffusion barrier which enables further shrinking of technology nodes beyond 5nm. In this dissertation, we have calculated the resistance and capacitance properties of graphene copper hybrid interconnect as a promising candidate of interconnect. As our calculation suggested that beyond 3 nm scaling of width of this graphene/copper hybrid interconnect quantum capacitance get enhanced, it may be useful for energy storages rather than an interconnect. However, for upcoming technology nodes, it is found that graphene on copper based hybrid interconnect outperform all other interconnect in terms of delay.

Further exploration and systematic study of electrical properties is possible along with experimentation to understand the feasibility of this material system to be integrated as post CMOS interconnect. Beside studying electrical properties any relevant optical and other excited states properties could be useful to understand at high bias condition.

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APPENDIX-A
PARTIAL LIST OF SYMBOLS AND ACRONYMS

Symbol	Definition
A	Cross-sectional area of CNT interconnect
C	Specific heat of CNT
C_{EK}	Electrostatic capacitance
D	Diameter of CNT
D_{in}	Inner diameter of a MWCNT
D_k	Diameter of k^{th} shell in MWCNT or in SWCNT bundle
D_{out}	Outer diameter of a MWCNT
E_0	True ground-state energy
E_{elec}	Electronic energy
E_{nu}	Energy of a nucleus
e	Magnitude of electronic charge
L	Length of a CNT interconnect
L_K	Kinetic inductance
L_M	Magnetic inductance
M_k	Equivalent conducting channels on k^{th} shell of a CNT
N	Number of electrons
N_H	Number of CNT shells in the direction of Height
N_{op}	Phonon occupation probability
N_{shell}	Total number of CNT shells
N_w	Number of CNT shells in the direction of width
R	Resistance
T	Temperature
Ta/TaN	Tantalum on tantalum nitride
Ti/TiN	Titanium on titanium nitride
T_k	Temperature of k^{th} shell
V	Biasing voltage across interconnect
V_{ext}	External potential

Symbol	Definition
ϵ_r	Relative permittivity of a material
μ	Magnetic permeability of the CNT environment
h	Plank constant
$\hbar$	Reduced Plank constant
h_k	Distance between ground plane and the center of k^{th} CNT shell
δ	Inter shell gap in between adjacent CNT shells (0.34 nm)
κ	Heat conductivity
κ_{ILD}	Heat conductivity of interlayer dielectric
κ_x	Heat conductivity in x direction
κ_y	Heat conductivity in y direction
κ_z	Heat conductivity in z direction
λ_{ac}	Scattering length of electrons due to acoustic phonons
λ_{eff}	Effective mean free path of electron
λ_{op}	Scattering length of electrons due to optical phonons
$\lambda_{op,abs}$	Scattering length due to optical phonon absorption
v_F	Fermi velocity (for graphene, 8.854×10^5 ms^{-1})
ρ	Density of materials
ω_{op}	Optical phonon frequency

Acronyms	Definition
BOA	Born-Oppenheimer approximation
BTE	Boltzmann transport equation
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary metal oxide semiconductor
CMP	Chemical and mechanical polishing
CNT	Carbon nanotube
CVD	Chemical vapor deposition
DFT	Density functional theories
DOS	Density of states
EM	Electromigration
FEM	Finite element method
FLOPS	Floating point operations
FS	Fuchs-Sondheimer
GNR	Graphene Nanoribbon
HF	Hartree-Fock
IC	Integrated circuit
ILD	Interlayer dielectric
LDA	Local density approximation
MFP	Mean free path
MLWF	Maximally localized Wannier Wave Function
MOSFET	Metal oxide semiconductor field effect transistor
MS	Mavadas-Shatzkes
MWCNT	Multiwall carbon nanotube
NEGF	Non-Equilibrium Green Function
QE	Quantum-Espresso
RTA	Relaxation time approximation
SCF	Self-consistent field
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single wall carbon nanotube
TCR	Temperature coefficient of resistance
THz	Tera Hertz
VLSI	Very large-scale integration
XC	Exchange correlation

APPENDIX-B
CODES

Code 1. MATLAB code solve coupled electro-thermal transport equation for SWCNT.

```
clear all; clc; %INitialization

% List of parameters. every time run if you edit it.
L=2e-6;     % Length of CNT [m]
Tin=350;    % Initial Temperature.
V=4;        % Bias voltage
D=2.7e-9;   % Diameter [nm]

%physical constants
K_B=1.3806503e-23;      % Boltzman constants
q=1.60217646e-19;       % Electronic charge.
m=9.10938188e-31;       % Mass of electron.
h=6.626068e-34;         % Planks constant.
g=0.15;                 % CNT-subs thermal conductivity [W/(m-K)].
Rc=1e3;                 % Contact Resistance.

%derived parameters
R0=h/(2*q^2);           % Quantized Resistance.
Lh=2e-9;                % Thermal healing length,
resolution=ceil(L/Lh);  % Points along the CNT length.

save parameters L V D K_B q m h g R0 Rc resolution

load parameters
T=350;

Tin=ones(1,resolution)*T;
R_differential=zeros(1,resolution);
differential_length=L/resolution;

iteration_number=10;
convergence_line=zeros(1,iteration_number);

for index_temp_convergence=1:iteration_number

    for index=1:resolution
        T_var=Tin(index);
        lambda_eff=lambda(T_var);
        R_differential(index)= ((R0*differential_length)/(4*lambda_eff));
    end
%REsistance and current and joule heat
% R=R0/(4*lambda_eff); %This R is in unit length. According to Yaos work.

    R=sum(R_differential);
    I=V/(R+Rc); % total resistance is R.
    p_joule_heat=I^2*R/L; % joule heating per unit length. R/L is the resistance
of per unit length. we need per unit length joule heating.
    T_x_ep=temp(p_joule_heat,T);
    convergence_line(index_temp_convergence)=p_joule_heat;
    Tin=T_x_ep;
end
```

```
figure(1);
plot(1:iteration_number,convergence_line);
x=linspace(-L/2,L/2,resolution);
figure(2)
plot(x,Tin)


function lambda_eff=lambda(T)

load parameters
h_cut_omega=0.16*q; %0.16~0.2 eV.
N_op_300=1/(exp(h_cut_omega/(K_B*300))-1);
N_op_T=1/(exp(h_cut_omega/(K_B*T))-1);

lambda_op=56.4*D;
lambda_op_abs=lambda_op*(N_op_300+1)/N_op_T;
lambda_ac=10^3*D*400.46/T; %
lambda_op_ems_fld_T=((h_cut_omega-K_B*T)/(q*(V/L)))+(((N_op_300+1)/(N_op_T+
1))*lambda_op);
lambda_op_ems_abs_T=lambda_op_abs+(((N_op_300+1)/(N_op_T+1))*lambda_op);
lambda_op_ems=(lambda_op_ems_fld_T^-1+lambda_op_ems_abs_T^-1)^-1;
% THIS IS RESULT
lambda_eff=(lambda_ac^-1+lambda_op_ems^-1+lambda_op_abs^-1)^-1;
```

Code 2. Finite element implementation using COMSOL scripting with live link to MATLAB. This code was implemented for MWCNT interconnect.

```
% This code will calculate the breaking condition for several gemoetry of MWCNT

clear all; clc; close all;
inputs;             %inputs parameter loading calling

cnt_length=5e-6;    %length of cnt, WE WILL NOT CHANGE IT
Din=50e-9;
Dout=10e-9;
V=[0.25 0.5 1 1.5]; % Bias voltage
for i=1:length(V)
    out(i,:)=Vbreaking(cnt_length,Din,Dout,V(i))
end
save data out
```

```
%Physical constants
K_B=1.3806503e-23; %boltzman constants
q=1.60217646e-19; %electronic charge.
m=9.10938188e-31; %mass of electron.
h=6.626068e-34;% planks constant.
mu0=4*pi*1e-7;
%RLC
R0=(h/(2*q^2)); %electrons degeneracy already included
vf=8e5;
Lk=R0/vf; % per unit meter.
Cq=1/(R0*vf); %per unit meter.
c=3e8;
epsilon_0=1/(c^2*mu0);

%inputs
T=350; %in kelvin this operational ambient for semiconductor chip
delta=0.34e-9; %for showing variation of T and dia in lambda_eff
Rcont=2e1; %contanct resistance
ILD_thickness=7.0E-7; %for FEM
Tbreaking=873;
tol=1.0; %this is tolerance for temperature for the Vbreaking code
```

```
function out=Vbreaking(cnt_length,Din,Dout,V)
constants;          % calling physical constants file
inputs;                    % calling input file.
Nshell=ceil(((Dout-Din)/(2*delta))+1);
D=Din:2*delta:Dout;
Volume=(cnt_length/4)*pi*(Dout^2-Din^2);
Area=pi*(Dout^2-Din^2)/4;
Surf_area=pi*Dout*cnt_length;

if length(D)<Nshell
    D=[D D(end)+2*delta];
end
    while 1
             M=Mshell(Din,Dout,T); %number of effective channel in diffeent shell
            %R calculation
            Nch=sum(M);
             s=zeros(size(Nshell));
             for k=1:Nshell
             %lambda_eff=lambda(L,T,V,D)
                 lambda_k=lambda(cnt_length,T,V,D(k)) ;
                 s(k)=(M(k)*lambda_k)/(lambda_k+cnt_length); %conductance of this
channel
                 r(k)=(h/(2*q^2))*s(k)^-1; %resistance of kth shell.
             %    r_inv(k)=r(k)^-1;%alternative way to calculate R
             end
             S=sum(s);
             Rintrinsic=(h/(2*q^2))*S^-1;
             % Rintrinsic=sum(r_inv)^-1; %alternative way to calculate R
             R=Rcont+Rintrinsic;

             Total_current=V/R;
             Total_power=Total_current^2*Rintrinsic;
             TotalPowerPerVolume=Total_power/Volume; %in m^3, everything in SI
%            total_power_pu_length=Total_power/cnt_length;
             current_den=(Total_current/Area)/10^4;    % A/cm^2
             in_out_temp=call_fem(cnt_length,Din,Dout,TotalPowerPerVolume); % FEM
by comsol
             avg_temp=sum(in_out_temp)/2;
             if abs(T-avg_temp)<1.0
                 break,
             end
             T=avg_temp;
             %start next cycle with avg_temp for Mshell(T)
    end

R=Rintrinsic/cnt_length;          %per unit length
Lk=Lk/Nch;                              %per unit length
Cq=Nch*Cq;                              %per unit length
Lm=((mu0/(2*pi))*log(Dout/Din));  %per unit length
Ce=((2*pi*epsilon_0)/log(Dout/Din)); %per unit length
I=Total_current;
out=[R,Lk,Cq,Lm,Ce,I];
```

```
% COMSOL Multiphysics FEM Model MATLAB-file
function in_out_T=call_fem(cnt_length,Din,Dout,TotalPowerPerVolume)
flclear fem
% COMSOL version
clear vrsn
vrsn.name = 'COMSOL 3.5';
fem.version = vrsn;
inputs
% Geometry
width=(Dout/2)-(Din/2);
g2=rect2(width,cnt_length,'base','corner','pos',{Din/2,'0'},'rot','0');
g4=rect2(ILD_thickness,cnt_length,'base','corner','pos',{Dout/2,'0'},'rot','0');
parr={point2(Din/2,cnt_length/2)}; g8=geomcoerce('point',parr);
parr={point2(Dout/2,cnt_length/2)}; g3=geomcoerce('point',parr);

% Analyzed geometry
clear p s
p.objs={g8,g3}; p.name={'PT1','PT2'}; p.tags={'g8','g3'};
s.objs={g2,g4}; s.name={'R1','R2'}; s.tags={'g2','g4'};
fem.draw=struct('p',p,'s',s); fem.geom=geomcsg(fem);

% Initialize mesh
fem.mesh=meshinit(fem, ...
                  'hauto',5);

% Application mode 1
clear appl
appl.mode.class = 'GeneralHeat'; appl.mode.type = 'axi';
appl.module = 'HT'; appl.shape = {'shlag(1,''J'')','shlag(2,''T'')'};
appl.assignsuffix = '_htgh'; clear prop
prop.analysis='static'; appl.prop = prop;
clear bnd; bnd.type = {'q0','T','cont'};
bnd.shape = 1; bnd.T0 = {273.15,350,273.15}; bnd.ind = [1,2,1,2,3,2,3,2,2];
appl.bnd = bnd; clear equ; equ.sdtype = 'gls';
equ.shape = 2; equ.Q = {TotalPowerPerVolume,0}; equ.k = {{0.05;1800},1.4};
equ.ind = [1,2]; appl.equ = equ; fem.appl{1} = appl;
fem.sdim = {'r','z'}; fem.frame = {'ref'}; fem.border = 1;
fem.outform = 'general'; clear units; units.basesystem = 'SI';
fem.units = units;

% ODE Settings
clear ode; clear units; units.basesystem = 'SI';
ode.units = units; fem.ode=ode;
% Multiphysics
fem=multiphysics(fem);
% Extend mesh
fem.xmesh=meshextend(fem);
% Solve problem
fem.sol=femstatic(fem, ...
                  'solcomp',{'T'}, ...
                  'outcomp',{'T'}, ...
                  'blocksize','auto');

fem0=fem;

Inner_shell_T=postint(fem,'T', ...
           'unit','K', ...
           'recover','off', ...
           'dl',[2], ...
           'edim',0);
Outer_shell_T=postint(fem,'T', ...
           'unit','K', ...
           'recover','off', ...
           'dl',[5], ...
           'edim',0);
in_out_T=[Inner_shell_T,Outer_shell_T];
```

Code 3. Quantum Espresso input file for a 2D graphene using Van der Waals correction. This following code is the first step of the DFT calculation and knows as SCF calculation.

```
&CONTROL
      calculation = 'scf'
      restart_mode='from_scratch',
      prefix='bulk',
      pseudo_dir = '/work/kmohsi1/QE_g/',
      outdir= '/work/kmohsi1/QE_g/output/',
      verbosity='high'
      tstress =.f, tprnfor =.f.
      wf_collect=.f,
/
&SYSTEM
      ibrav= 0,
      celldm(1) =4.830366967101510,
      nat= 2,    ntyp= 1,
      ecutwfc =40.0,
      occupations='smearing', smearing='mp',
      degauss=0.01, input_dft='vdW-DF-ob86',
/
&ELECTRONS
      diagonalization='david',
      electron_maxstep = 100,
      mixing_mode = 'local-TF',
      mixing_beta = 0.2,
      conv_thr = 1.0d-3,
/
ATOMIC_SPECIES
    C   12.0107       C.pz-n-kjpaw_psl.0.1.UPF
CELL_PARAMETERS alat
   1.000000000000000                    0                    0
   0.500000000000000   0.866025403784439                    0
                   0                    0  10.732721359260136
ATOMIC_POSITIONS alat
C                   0                    0   0
C                   0   0.577350269189626   0
K_POINTS automatic
4 4 1 0 0 0
```

Code 4. Quantum Espresso input file for the second step. This step is known as NSCF. This is to sample Brillouin zone with high resolution to be used for band structure calculation.

```
&CONTROL
      calculation = 'nscf'
      restart_mode='from_scratch',
      prefix='bulk',
      pseudo_dir = '/work/kmohsi1/QE_g/',
      outdir= '/work/kmohsi1/QE_g/output/',
      verbosity='high'
      tstress =.f, tprnfor =.f.
      wf_collect=.f,
/
&SYSTEM
      ibrav= 0,
      celldm(1) =4.830366967101510,
      nat= 2,    ntyp= 1, nbnd=12,
      ecutwfc =40.0,
      occupations='smearing', smearing='mp',
      degauss=0.01, input_dft='vdW-DF-ob86',
/
&ELECTRONS
      diagonalization='david',
      electron_maxstep = 100,
      mixing_mode = 'local-TF',
      mixing_beta = 0.2,
      conv_thr = 1.0d-3,
/
ATOMIC_SPECIES
    C   12.0107       C.pz-n-kjpaw_psl.0.1.UPF
CELL_PARAMETERS alat
   1.000000000000000                    0                    0
   0.500000000000000   0.866025403784439                    0
                   0                    0  10.732721359260136
ATOMIC_POSITIONS alat
C                   0                    0   0
C                   0   0.577350269189626   0
K_POINTS automatic
32 32 1 0 0 0
```

Code 5. Quantum Espresso input file for density of states calculation. This calculation requires results from previous two calculations.

```
 &dos
    prefix='bulk',
    outdir = '/work/kmohsi1/QE_g/output/',
    Emin = -8.4193    , Emax = 2.4193
    DeltaE = 0.01,
    fildos = '/work/kmohsi1/QE_g/dos.dat'
/
```

Code 6. PBS file is to run all these above calculations sequentially one after another using HPC environment. PBS file automates the user interaction with supercomputers. Following is a sample PBS input file to run a code using 64 processors in parallel in SuperMike-II.

```
#!/bin/bash
#PBS -l nodes=4:ppn=16
#PBS -l walltime=04:00:00
#PBS -q workq
#PBS -A hpc_graphene01
BIN_DIR=$ESPRESSO_ROOT/bin
myfile=/work/kmohsi1/QE_g
mpirun -np 64 $BIN_DIR/pw.x -i $myfile/scf.in > $myfile/scf.out
mpirun -np 64 $BIN_DIR/pw.x -i $myfile/nscf.in > $myfile/nscf.out
```

APPENDIX-C
MATLAB CODE FOR FDTD TECHNIUQE

For implementing FDTD analysis following is the sample code.

```
% Defining parameters.
F= 10e9 ; % Frequency [Hz]
% Constants computed in previous section
R= 8.8e6; % [Ohm/meter]
L= 0.0011e-3; % [H/m0
G= 0;
C=0.013e-9; %[F/m]
Length=1e-6;
Dx=1e-9; % Discretization of space
Dt=1e-12; % 0.1 ps, Discretization of time.

x_hi=Length/Dx; % Highest value of x
t_hi= 1000e-12/Dt; % Highest value of t [s], upto 100 ps.

% Initialization of IV
V=zeros(1,x_hi);
I= zeros(1,x_hi);

% FDTD parameters
A1=((C/Dt)+(G/2))^-1;
A2=((C/Dt)-(G/2));
B1=((L/Dt)+(R/2))^-1;
B2=((L/Dt)-(R/2));

%FDTD loops
for N=1:t_hi;
    V(1) = sin(2*pi*F*N*Dt); % sine wave source
    for K=2:x_hi;  % find voltage everywhere on the line
        V(K)= A1*A2*V(K)+(A1/Dx)*(I(K-1)-I(K));
    end
    for K=1:x_hi-1;                % find current everywhere on the line
        I(K)= B1*B2*I(K)+(B1/Dx)*(V(K)-V(K+1));
    end
plot(V)                        % plot the voltage all along the line at time N
axis([0 x_hi -2 2])   % control the axis for uniform pictures
pause(.1);                % give the program time to plot to screen
end


% modeling of pulse source
fs = Dt; % sample freq
D = [5 10 50]' * 1e-12; % pulse delay times
t = 0 : Dt : 100e-12; % signal evaluation time
w = 100e-12; % Pulse Width [s]
yp = pulstran(t,D,@rectpuls,w);
```

VITA

K M Mohsin was born in 1988 in Dhaka, Bangladesh. He completed his B.S. in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in March 2011. Since January 2012, he started his Ph.D. under Dr. Ashok Srivastava in the division of electrical and computer engineering at the Louisiana State University, Baton Rouge, LA. He obtained his M.S. from the same university in May 2017. Mohsin's research interest includes theory, design, modeling, simulation and fabrication of energy efficient two-dimensional materials and devices for integrated circuit design. He is also a visionary futuristic, technocrat and has an active interest on technology trend combining the concept of engineering, philosophy and entrepreneurship of nanotechnology. He is expected to graduate in December 2017. K M Mohsin will join technology and manufacturing group in Intel Corporation at Hillsboro, OR as an interconnect integration development engineer after his graduation.