2005

Wafer level chip scale packaging using wafer bonder

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WAFFER LEVEL CHIP SCALE PACKAGING USING WAFER BONDER

A Thesis
Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering
in
The Department of Electrical and Computer Engineering

by
Kailash Upadhyaya
B.E., University of Madras, India, 2001
August 2005
Dedicated to the Almighty.............
ACKNOWLEDGEMENTS

I would like to express my sincere gratitude and appreciation to my graduate advisor, Dr. Pratul K. Ajmera for his invaluable technical guidance and support.

The completion of this thesis would have been impossible without the help of Bharath Thiruvengadachari, Abhilash Krishna, Daniel Brignac, Dr. Kim Lewis, Varsha Francis, Nagaraju Komuravelli and CAMD (Center for Advanced Microstructures and Devices) personnel. All gratitude is due to them.

I would like to express my heart felt gratitude to Dr. Yoonyoung Jin and Fareed Dawan in CAMD for deposition of Cr/Au thin films.

I would like to extend my deepest appreciation to Mr. Yohannes Desta, CAMD for nickel electroplating on glass substrates.

This work was supported in part by the Center for Advanced Microstructures and Devices (CAMD) at Louisiana State University. Significant experimental work in this research was carried out in the Electronic Material and Device Laboratory in the Department of Electrical and Computer Engineering at LSU and use of its facilities is also sincerely acknowledged.
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ABSTRACT

An in-house processing capability is developed in this research for silicon-glass bonding for microfabrication and wafer level chip scale packaging (WLCSP) using a wafer bonder. New masking technology for wet etching of glass to a depth of more than 430 µm is reported in this research work along with development of an anodic bonding process that permits electrical feedthroughs for connections to outside world.

Three novel masks were developed in this work for deep wet etching of glass. They were multilayers of metals Mo/Cr/Au (mask 1) and Cr/Au/electroplated Ni (mask 2) both in combination with 20 µm thick AZ® P4620 photoresist and anodically bonded silicon (mask 3). Etch depths greater than 600 µm in glass has been achieved using anodically bonded silicon mask 3 above. It may be currently the only method available to achieve etch depths of 1 mm in glass. Earlier barrier of 300 µm etch depth in glass using multilayer metal mask has effectively been broken in this work with an etch depth of 430 µm achieved using electroplated Ni mask 2) above. A high value of 0.88 for the aspect ratio, defined as the ratio of the vertical etch depth to the lateral etch distance, was achieved using mask 1) above.

The problem of etched surface roughness observed in glass with undiluted HF etching has been alleviated by use of a combination of 50:5:1 by volume HF:HCl:HNO₃.

Etch depths of 355 µm has been achieved in silicon using 45 % KOH solution at 50 °C with 1 µm thick oxide mask. The above etch parameters also resulted in smooth etched mirror like surfaces, sharp edges in etched pits and deep trenches in silicon. The decontaminated etched glass and silicon substrates were aligned in-situ and bonded using an AML 402 wafer bonder. The corner areas of the glass wafer were diced to expose the
metal lines permitting electrical communication from the anodically bonded packaged chip to the outside world. The concept of WLCSP using anodic bonding has been developed and demonstrated in this research.
1. INTRODUCTION

There are many different types of chip scale packaging (CSP) commercially available. Wafer level chip scale packaging (WLCSP), a type of CSP, has been gaining momentum in recent years because for this case all the fabrication procedures are performed at the wafer level. WLCSP integrates the advantages of both chip scale packaging (CSP) and wafer level packaging (WLP). Wafer bonding is one of the viable means to achieve WLCSP.

1.1 Wafer Bonding and Its Objective

Wafer bonding may be defined as permanent or temporary binding of two similar or dissimilar substrates either chemically or physically. There are three types of wafer bonding commonly employed. These are 1) direct wafer bonding (DWB), 2) intermediate layer bonding (ILB) and 3) anodic wafer bonding (AWB). AWB is used to permanently bond glass to silicon without use of adhesives. The glass and silicon wafers are heated to a typical temperature in the range of 300 – 500 °C, depending on the type of glass used for bonding. At this temperature, the alkali metal ions in glass become mobile. The glass and silicon wafers are brought into contact and a high voltage is applied across them. This results in the alkali metal ions in the interface to migrate towards the cathode resulting in an interface layer with high electric field. This phenomenon results in an electrostatic attraction bringing the glass and silicon into intimate contact. The presence of high electric field causes the oxygen anions to flow from glass to silicon resulting in an anodic reaction at the interface and therefore a permanent chemical bond between glass and silicon occurs. ILB involves deposition of an intermediate thin film layer such as low melting point glasses, low temperature eutectics or adhesives prior to bonding. DWB
takes advantage of the fact that any two flat, clean, highly polished surfaces will stick together if they are brought into contact. The initial bonding is usually done at room temperature with some force applied. The mechanism of DWB involves pre-bonding comprising of van der Waals forces on hydrophobic surfaces or hydrogen bond bridging on hydrophilic surfaces followed by fusion bonding involving formation of chemical bonds upon a higher temperature anneal.

Wafer bonding is an enabling technology that permits 1) fabrication of microstructures that are otherwise not possible and 2) facilitates packaging. Wafer bonding permits use of new starting materials for MEMS such as the thick film SOI wafers or fabrication of novel microstructures otherwise not possible. There are many advantages of the packaging aspects of wafer bonding as well. Few of the latter advantages are listed below:

- To attach two halves of a device, microstructure or a microsystem
- To protect the sensitive microsystem from harsh environment
- To provide a high level of cleanliness as wafer bonding is performed prior to chip dicing
- To facilitate hermetic sealing and mounting onto the final package providing mechanical stability.

1.2 Research Goals

The main goal of this research is to 1) demonstrate the concept of WLCSP using a wafer bonder and 2) to prove the feasibility of communication with the outside world from within the package after the WLCSP has been carried out.
WLCSP integrates the advantages of both chip and wafer level packaging. The advantage of chip scale packaging (CSP) is that only the chips that are functional after testing are packaged. Advantage of wafer level packaging (WLP) is that it brings the packaging process into the realm of batch processing with associated cost savings due to ease of handling and processing an entire wafer at one time. Testing of individual chips need only be carried out for WLCSP after the packaging is complete. In order to realize the above objectives, the following subtasks need to be performed:

1. Developing a novel masking technology to etch glass wafers.
2. Develop anodic bonding process with electrical feedthroughs.

1.3 Organization of Thesis

The work described here is divided into six chapters. Chapter 2 discusses the background theory of wafer bonding, packaging and wet etching chemistry for silicon and glass wafers. Chapter 3 deals with a review of selected papers on anodic bonding and glass etching. Chapter 4 details the process flow, methodology and experimental procedures for etching of silicon and glass substrates prior to anodic bonding. Chapter 5 discusses experimental results. Chapter 6 provides the summary and makes suggestions for future work.
2. BACKGROUND THEORY

Wafer Bonding may be defined as a process in which two wafers are bonded to form a single substrate featuring specific properties. There are three major wafer bonding techniques available. They are 1) anodic bonding 2) silicon fusion bonding or direct wafer bonding and 3) intermediate layer bonding.

2.1 Anodic Bonding

In 1969, Wallis and Pomerantz invented the concept of glass-metal seal bonding using assisted electric field [1] based on the adhesion between two optically smooth surfaces first observed by Lord Rayleigh [2] in 1936. Rayleigh made a notable observation that the interaction energy between the two surfaces was of the order of 100 mJ/m² [2]. This phenomenon did not have any technological impact for a long time. Wallis and Pomerantz’s work has resulted into what is now classified as anodic bonding. This technique has widely been used in the area of encapsulation of sensors. A major problem associated with anodic bonding is the presence of alkali ions such as sodium which may make it difficult to be used in conjunction with CMOS based devices because alkali ions cause serious reliability problems in MOS devices. Other major problem is the use of high electric fields. However, innovations in semiconductor technology have alleviated some of the problems of electrical damage and alkali ion contamination inherent in an anodic bonding process. The mitigation procedures for the electrostatic discharge damage caused by anodic bonding include static protection circuits, metallic shields and pre-etched cavities in the borofloat glass substrate right above the circuitry on the silicon substrate [2].
Anodic bonding is useful in the fabrication of pressure sensors, solar cells, piezoresistive applications and various other MEMS packaging applications.

Anodic bonding is also referred to as Electrostatic Bonding or Field-Assisted Thermal Bonding. This bonding process is assisted by electric field. In this method we bond a conductive silicon substrate to a glass substrate which is rich in sodium. The advantages of this method include low bonding temperatures (200 - 500 °C), low residual stress, and less stringent requirements on the surface quality prior to processing [3]. The problem of high temperatures (1000 °C) for anodic bonding was mitigated by the use of high electric fields. The use of high electric fields resulted in the formation of anodic bonds at relatively low temperatures. Bonding can be achieved at temperatures between 200 °C and 500 °C depending on the thickness of the glass.

The schematic representation of an anodic bonding set up is as shown in Fig. 2.1. For this specific case, the silicon and the glass substrates are bonded by clamping them between two metal electrodes at 380 °C. A high electric field is created by applying a DC potential of 1 kV between the two electrodes. Glass substrate contains Na⁺ ions, which at this high temperature are displaced from the bonding surface of the glass by the applied electric field as shown in Fig. 2.2. The depletion of the sodium ions near the surface of the glass makes the glass substrate surface highly reactive with the silicon surface, resulting in formation of chemical bonds. The operating temperatures are near the glass softening temperature but well below its melting point. The wafers are usually bonded in about 10 minutes depending on the bonded area and the applied voltage.

The anodic bonding process is an electrochemical process where the silicon to be joined to the glass is positively biased. There are a number of explanations for the
mechanism of anodic bonding. According to one explanation by Wallis and Pomerantz [1], Na\(^+\) ions being cations are attracted towards the cathode in the presence of applied voltage forming a layer depleted of Na\(^+\) ions close to surface. This results in a very high electric field which in turn causes the motion of oxygen anions. The moving oxygen anions results in the formation of an oxide layer at the interface as shown in Fig. 2.2. This oxide layer is the reason for final bond strength.

Fig. 2.1: Basic anodic bonding setup scheme.

Fig. 2.2: Mechanism of anodic bonding. After reference [3].
Some of the requirements to achieve a good anodic bond are that the interface should be flat, smooth, free from hillock formation and dust. The native oxide layer on silicon substrate, if present, must be less than 200 nm [3]. It is best to limit the process below 450 °C to avoid effects of high temperature on both substrates. In order to minimize thermal stresses, the thermal co-efficient of expansion of glass must closely match that of silicon. There are few such glasses commercially available for the purpose of wafer bonding. Commonly used glasses include Corning 7740 (Pyrex), Corning 7070, Schott 8330, Hoya SD-2 and Iwaki 7570. Pyrex is the most commonly used glass in MEMS for bonding purposes due to its capability to form a strong hermetic seal to silicon. Glass provides a wide variety of advantages and is increasingly being used in the fabrication of MEMS devices. Glass also has good mechanical and optical properties, high electric resistance and is readily bondable with silicon substrate at temperatures far lower than necessary for a fusion bond.

2.1.1 Advantages of Anodic Bonding

Anodic bonding has its own advantages and disadvantages. Few of the advantages [4] are as follows:

- Bonding is achieved at lower temperatures, 200 – 450 °C, which in turn gives more design flexibility
- There is no loss of dimensional tolerances around etched cavities because there is no measurable flow of glass
- Makes possible packaging of moving microstructures in silicon with relative ease
- Permits coupling of light from outside to silicon wafer
• Parasitic capacitances are small since glass has low permeability and is usually quite thick
• It facilitates hermetic sealing in vacuum
• Accurate alignment of pre-patterned glass and silicon wafers is possible. This alignment is attributed to the transparency of the glass at optical wavelengths
• Anodic bonding is highly tolerant to particle contamination. This is attributed to the clamping force generated by the electrostatic field
• Very high strength permanent bond can be achieved with relative ease
• Glass protects the microstructures in silicon from package induced stresses. The sensitive microstructure is bonded to a relatively thick glass (700-1000 µm) which in turn can be mounted on a PCB or other substrates having a thermal mismatch with silicon. In this way the stresses are limited to the glass layer without affecting the silicon
• It brings packaging process into the realm of batch processing with associated cost savings.

2.1.2 Disadvantages of Anodic Bonding

Two major disadvantages associated with anodic bonding are bow or warp and electrolysis products formed during anodic bonding.

Recent studies [5] have shown that this bow may be associated with the considerable volumetric changes undergone by the glass during anodic bonding. The bow may be considerable, as high as 30 µm for 3 mm glass substrates. Thermal mismatch of the substrates contribute to bow.
It is suggested that electrolytically available oxygen anions at the silicon/glass interface are responsible for the final bond strength in anodic bonding. If the wafers are structured (cavities, etched grooves or pits), there will be entrapment of oxygen in the cavities during hermetic sealing which in turn can have serious implications on sensitivity and temperature stability of low pressure devices [5]. Oxidation of metal lines is also possible resulting in higher resistance. If active metals are present at the interface, they may inhibit final chemical bond strength. This inhibition is attributed to the reduced supply of oxygen anions available for final high strength covalent bond.

2.2 Direct Wafer Bonding (Silicon Fusion Bonding)

Antypas and Edgecumbe [6] in 1975 were the first to perform “wafer fusion” at elevated temperatures which involved transfer of thin gallium arsenide layer to a glass substrate. The concept of silicon-silicon wafer bonding at room temperature came into inception during the year 1985-1986. The initial low strength wafer bonding performed at room temperature was followed by high temperature thermal treatment. Investigations were done on silicon wafers without any thermal oxide [7] and with one or both the wafers covered by a thermally grown oxide [8]. Peterson et al. [9] pioneered the concept of silicon wafer bonding for the manufacture of world’s first pressure sensors with cavities etched in one of the silicon wafers.

Direct wafer bonding (DWB) can be defined as direct bonding of two silicon wafers without the presence of any intermediate layer. The bond is purely based on van der Waals forces which can be further improved by annealing. DWB has also been referred to as silicon fusion bonding (SFB) because of the thermal treatment involved after the initial bonding is achieved at room temperature. SFB is used for fabrication of
silicon on insulator (SOI) structures. The basic process for SOI structures comprises of bringing in contact the two substrates to be bonded and annealing them in a wet or dry oxidation furnace. Very high temperatures exceeding 1000 °C are required, which is a major disadvantage of this process and is incompatible with any post CMOS process. Two wafers with or without silicon dioxide layers can be directly bonded. Unlike anodic bonding, interfacial thermal stresses are absent because the thermal co-efficient of expansion of both wafers are identical.

The AML 402 bonder utilizes about 500 N force under vacuum to initiate pre-bonding at room temperature. The bonder utilizes a special type of pin chuck which ensures that the bonding propagates from the center towards the wafer edges. This ensures that there is no trapped air at the interface thereby aiding in reduction of voids which in turn improves the quality of the bond.

SFB is usually achieved by placing the wafers in close contact at temperatures greater than 800 °C. The quality of the bond depends on various factors such as temperature and flatness of the surface to be bonded. The latter needs to be within 4 nm [3]. Circuits cannot be fabricated prior to direct wafer bonding because of temperature constraints of fabricated ICs which should be limited below 450 °C. High temperatures and application of small amounts of pressure are required to obtain high bond strength and voidless structures. SFB can be performed either on two oxidized silicon wafers or two bare silicon wafers or between one bare silicon wafer and one oxidized silicon wafer and even between two wafers with a thin coating of nitride (100 to 200 nm) [3] provided the surfaces are mirror polished and exceptionally clean.
There are two mechanisms by which direct wafer bonding can be explained. They are SiO$_2$ - SiO$_2$ bonding attributed to hydrogen bond bridging (hydrophilic) and Si - Si bonding (hydrophobic) [10]. The surfaces to be bonded may be either hydrophilic or hydrophobic. Hydration is done by soaking the silicon wafers in a H$_2$O$_2$:H$_2$SO$_4$ mixture or boiling in nitric acid. Hydration results in the formation of hydrophilic layer consisting of hydroxyl groups on the oxide surface. To enhance the hydroxyl groups, additional treatment in oxygen plasma may be required. The instant self bonding between the mirrored surfaces is attributed to the presence of hydroxyl groups in form of silanol (Si-OH) bonds for both hydrophilic and hydrophobic surfaces. The bonding process is done at room temperature in clean-room conditions. Further annealing will result in stronger atomic bonds. A dip in HF will facilitate self bonding of hydrophobic silicon surfaces provided the surfaces are clean. The next section discusses the mechanism of direct wafer bonding.

2.2.1 Mechanism of Direct Wafer Bonding

DWB is classified into SiO$_2$ - SiO$_2$ bonding (hydrophilic surfaces) and Si – Si bonding (hydrophobic surfaces). SiO$_2$ - SiO$_2$ bonding is attributed to formation of siloxane (Si-O-Si) bonds from the existing silanol (Si-OH) bonds [11].

\[
\text{Si-OH} + \text{OH}^- \rightarrow \text{H}_2\text{O} + \text{Si-O-Si}.
\]

The silicon dangling bonds react with water to form SiOH groups. According to Maszara et al. [12], when the two hydrophilic surfaces are brought together at room temperature, the wafers instantly adhere to each other due to hydrogen bonds. At temperatures close to 200 °C, the surface mobility of the hydroxyl groups increases resulting in increased hydrogen bond bridging between the opposite hydroxyl groups. At
about 300 °C the opposite hydroxyl groups combine to form water and siloxane network begins to form between the surfaces. Fig. 2.3 clearly illustrates the conversion of silanol bond to siloxane network.

For hydrophobic case, the native oxides are usually etched off using HF solution prior to bonding. The wafers in this case are held together initially by van der Waals forces. One has to understand that few hydroxyl groups will exist even for hydrophobic surfaces. Initially, the bonding is attributed to binding of hydroxyl groups when heated to 200 °C. However, at 200 °C water becomes mobile (dehydration of hydroxyl groups), hydrogen bonds are replaced by Si-O-Si bond. At about 400 °C strong Si-Si covalent bonds are formed as also shown in Fig. 2.3.

2.2.2 Advantages/Disadvantages of Direct Wafer Bonding

The advantages of DWB include:

- Unlike anodic bonding, the problem of thermal expansion mismatch at the interface is eliminated. The stress at the interface is drastically reduced in fusion bonded silicon wafers.
- The bond strength is a function of annealing temperature and can be as high as single crystal silicon [10].
- For certain applications such as micro-turbine application, SFB can be used at much higher operating temperatures not possible by anodic bonding.

The disadvantages of DWB include:

- Stringent surface roughness requirements to the order of a fraction of a nm compared to a few tens of nm required for anodic bonding. Also surfaces must be ultra-clean.
- Annealing of fusion bonded wafers above 450 °C cannot be performed if the substrate contains CMOS devices.

2.3 Intermediate Layer Bonding

This type of bonding involves deposition of intermediate layers such as metal film, glass film, epoxy, polymer and other materials prior to bonding. There are different types of intermediate layer bonding commercially available. They are as follows:

1. Eutectic bonding
2. Glass frit bonding
3. Adhesive bonding.
2.3.1 Eutectic Bonding

Eutectic point gives the lowest melting temperature for an alloy. An eutectic can be formed by solid-liquid inter-diffusion at their contact interface, followed by solidification upon cooling. In the case of Au and silicon, this point is located at 363 °C and corresponds to a eutectic composition of 2.85 % silicon and 97.15 % Au by weight. In order to accomplish a good eutectic bond, silicon surface preparation requires the etching of silicon oxide films that can hamper diffusion of gold into silicon. It is important that all the organic contaminants be removed prior to bonding by UV radiation exposure. To achieve good quality bond, small amount of pressure is applied. The main advantage of eutectic bonding is low temperature requirements to reach the eutectic point. The disadvantage of eutectic bonding is presence of native oxides that can hamper bonding.

2.3.2 Glass Frit Bonding

Good hermetic seals can be obtained by using glass frit bonding technique at relatively low temperatures. Prior to bonding, the glass is deposited by sputtering, spin on or screen print technique and the wafers are brought into contact at melting temperature of the glass (< 600 °C). Lead borate with significant lead oxide content is commonly used for this purpose.

2.3.3 Adhesive Bonding Technology

Adhesive bonding has found applications in many industries such as airplane, aerospace and car manufacturing industries. Like other bonding techniques, atoms and molecules fuse and stick to each other when brought in close contact in adhesive bonding. In order to facilitate adhesion at least one material must deform to fit the other. This deformation may be accomplished by several methods either by plastic or elastic
deformation, by diffusion of a solid-state material or by wetting of a surface with a liquid material. Adhesive materials can be classified as organic and inorganic adhesives. Organic adhesives are plastic and polymeric materials. Inorganic adhesives are mostly ceramic materials that are based on oxides or silicates. Few of the adhesive materials used for bonding applications are B-stage epoxies, UV epoxies, positive photoresist, negative photoresist, benzo cyclobutene, poly methyl methacrylate (PMMA), poly dimethyl siloxane (PDMS), polymides, fluoro polymers and waxes.

Photo-patterned photoresists such as SU-8 and AZ® 4000 involve an interesting technology for adhesion. The procedure for silicon/polymer/silicon bonding involves the following steps. The first step involves spinning of photoresist (positive or negative) using a spin coater. The second step involves exposure to UV light using an UV station and developing the wafer in a suitable developer to obtain the necessary pattern. The third step involves pressing the second wafer onto the polymeric pattern and either leaving the bonded wafer to dry in air for 10 hours [13] or hard baking it to 100 °C for 2 hours. This is a classic example of photo patterned bonding by the polysiloxane interconnection between two substrates [13]. This process basically involves the condensation crosslinking of the UV sensitive patterned polymer which holds the two substrates together.

The advantages of photo-patternable photoresists are as follows:

- Absence of alkali metal ions
- Low bonding temperature
- Polymers are elastic which in turn can reduce stress.

The disadvantages of photo-patternable photoresists are as follows:
Hermetic seals cannot be obtained

- Vapor pressure is high
- Mechanical properties are poor.

### 2.4 Wet Etching Chemistry of Silicon

“Wet etching” is a process by which the substrates to be etched are immersed in a reactive solution or etchant. The materials are removed either by direct dissolution or dissolution of chemical reaction products formed by the etchant. There are two types of wet etching namely isotropic etching and anisotropic etching.

#### 2.4.1 Isotropic Etching of Silicon

Isotropic etching means etch rate is equal in all directions. The processing steps involved in the isotropic etching of silicon are illustrated in Fig. 2.4. The most commonly used isotropic etchant is “HNA” [14] which stands for HF/HNO₃/CH₃COOH. Typical formulation used is 10ml HF/30ml HNO₃/80ml DI H₂O or CH₃COOH at 22 ºC [15]. The silicon is etched at a rate of 0.7 - 3.0 µm/minute [15]. The (100)/(111) etch ratio is 1:1. The silicon dioxide mask is etched at a rate of 30-70 nm/minute [15]. The HNA etching rate is drastically reduced in lightly doped regions. A major setback of this method is that it is not CMOS compatible and etches the oxide mask at a high rate. The overall reaction is given by the following equation [16]:

\[
18\text{HF} + 4\text{HNO}_3 + 3\text{Si} \rightarrow 2\text{H}_2\text{SiF}_6 + 4\text{NO} + 8\text{H}_2\text{O}.
\]

#### 2.4.2 Anisotropic Etching of Silicon

Anisotropic etching means etch rate is not equal in all crystal directions and is orientation dependent. The etch rate is faster in one direction than the other. In a typical (100) oriented silicon surface, the (100) surface etches faster than the (111) surfaces. The
A typical etch ratio can be 400:1 along <100>/<111> directions and 600:1 for <110>/<111> directions respectively in appropriate etchants. The cross sections of anisotropic etching of (100) and (110) silicon are illustrated in Fig. 2.5 and 2.6 respectively.

Fig. 2.4: Illustration of isotropic etching of silicon; a) UV exposure of positive photoresist (PR); b) PR reaction c) PR development in a suitable developer d) Etching of oxide or nitride layer with PR as mask; e) Isotropic etching of silicon with oxide or nitride as mask. After reference [2].
A variety of anisotropic etchants are available. Few of the notable ones are KOH, NaOH, NH₄OH, TMAH (Tetramethyl ammonium hydroxide), EDP (Ethylene diamine pyrochatechol), hydrazine and amine gallate etchants. KOH etchant was used to etch silicon wafer in EMDL (Electronic Material and Device Laboratory) at LSU and hence only anisotropic KOH etching will be discussed in detail here.

2.4.2.1 KOH Etching

Typical formulations reported in literature include 44 g KOH, 80 ml DI H₂O, 20 ml IPA (Isopropyl alcohol) at 85 °C or 50 g KOH, 80 ml DI H₂O, 20 ml IPA (Isopropyl alcohol) at 50 °C [15]. The etch rate for the former is 1.4 µm/minute and the latter is 1 µm/minute [15]. Recent studies [17, 18] have shown that addition of IPA not only reduces etch rate by 20 % but also increases selectivity between {111} and {100} planes. The etch ratio <100>/<111> for the above formulations is 400:1. The silicon dioxide mask is etched at a rate of 1.4 nm/minute and there is negligible etching for a
nitride mask [15]. Therefore, nitride is the most suitable mask for deep anisotropic etching of silicon with KOH. The selectivity of Si$_3$N$_4$ mask in KOH etchant is greater than 1000 and that of SiO$_2$ mask is approximately equal to 100. For the case without use of IPA, etch rates of crystal planes: $\{110\} > \{100\} > \{111\}$. For the case with use of IPA, etch rates of crystal planes: $\{100\} > \{110\} > \{111\}$.

The overall reaction is given by the following equation [17]:

$$\text{Si} + 2\text{OH}^- + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2(\text{OH})_2^{2-} + 2\text{H}_2.$$  

Concentration and temperature play vital roles in anisotropic etching of silicon using KOH. The etch rates of both silicon and silicon dioxide at varying temperature and concentration are clearly illustrated in Figs. 2.7 and 2.8.

![Fig. 2.7: KOH etching rate of \{100\} silicon in \(\mu\text{m}/\text{hour}\) at various concentration and temperature. After reference [17, 18].](image-url)
Fig. 2.8: KOH etching rate of silicon dioxide in nm/hour at various concentration and temperature. After reference [17, 18].
2.5 Wet Etching of Glass

Glass has been gaining a lot of importance in microfabrication, particularly in the area of MEMS in recent years. Glass offers certain advantages that make it a preferable material for MEMS. It has good mechanical and optical properties, high electric insulation and is readily bondable with silicon substrate at temperatures far lower than necessary for a silicon fusion bond.

Etching of glass poses serious challenges. Glass is usually etched isotropically. Various concentrations of HF have been used to etch glass. Some of the commonly used concentrations of HF to etch glass include 48 % HF, 10:1 by volume DI H₂O:HF, 6:1 by volume DI H₂O:buffered oxide etchant (BOE). The latter is a combination of HF, NH₄F and DI H₂O. Other techniques used to etch glass are deep reactive ion etching (DRIE) using SF₆ [19], ultrasonic drilling [20], powder blasting [21], laser micromachining [22] and sawing [23]. Fluorosilicic acid has been reported to etch smooth channel features in pyrex glass [24]. A combination of H₃PO₄: H₂O: HF with volume ratio of 14:5:1 has also been used to etch 120 µm deep recess with smooth bottom surfaces [25]. Ultrasonic machining is recommended for holes in glass. Powder blasting provides etch rate of up to 25 µm/hr [21].

Various masks have been reported for preferential etching of glass. The most common masks include 1) Cr and Au layers and 2) photoresists. The major problems associated with metal masks are pinhole formation and rapid undercutting. The problem associated with photoresist mask is that etch depths greater than 5 µm cannot be achieved because the photoresist eventually peels off in concentrated acids. A number of other materials such as SiC [25], polysilicon [26] and amorphous silicon [25] have been used
as masks to etch glass. Anisotropic etching of glass has also been reported by using anodically bonded silicon substrate [27].

At LSU, novel masks have been developed to etch glass. The notable ones include Mo/Cr/Au layers in conjunction with 20 µm AZ® P4620 mask, Cr/Au/electroplated Ni layers in conjunction with 20 µm AZ® P4620 mask and anodically bonded silicon mask. Etch depth of 400 µm has been readily achieved in less than 60 minutes with concentrated HF as etchant using the above mask containing electroplated Ni.

2.6 Packaging

Wafer level packaging (WLP) can be defined as a packaging technology where critical component steps of the packaging processes are carried out at the wafer level. WLP may also be utilized as a packaging technology for IC chips and can result in packaging of nearly the same size as the die. The traditional packaging process involved wafer dicing followed by individual packaging of IC chips making the packaging process costly and time consuming. WLP provides an integration of wafer fabrication, testing and some portion of packaging at wafer level, thereby benefiting from the economics of batch processing.

Wafer is fabricated first followed by packaging and dicing which is the reverse process of traditional packaging technology as shown in Fig. 2.9. Wafer level chip scale packaging (WLCSP) achieves chip scale packaging with batch processing through WLP. Other advantages of WLP include processing of die and package on the wafer before dicing, increased functionality, smaller package size and lower costs. WLCSP facilitates packaging of different die sizes on the same wafer at the same time.
WLP can be classified into zero level packaging (L0) and first level packaging (L1). The former deals with enclosing a feature on a die (silicon substrate) and the latter with enclosing the whole die at a time. The entire wafer bonding techniques belongs to L1 or level 1 packaging family.

The packaging function has many advantages and few of the important ones are as follows:
• To provide a protective cover or attach two halves of a device

• To protect sensitive electronic device from the harsh environment and provide a high level of cleanliness as the packaging cover is attached prior to dicing

• To facilitate hermetic sealing and mounting onto the final package

• To provide specialized environment ambients such as vacuum or inert gas for MEMS devices.
3. SELECTED REVIEW OF GLASS ETCHING AND ANODIC BONDING

Glass is a difficult material to etch deeply and poses serious challenges. The choice of right mask and etchant plays a vital role on the success of this project. Therefore, it is imperative to review the literature regarding techniques available to successfully etch glass. Etching of glass in this work is followed by anodic bonding. The success of the bond depends on a number of factors. So, it becomes necessary to analyze and mitigate the common problems encountered during bonding. The literature is a vital source for this information. This chapter discusses the various etch masks and etchants that have been successfully used to etch glass. Selected papers of anodic bonding and wafer level packaging have also been summarized.

Fielden et al. [24] have shown ways to fabricate smooth channel features in pyrex glass using fluorosilicic acid which is conventionally safer than hydrofluoric acid. Simpson et al. [29] have demonstrated pyrex etching using conventional Cr/Au layers in combination with photoresist as a mask. Verpoorte et al. [26] were successful in etching pyrex using polysilicon as etch mask and 49 % HF as etchant. Corman et al. [27] have presented ways for etching deep into pyrex using an anodically bonded silicon substrate as a mask. Etch depths of 500 μm in glass were readily achieved using this technique.

Torigoe et al. [30] have used HOYA SD-2 glass wafers instead of pyrex 7740 wafers and have demonstrated the compatibility of SD-2 glass wafers for anodic bonding. They also reported smoother etching using a conventional gold/chromium mask.
A research work [31] has reported that Mo is not penetrated by concentrated HF even after few minutes of exposure. Therefore, it makes a good candidate as etch mask for glass. Stadler [32] has demonstrated thinning of glass slides using buffered hydrofluoric acid (BHF) solution. The cover glass slides were dipped in the BHF solution which in turn was immersed in a water bath excited with an ultrasonic device to yield a uniform etch rate. Berthold et al. [25] have devised a two step glass etching process using a double layer mask consisting of 400 nm thick amorphous silicon and 500 nm thick PECVD silicon carbide.

Bu et al. [33] have devised a novel masking technology for deep etching in glass to a depth of more than 300 µm. The mask used is a multilayer mask comprising of Cr/Au/Cr/Au with 20 µm SPR 220-7 photoresist. The major problems associated with glass etching using thin metal films are 1) the presence of pinholes and 2) lateral undercutting due to the underetching of the Cr mask. Both problems were eliminated using the above masking technology. This etching technology has been used to fabricate microfluid devices in glass substrates.

Schjolberg-Henriksen et al. [34] have investigated both the electrical damage caused by anodic bonding on CMOS gate oxide and also ways to mitigate this problem. The solution to this problem was to etch cavities in the pyrex wafer prior to bonding it to the silicon substrate housing the CMOS device. The interface trap density and leakage current were tested after bonding. Experiments showed that the electrical damage problem caused by anodic bonding was alleviated by etching a 10 µm deep cavity in the pyrex wafer right above the circuitry in the silicon substrate and coating the cavity with aluminum which effectively resulted in a faraday cage like structure reducing
the electric field across the cavity during anodic bonding. The second method used to alleviate the electrical damage caused by anodic bonding was to etch 50 µm deep recess instead of 10 µm deep recess coated with aluminum also resulting in reduction of electric field across the gate oxide during bonding.

Choi et al. [35] have realized silicon to silicon anodic bonding by depositing pyrex glass on one of the silicon substrates by e-beam evaporation. Anodic bonding was achieved at 135 ºC and at 35 V bias. It was noticed that that the initial surface roughness of glass deposited by e-beam evaporation was higher but as the thickness of the deposited glass increased (> 1.5 µm), there was a drastic reduction in the surface roughness. Also the role of sodium ions in anodic bonding was studied in this paper.

Weichel et al. [36] have been successful in achieving a low temperature bond using silicon nitride as the intermediate layer. To improve bonding, the nitride layer was passivated with an oxide layer through an oxygen plasma treatment. Bond strengths in the order of 35 N/mm² have been achieved. Bonding was performed at a temperature of 350 – 400 ºC. This success has been attributed to the oxygen plasma treatment of the nitride film.

Visser et al. [37] have studied diffusion of gas molecules at anodically bonded interfaces. Diffusion of gases into the sealed cavity was measured during the annealing process. The annealing temperatures were varied between 150 – 430 ºC. Diffusion effects were obvious at temperatures above 350 ºC while no change in cavity pressure was observed at 300 ºC. Pressure changes of the order of 50 – 200 mbar were observed at higher temperatures and for higher annealing times.
Lee et al. [38] have studied the effects of a hydrophilic surface on anodic bonding. The wafer was pre-treated with RCA1 clean solution (DI H<sub>2</sub>O:NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub> with volume ratio of 6:1:1) to make the surface more hydrophilic. The RCA 1 treatment results in large number of hydroxyl groups on the wafer surface. The mechanism behind bonding of two hydrophilic surfaces is hydrogen bond bridging. Hence, when two hydrophilic surfaces are brought into contact, hydrogen bonds are formed almost instantly reducing the gap between the wafers. This reduction in gap induces higher electrostatic force resulting in higher bond strength and wider bonded area.

Schjolberg-Henriksen et al. [39] have investigated sodium contamination of silicon dioxide layer during anodic bonding using MOS capacitors as test structures. Contamination was detected both outside and inside the glass cavity where the MOS structures were housed. Location of the oxide and glass cavity geometry played a vital role in the amount of contamination. It was observed that the gate aluminum of MOS played a part in shielding the contamination. Applied voltage did not affect sodium contamination. A passivated layer of PECVD nitride on the MOS capacitor within the glass cavity played a vital role in shielding the MOS capacitors.

Pan et al. [40] have demonstrated use of photo-patternable materials such as SU-8 to facilitate low temperature, non-electrostatic and localized area bonding. Bonding strength of upto 213 kg/cm<sup>2</sup> has been achieved using this method.

Recent studies [41] have shown that wafer level packaging can be achieved using anodic bonding technology. Wafer level chip scale packaging for RF applications has also been achieved using adhesive bonding [42]. Metallization in silicon wafer in the above process was achieved through a two step anisotropic etching and aluminum
sputtering. WLCSP has also been achieved for power devices using low ohmic through-hole vias [43].
4. EXPERIMENTAL DETAILS

As noted in chapter 3, Lee et al. [41] have demonstrated use of anodic bonding technique to facilitate WLCSP. Anodic bonding is chosen in the present research to achieve chip level packaging. Glass and silicon etching play vital roles in this project as they facilitate dicing of the thick package, which in our case is 1.2 mm thick. A number of masks [25, 27, and 33] have been reported for etching of glass. Bu et al. [33] have successfully used a combination of Cr/Au/Cr/Au mask to etch glass. A number of novel multilayer masks have been developed for etching of glass in this research and the multilayer combination mask reported by Bu et al. [33] has been a major source of inspiration.

This chapter deals with various fabrication processes performed on glass and silicon substrates prior to bonding. These are illustrated in Fig. 4.1.

In this research, 4” diameter, 500 µm thick, (100) oriented single and double side polished, p-type silicon wafers with a resistivity of 1 – 10 Ω-cm were used. The silicon wafers were coated with 1 µm thermal oxide which served as a hard mask to etch silicon. The glass wafers used for anodic bonding were either 4” diameter, 700 µm thick double sided polished pyrex glass or 4” diameter, 800 µm thick borofloat glass. Glass etching requires a thin metal mask which was deposited either by sputtering or evaporation. The step by step process flow and methodology has been described in detail in this chapter that includes wafer cleaning, thin film deposition, spin coating, photolithography, glass and silicon wet etch process, decontamination procedures, anodic bonding and dicing.
Fig. 4.1: Illustration of various fabrication steps performed on a) glass and b) silicon.
4.1 Wafer Cleaning

In order to achieve void free anodic bonding, wafer cleaning plays a vital role. The wafers have to be extremely clean and this can be achieved using conventionally used hydrogen peroxide based cleaning techniques. Fig. 4.2 illustrates the implementation of a modified RCA cleaning procedure. The standard RCA procedure involves HF dip to strip chemical and native oxide. HF dip step was omitted in modified RCA cleaning process since the thermal oxide was used as hard mask to etch silicon.

4.1.1 Silicon Substrate Cleaning

![Diagram of modified RCA wafer cleaning process](Fig. 4.2: Modified RCA wafer cleaning process. After reference [44].)
4.1.2 Glass Wafer Cleaning

The first step in the glass cleaning process involved a solvent clean which stripped organics including photoresists. The second step involved nitric acid clean which cleaned the glass by leaching the ions from the surface. The third step was the hydrochloric acid clean which cleaned the glass by removing metal particles if any from the glass surface. The final step was aqua regia clean which stripped most of the metal on the glass surface. In order to achieve ultra clean surfaces, the glass wafers were dipped in nitric acid for 24 hours instead of 30 minutes.

![Flowchart of glass cleaning process]

**Fig. 4.3:** Standard glass cleaning technique. After reference [45].
Dilute HF was not used in the above glass cleaning process because HF attacks glass and makes the glass surface rough.

4.2 Thin Film Deposition

There are a number of methods whereby thin metal films can be deposited on the substrate. Some of the metal deposition techniques used in Electronic Material and Device Laboratory (EMDL) and at Center for Advanced Microstructures and Devices (CAMD) are thermal evaporation, e-beam evaporation, electroplating and sputtering.

Glass wet etch process requires a thin metal film mask. A number of thin metal films have been investigated for this purpose and few of the notable ones are molybdenum, gold, chromium, titanium and nickel. All of the above metals are resistant to HF and BOE which are the primary glass etchants. Molybdenum was deposited by RF sputtering at 8 mtorr and 300 W RF power for 45 minutes using Edwards 306A magnetron sputtering system. An average Mo thickness of 612 nm corresponding to a deposition rate of 13.6 nm/minute was obtained using the above deposition parameter values. The thickness of the deposited metal film was measured by Tencor alpha step 200 mechanical stylus profiler.

Stress plays a vital role in the quality of the deposited film. Excess stress causes the thin metal film to peel off the substrate or form cracks. Stadler [32] demonstrated lattice mismatch in sputtered molybdenum films using d-spacing values obtained from x-ray diffraction measurements. He observed absence of lattice mismatch when films were sputtered at 8, 17 and 25 mtorr pressure respectively and were annealed at 400 °C for 1 hour. He also observed that annealing of the deposited film was not necessary if dilute HF was used instead of concentrated HF during etching. Thus, he
concluded that molybdenum films deposited at 8 mtorr were under least strain in the absence of thermal treatment or annealing after deposition [32]. This is the justification for sputtering molybdenum at 8 mtorr sputtering pressure in this work.

Gold was deposited by resistive evaporation technique using NRC 3177 thermal evaporator. The schematic representation of a resistive evaporator is shown in Fig. 4.4. The gold slugs were placed in a tungsten boat and the chamber was pumped down to $10^{-5}$ torr. At about 18 A of current I through the tungsten boat, Au evaporation at a rate of 1.5 nm/sec was achieved. Total Au thickness of 500 nm was obtained from three 0.6 x 0.3 cm (length x diameter) gold slugs used as evaporation source. Smooth crack-free layers of evaporated Au were obtained. Chromium was used as an adhesion layer and was deposited first.

Fig. 4.4: Schematic representation of an evaporation chamber.
Nickel was deposited on pyrex glass substrate by electroplating technique. The glass wafer was metallized with chromium to define regions of deposition and was maintained at a negative potential relative to an inert anode. The substrate had to be metallized to make it conductive. The electroplating solution contained the nickel metal in aqueous form. The electrolyte used was a combination of 330 g/l nickel sulfate, 45 g/l nickel chloride and 38 g/l boric acid. The temperature of the bath was maintained at 52 °C. The pH was 3.7 and the plating rate was 0.85 µm/min. Nickel coatings of 1 and 10 µm thickness respectively were obtained by this electrodeposition technique.

Titanium and chromium were deposited using DC sputtering at 1.2 x 10⁻² torr.

4.3 Spin Coating of Photoresist

The silicon and glass substrates were coated with Microposit® S1813 and Clariant AZ® P4620 positive photoresists respectively. Microposit® S1813 resulted in an average thickness of 1.2 µm when spun at 2500 rpm for 30 seconds. AZ® P4620 resulted in an average thickness of 12 µm when spun at 2500 rpm for 60 seconds. A 20 µm thick AZ P4620 photoresist plays a vital role in attaining deep isotropic etching of glass. The process parameters for Microposit® S1813 and AZ® P4620 are illustrated in Table 4.1 and 4.2 respectively.

Table 4.1: 1.2 µm process for Microposit® S1813 photoresist.

<table>
<thead>
<tr>
<th>Step</th>
<th>Event</th>
<th>Time (sec)</th>
<th>Speed (rpm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Dispense Resist</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>Spin High Speed</td>
<td>30</td>
<td>2500</td>
</tr>
</tbody>
</table>

Soft Bake using hot plate

|    | Bake      | 5 minutes | 90 °C |

or Soft bake using conventional oven

|    | Bake      | 20 minutes | 90 °C |

36
Table: 4.2: 20+ µm process for AZ® P4620 photoresist. After reference [46].

<table>
<thead>
<tr>
<th>Event</th>
<th>Time (sec)</th>
<th>Speed (rpm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>First coat: 10+ µm thickness</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Dispense Resist</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>2 Spin Low Speed</td>
<td>3</td>
<td>300</td>
</tr>
<tr>
<td>3 Spin High Speed</td>
<td>60</td>
<td>2500</td>
</tr>
<tr>
<td>First soft bake using hotplate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Bake</td>
<td>85</td>
<td>110 °C</td>
</tr>
<tr>
<td>Second coat: 20+ µm total thickness</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Dispense Resist</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>2 Spin Low Speed</td>
<td>3</td>
<td>300</td>
</tr>
<tr>
<td>3 Spin High Speed</td>
<td>60</td>
<td>1600</td>
</tr>
<tr>
<td>Second soft bake using hotplate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Bake</td>
<td>165</td>
<td>110 °C</td>
</tr>
</tbody>
</table>

Figures 4.5 and 4.6 illustrate the spin cycles for Microposit® S1813 and AZ® P4620 photoresists.

Fig. 4.5: Spin cycle for Microposit® S1813 photoresist.
4.4 Photolithography

The substrates were removed from the oven or hotplate after photoresist coating and the stipulated soft baking cycles and were allowed to cool down for 5 minutes before proceeding with the photolithography process. A Quintel, Q-4000 UV station was used to expose the substrates under broadband UV light. The 1.2 µm thick Microposit® S1813 photoresist deposited on the silicon wafers was exposed for 20 seconds. The 20 µm thick AZ® P4620 photoresist deposited on the borofloat glass wafers was exposed for 90 seconds.

4.4.1 Mask Pattern

Different mask pattern were used in this research and are illustrated in Figs. 4.7, 4.8 and 4.9. A GCA Mann 3600 pattern generator was used for patterning standard 5” x 5” mask plates for use in optical lithography. Pattern designs were created in AutoCAD. The minimum feature size in this design was 500 µm alignment marks.

Fig. 4.6: Spin cycle for AZ® P4620 photoresist (10+ µm thickness).
Fig. 4.7: Mask for dicing of glass and silicon after bonding for unbonded sides of glass and bonded sides of silicon wafer.

Fig. 4.8: Mask for metallization.

Fig 4.9: Mask for 50 µm deep cavities on glass surface side to be bonded with Si wafer for protection of circuitry and for trenches to expose Al metal lines in silicon wafer after anodic bonding.
4.4.2 Developing and Hard Baking of Photoresist

Microposit® S1813 photoresist was developed in Microposit® 354 developer for 10-20 seconds while AZ® P4620 photoresist was developed in 1:3 AZ® 400K:DI H₂O developer for 4-5 minutes after exposure.

Microposit® S1813 was hard baked at 90 ºC for 40 minutes in a conventional oven while AZ® P4620 photoresist was post exposure baked at 110 ºC for 60 seconds in a hot plate and was left to dry in air for 10 hours. It is not advisable to hard bake thick resists like AZ® P4620 because it causes distortion of the pattern due to reflow. Also bubbles and pinholes were noticed when hard baked at 150 ºC for 30 minutes. In some cases the AZ® P4620 resist also started cracking when hard baked at high temperatures. There were also instances when the AZ® P4620 was hard baked at 90 ºC and 115 ºC for 1 hour without problems of cracking and bubble formation.

SU-8 50 polymer was applied using a disposable pipette on hard baked AZ® P4620 to prevent cracking of AZ® P4620 photoresist when dipped in concentrated HF. Sometimes, minute pinholes exist after a post-exposure bake of AZ® P4620 photoresist. When exposed to strong acids, seepage of acid was noticed through these pinholes eventually attacking the thin metal film and the glass underneath. The SU-8 polymer was used for the protection of AZ® P4620 photoresist from these HF attack. The SU-8 50 polymer was soft baked in hotplate at 110 ºC for 20 minutes and left to dry for 1 hour. The SU-8 50 polymer was not soft baked inside the oven as it resulted in the formation of bubbles. As will be seen later in section 5.4.4 that the use of SU-8 was not a good solution to this problem.
4.5 Etching Process

KOH was the primary etchant used to etch silicon with a 1 µm thick thermally grown oxide as a hard mask. Concentrated HF was the primary etchant used to etch glass. Various other concentrations of HF like 10:1 by volume DI H₂O:HF and 6:1 by volume DI H₂O:BOE were also investigated to etch glass. The various metal masks investigated for etching glass were Cr, Au, Mo, Ni, Cu and Ti.

4.5.1 Silicon Wet Etch Process

KOH etching of silicon is essentially an anisotropic wet etching process with the etching taking place preferentially for the \{100\} planes. Anisotropic etching results in V-shaped grooves with the sidewalls forming an angle of 54.74° with the surface due to the exposed \{111\} surfaces.

The total time needed to achieve a depth of 250 µm in KOH was 22 hours and 10 minutes giving an etch rate of approximately 11.3 µm/hour.

Materials used for KOH etching include:

- 4” diameter, 500 µm thick, p-type, 1-10 Ω-cm, single side polished (SSP) and double side polished (DSP), (100) silicon wafers with 1,000 nm thermally grown oxide
- KOH pellets
- Isopropyl alcohol (IPA)
- Pyrex petri dishes and cover, funnel and test tubes
- Hot plate.

KOH solutions with concentration of 20 %, 30 %, 45 % and 50 % were used to etch silicon. The recipe for 20 % KOH solution was 20 grams KOH pellets, 80 ml DI
H₂O and 20 ml IPA. The recipe for 30 % KOH solution was 70 grams KOH pellets, 190 ml DI H₂O and 40 ml IPA. The recipe for 45 % KOH solution was 45 grams KOH pellets, 80 ml DI H₂O and 20 ml IPA and that of 50% KOH solution was 50 grams KOH pellets, 80 ml DI H₂O and 20 ml IPA. Addition of IPA increased the anisotropy in the etch. DI H₂O was added to the KOH pellets first and the solution stirred on a warm surface so that the KOH pellets dissolved. This was followed by addition of IPA and a layer of IPA was found floating on top. The 150 x 20 mm pyrex petri dish was immediately covered with the glass cover and the temperature of the hot plate was raised to the process temperature of 50 ºC. The stirrer on the hot plate was maintained at 600 rpm.

Silicon etching requires a hard mask of silicon dioxide, nitride or thin metal films. In this research, silicon dioxide of 1 µm thickness was used as mask to etch silicon anisotropically. The thermal oxide wafers were RCA cleaned and patterned with 1 µm thick Microposit® S1813 photoresist. The exposed oxide was etched with 6:1 by volume DI H₂O:BOE solution. The etch rate of the oxide in BOE was 66.7 nm per minute. The back side of the wafer was protected by Harman Corporation’s polyester masking discs. These masks totally eliminated pinholes on the back side of the wafer and gave a superior protection against attack by BOE. After the oxide was etched, the polyester mask was removed and photoresist was stripped using acetone followed by IPA rinse. A great difference in surface morphology of silicon surface was noticed with and without piranha cleaning immediately after photoresist stripping. Without piranha cleaning, hillocks were observed during KOH etching. However, cleaning the wafers in a mixture of 1:1 by
volume H₂SO₄:H₂O₂ prior to etching resulted in a mirror smooth etched surface. Piranha cleaning was followed by through rinsing in DI H₂O.

The patterned wafer, after the DI H₂O rinse in the previous step, was placed in KOH solution and the KOH solution bubbled at the exposed silicon sites while etching. The etch rates, surface morphology and depths achieved will be discussed in detail in section 5.3 in chapter 5.

4.5.2 Glass Wet Etch Process

Etching of glass by HF is essentially an isotropic etching process with the etch rate being equal in all directions since glass is amorphous. Etching of glass with HF generally results in a rough surface but in this work it was observed that addition of HCl and HNO₃ to concentrated HF results in a smoother surface.

Approximately in 60 minutes, depth of 432 µm was etched in 48 % HF giving an etch rate of 7.2 µm/min.

Materials used for glass etching include:

- 4” diameter, 800 µm thick, DSP, borofloat glass wafers and 4” diameter, 700 µm thick, DSP, pyrex glass wafers
- Teflon container and stirrer as HF attacks glass containers
- 48 % HF, 70 % ACS HNO₃ and H₂SO₄
- Harman Corporation’s polyester masking discs.

A layer of 20 µm of AZ® P4620 photoresist by itself and a combination of 20 µm of AZ® P4620 photoresist and SU-8 50 were used as masks to protect thin metal film masks from peeling off during glass etching in concentrated HF. The metal masks used for glass etching were molybdenum, chromium, gold, electroplated nickel and titanium.
The back side of the glass wafer was protected by a double layer comprising of Cr and Harman Corporation’s polyester masking disc.

The patterned glass wafer was placed in concentrated HF solution. It is important that all necessary precautions such as rubber gloves, goggles and necessary clothing be donned because HF poses a great health hazard. The glass was etched at a rate of approximately 7 µm per minute, the details of which will be discussed in section 5.4 in chapter 5.

4.6 Decontamination Procedures

KOH etching of silicon is not CMOS compatible because alkali ion cause instabilities in MOS devices. It becomes imperative to decontaminate the substrates to make it CMOS compatible. To achieve successful anodic bonding, the glass and silicon substrates must be ultra clean and a number of decontamination techniques are commercially available. In this research, hydrogen peroxide based cleaning techniques were used to decontaminate the substrates.

The cleaning process of silicon was divided into four stages. The first stage involved BOE dip. The concentration used was 6:1 by volume DI H2O:BOE. The native and thermal oxides can trap a number of impurities during different stages of microfabrication. So, stripping these oxide layers gets rid of these trapped impurities. The second stage included RCA 1 cleaning which involved heating the silicon substrate in a mixture of 5:1:1 by volume of H2O:H2O2:NH4OH at 75 ºC for 10 minutes. RCA 1 cleaning step strips organic and metal particles. This was again followed by BOE dip to strip any oxide formed. The third stage was RCA 2 cleaning which involved heating the substrate in a mixture of 6:1:1 by volume of H2O:H2O2:HCl at 75 ºC for 10 minutes.
RCA 2 cleaning step strips alkali ions and metal particles. The fourth and final stage was piranha cleaning which involved heating the silicon substrate in a self heating mixture of 2:1 by volume of H₂O₂:H₂SO₄ at 120 ºC for 20 minutes. The piranha cleaning process oxidizes the wafer and hence the wafer undergoes another BOE dip to strip the oxide. This was followed by thorough rinsing in DI H₂O and blow drying in nitrogen. DI H₂O rinse was performed between every stage of silicon wafer cleaning process.

Decontamination procedures for glass involved the same steps as silicon wafer cleaning except that the BOE dip steps were omitted. Prior to bonding, the glass wafer was placed in fuming nitric acid for 10 minutes and then rinsed in running DI H₂O for 10 minutes. This cleaning process removes most particles from the glass wafer.

4.7 Metallization Using Lift-off Process

Electrical connection through a bonded package can be achieved either through lift off process or by etching of deposited metal. Lift-off of metal is judged to be better suited for this process here. The wafers have been thoroughly cleaned in the previous steps removing all organic, alkali ions and metal particles. So, it becomes imperative that metal is not deposited directly on the wafer everywhere and deposited only on small areas where necessary. Presence of metal over large area may inhibit proper bonding and also removal of unneeded metal poses a great problem after metallization is achieved. None of the hydrogen peroxide based cleaning techniques can be used for cleaning of wafers once metallization has been achieved. Aluminum metal is attacked by RCA 1, RCA 2 and piranha cleaning solutions.

The lift-off process used here comprised of the following steps: 1) Microposit® S1813 photoresist is first spin coated on the silicon wafer. 2) Photoresist is
soft baked for 10 minutes at 90 °C. 3) Photoresist is exposed and developed in Microposit® 354 developer to define the pattern. 4) The metal is deposited by e-beam evaporation and 5) the wafer is soaked in acetone to aid in lift-off. During the lift-off process, the acetone penetrates the photoresist, thus lifting off both photoresist and the undesired metal leaving behind only the metal film which was deposited directly on the substrate. Fig. 4.10 clearly illustrates the photoresist based lift-off process to achieve metallization.

![Diagram of the lift-off process](image)

**Fig. 4.10:** Illustration of photoresist based lift-off process to achieve metallization. After reference [2].

### 4.8 Anodic Bonding

An AML 402 HVP bonder shown in Fig. 4.11 was used to achieve anodic bonding. The AML 402 bonder has the capability to perform anodic, direct and intermediate layer bonding. Important features of the AML 402 wafer bonder include a high vacuum process chamber, in-situ wafer alignment system and automated and manual mode selection to achieve anodic bonding.

A graphical user interface (GUI) as shown in Fig. 4.12 is used to operate the AML 402 HVP wafer bonder. It has two modes of operation. In the automatic mode, all the parameters are pre-set by the user and there is minimum human intervention. In the manual mode, the user controls the process directly.
The default mode of operation is the automated anodic bonding mode. Once the automated anodic bonding tab on the GUI shown above is clicked, the software presents a set of process parameters such as operating conditions, bonding parameters, vacuum pump parameters, tolerances and temperatures required for bonding. The GUI
that displays the above mentioned parameters is illustrated in Fig. 4.13. These default configuration parameters are suited for a typical bonding procedure. However, the parameters can be edited to suit one’s needs and saved to a configuration file. The various configuration files can be recalled using the load parameters tab (#1 in Fig. 4.13) on the GUI. When the required parameters are loaded, the done tab (#2 in Fig. 4.13) on the GUI is clicked which opens up a control panel as shown in Fig. 4.14.

Fig. 4.13: GUI display showing the various parameters required for bonding.

Once the start tab on the control panel is clicked, the bonding will take place with minimum human intervention. The switching to manual mode is also possible at any stage during automated bonding. There are six stages in the anodic bonding process. These are: 1) Pumping down of the vacuum chamber; 2) Heating to the operating temperature of 380 ºC and pumping down of the vacuum chamber to the operating pressure of 1x10⁻³ mbar; 3) In-situ alignment of wafers and application of a force of the order of 100 N; 4) Ramping up the voltage to 1 kV and applying a current of 8 mA; 5)
Bonding at constant voltage and 6) Completion of the process and cooling of platens using forced nitrogen cooling.

![Fig. 4.14: Control panel for automated bonding.](image)

The glass is always loaded on the top platen and the silicon on the bottom platen. This concept is illustrated in Fig. 4.15. There are grooves present in the platens of the wafer bonder and the wafer flat is aligned with this groove to ensure alignment marks are in correct orientation relative to the viewing apertures of the camera. The alignment marks should be symmetrical on the wafer separated by a distance of $67 \pm 5$ mm. The glass on the top platen is gently held by two screw stops mounted on the platen and a glass clamp, which can be retracted to release the glass wafer. It is very important that both the lower and upper platens do not come in contact when the lid is closed.
Before loading the wafers to facilitate bonding, certain procedures need to be carried out on the wafer bonder to ensure a good quality bond. These include adjusting the parallelism of the platens and zeroing the force and height of the wafer bonder. The upper and the lower platens must be parallel to one another and extreme care must be taken to maintain the parallelism, otherwise uniform force will not be applied throughout the wafer drastically affecting the bond quality. It is also important to zero the force and height of the wafer bonder. With the chamber under vacuum, the voltage on the manual control panel shown in Fig. 4.16 was set to 20 V and current set to 1 mA (#1 in Fig. 4.16) and the HV switch was enabled on the control panel (#2 in Fig. 4.16). The lower platen was raised slowly until it touched the upper platen and resulted in a HV trip. At this point of contact between the upper and the lower electrode, the “zero platen” button on the control panel was clicked to zero the platen (#3 in Fig. 4.16). This was followed by zeroing the digital indicator on the manipulator by disconnecting and reconnecting the lead in order to achieve synchronization with the PC display. To zero the setting at the
point where the wafers touch, the following procedure was followed. Silicon thickness (mm) + glass thickness (mm) – platen screw height (mm) = difference (mm). Now the bottom electrode was lowered to read this difference and re-zeroed as above. After the above adjustments were performed, the wafers were loaded and automated anodic bonding was performed as described earlier in the section.

4.9 Dicing

The glass wafer that was anodically bonded to silicon substrate was diced at the corners to expose the metal lines. The corner areas of the glass were etched on back side of the wafer such that bonding was not achieved in these areas to dice and expose the metal lines on silicon as illustrated in Figs. 4.17 (a) and (b) respectively. The scribing of the glass was achieved using a diamond scribe.

Fig. 4.16: Control panel for manual bonding.
Fig 4.17: (a) Top view of anodically bonded glass-silicon package. (b) Cross section view along A-A’ of anodically bonded glass/silicon package with trenches to facilitate dicing.
5. RESULTS AND DISCUSSIONS

Etching of glass and silicon, as mentioned in chapters 3 and 4, play vital roles in this research as they facilitate dicing of the anodically bonded thick package. The etched trenches on the silicon surface and the etched channels on the glass and silicon are analyzed using a Hitachi S-4500II Field Emission Scanning Electron Microscope (SEM) and Nikon Optiphot-88 Optical Microscope.

5.1 Temperature and KOH Concentration Dependence of Silicon Etch Rates

KOH was the primary etchant used to etch silicon in this work. It was observed that etch rate of silicon depended primarily on bath temperature and KOH concentration by weight in deionized water. Silicon etchings were performed at concentrations of 20 %, 30 %, 45 % and 50 % KOH by weight in deionized water and at bath temperatures of 50 ºC, 60 ºC, 70 ºC and 80 ºC.

5.1.1 Effect of Temperature on Silicon Etching

Figure 5.1 demonstrates the dependence of silicon etch rate on bath temperature. It is seen from Fig. 5.1 that the etch rate increases with bath temperature regardless of KOH concentration and is highest for 80 ºC, which is the highest temperature used. With the obtained experimental data, it can also be concluded that the etch rate decreases with KOH concentration levels above 20 % and is the highest for 20 % concentration at 80 ºC.

5.1.2 Effect of KOH Concentration on Silicon Etching

Figure 5.2 illustrates the dependence of etch rate as a function of KOH concentration by weight in deionized water. It is clear from Fig. 5.2 that KOH concentration has smaller effect on etch rate when compared to bath temperature. From
Figs. 5.1 and 5.2, an important observation can be made that etch rate dependence on KOH concentration at 50 °C is negligible, which is consistent with Seidel’s results [17]. However, KOH concentration plays a vital role on surface roughness (R_a) during etching. With decrease in KOH concentration typically less than 30 %, R_a increased considerably. In this research, KOH concentration of 45 % and a bath temperature of 50 °C were used to etch silicon. These parameters resulted in deep trenches, sharp edges and smooth surfaces as shown later in section 5.3.

![Fig. 5.1: Etch rate of silicon as a function of bath temperature.](image1)

![Fig. 5.2: Etch rate of silicon as a function of KOH concentration by weight.](image2)
Seidel et al. [17] have deduced an empirical formula that is in close agreement with the experimental data observed in this work. Seidel’s empirical formula gave etch rate of silicon in µm/hour \( R = k_o [H_2O]^4 [KOH]^{1/4} e^{-E_a/kT} \) where \( k_o \) is a constant in µm/hour, \([H_2O]\) is the water concentration, \([KOH]\) is the KOH concentration, \( E_a \) is the activation energy in eV, \( k \) is the Boltzmann constant and \( T \) is the etching temperature. They concluded that silicon etch rate is mainly a function of water concentration. From the experimental data obtained in this research, which are consistent with Seidel’s results [17], one can conclude that etch rate varies with the fourth power of water concentration for high KOH concentration. High KOH concentration is required to remove the native silicon dioxide from the surface and also increase the solubility of a byproduct, Si(OH)\(_4\) complex, formed during silicon etching.

5.2 Temperature and KOH Concentration Dependence of Silicon Dioxide Etch Rates

KOH concentration and bath temperature are important parameters to be taken into consideration during silicon etching with oxide as mask since these parameters also significantly affect the silicon dioxide layer. So, it is important to choose the right temperature and concentration. Lower concentration and lower temperature would be typically desired as it results in slower etching of passivation layer which is desirable for etching deep channels in a silicon substrate. However, lower temperature and concentration are unacceptable in many cases as they result in rough surfaces during etching. It has been observed that at 45 % KOH concentration, 50 °C bath temperature and with 1 µm thick oxide mask, not only excellent, smooth mirror like surfaces are obtained but also an etch depth of 355 µm in silicon can be achieved without significant difficulty with few hundreds of nanometer thick oxide mask still adhering to the silicon
surface as shown in Fig. 5.3. The oxide etch rate in KOH for this case appears to be somewhat lower than measured without any simultaneous silicon etching in section 5.3, Table 5.2.

5.2.1 Effect of Temperature on Silicon Dioxide Layer

Figure 5.4 demonstrates the dependence of silicon dioxide etch rate on the etching temperature. It is a noteworthy observation from Fig. 5.4 that silicon dioxide etch rate is highest for 30 \% KOH concentration by weight in deionized water from among the four different concentration values used.

![Fig. 5.3: (a) Digital image of etched silicon channel of 355 µm depth and (b) few hundreds of nanometer thick silicon dioxide hard mask adhering to the silicon surface after Si etching.](image)

![Fig. 5.4: Etch rate of silicon dioxide as a function of bath temperature.](image)

Fig. 5.3: (a) Digital image of etched silicon channel of 355 µm depth and (b) few hundreds of nanometer thick silicon dioxide hard mask adhering to the silicon surface after Si etching.

Fig. 5.4: Etch rate of silicon dioxide as a function of bath temperature.
Etch rate (R) in Fig. 5.4 increases with temperature consistent with Arrhenius equation given by $R = A \exp (-E_a/kT)$, where $R$ is the etch rate in nm/hr, $A$ is the pre-exponential factor in nm/hr, $E_a$ is the activation energy in eV or kJ/mol., $k$ is the boltzmann constant and $T$ is the bath temperature.

**5.2.2 Effect of KOH Concentration on Silicon Dioxide Layer**

Seidel et al. [17] have observed in their experimental work that the silicon dioxide etch rate increases linearly at low values of KOH concentration and for high KOH concentration above 35 %, the etch rate decreases with the square of the water concentration, indicating a role of water in the reaction. A similar trend was observed in this research with the etch rate of silicon dioxide being maximum for 30 % KOH concentration among the different concentrations used as shown in Fig. 5.5. Seidel et al. [17] attributed the decrease in etch rates at higher KOH concentration values to negative charge build up on the oxide surface. It is known from the literature that at a pH value of 2.8, there is zero charge at the silicon dioxide electrolyte interface [47]. Above this pH value or at high KOH concentration, there is a build up of negative charge on the oxide surface. It is the presence of this charge that hinders the diffusion of hydroxide ions to the silicon surface. Hence, it is believed that water molecules play a major role in the reaction at high KOH concentration above 35 % and hence the etch rate decreases with the square of the water concentration [17]. The linear dependence of silicon dioxide etch rate at low KOH concentration below 35 % can be explained by a pure chemical reaction of silicon dioxide with hydroxide ions given by the following equation [17]:

$$\text{SiO}_2 + 2 \text{OH}^- \rightarrow \text{SiO}_2(\text{OH})_2^-.$$
5.3 Observations During Silicon Etching

This section describes in detail various observations and problems encountered during silicon etching. As described earlier, a bath temperature of 50 °C and KOH concentration of 45 % by weight was determined to be the most suitable for this work. It resulted in deep trenches, sharp edges and smooth surfaces. Figure 5.6 shows smooth etched surfaces that were achieved using a bath temperature of 50 °C and KOH concentration of 45 % by weight. Trenches 355 μm deep with sharp edges along channels were also observed using the above parameters and are illustrated in Figs. 5.7 - 5.9.
Fig. 5.6: Microphotograph of smooth etched surfaces obtained at 50 °C temperature and 45 % KOH concentration by weight. (a) Magnification approximately x 100. (b) Magnification approximately x 25.

Fig. 5.7: SEM micrographs of a 355 μm deep trench which is used to align silicon with similar alignment trenches in glass during bonding.
Fig. 5.8: SEM micrograph of sharp edges observed in the trenches with etching carried out in 45 % KOH concentration at 50 °C.

Fig. 5.9: Outer and inner edges of silicon etched at 50 °C in 45 % KOH concentration. (a) Microphotograph of outer edge of etched silicon (magnification x 100). (b) SEM micrograph of top edge of sidewall in etched channel. (c) Microphotograph of inner edge of etched silicon (magnification x 100). (d) SEM micrograph of bottom edge of sidewall in etched channel.
A number of problems were encountered during silicon etching. The first major problem was the back side of the silicon wafer protected by the oxide layer being riddled with pinholes after etching of silicon in KOH solution. This problem was attributed to bubble formation in Shipley 1813 photoresist during hard baking which resulted in attack of the oxide layer underneath the bubbles during oxide etch of patterned areas using BOE. Thus, the silicon was exposed resulting in a large number of tiny pinholes during KOH etching. A number of solutions are proposed to eliminate this problem including 1) ramping of temperature in small incremental steps of 5 ºC during hard baking of photoresist, 2) sealing the silicon backside with Harman Corporation’s paint mask which is basically a polyester film and highly resistant to HF and 3) allowing the hard baked photoresist to cool down slowly for 1 – 2 hours before BOE exposure. This problem of pinholes was completely resolved by using a polyester film mask on the back side of the wafer as illustrated in Fig. 5.10.

Undercutting of convex corners was visible during silicon etching. The actual phenomenon of undercutting is still not entirely understood. It has been observed that undercutting depends on two parameters namely the total etch time and the surface area attacked by KOH. Fig. 5.11 illustrates the phenomenon of undercutting of convex corner.

The third problem faced during silicon etching was formation of hillocks even at concentration as high as 45 % KOH solution. The problem of hillock formation during silicon etching at 45 % KOH concentration was eliminated by dipping patterned silicon wafer in piranha solution (1:1 by volume H₂SO₄:H₂O₂) for 10 minutes at 120 ºC. It was observed that there was a great difference in surface roughness and finish with and without piranha cleaning prior to and in between etching as illustrated in Fig. 5.12.
Silicon was subjected to piranha cleaning before etching and intermittently after every 6 hours of KOH etching. The total etch time being 22 hours and 10 minutes for the case shown.

Fig. 5.10: Illustration of pinhole formation and remedy. (a) The back side of the silicon wafer riddled with pinholes (magnification x 22). (b) Harman Corporation’s polyester mask that assisted in the complete elimination of pinholes during oxide strip in BOE. (c) Pinhole free silicon wafer observed after etching in 45 % KOH concentration at 50 ºC. (d) Microphotograph of pinhole free silicon surface after etching in 45 % KOH concentration at 50 ºC (magnification x 22). Wafer diameter is 4”.

Fig. 5.11: Microphotograph of undercutting of convex corner (magnification x 18).
Fig. 5.12: Surface finish with and without piranha cleaning prior to and in between KOH etching. a) Microphotograph of formation of hillocks on KOH etched surface for which no piranha treatment was carried out prior to etching (magnification x 22). (b) Microphotograph of smooth etched surface for which piranha treatment was carried out prior to and in between KOH etching (magnification x 100).

An explanation to this hillock problem may lie in hindrance to etching due to polymerization of the reaction products, mainly Si(OH)₄. This polymerization will result in the formation of covered areas on the surface and prevent KOH etchant from reaching the silicon surface [48]. Another hypothesis attributes origination of the hillocks to gas bubbles [49]. The bubbles are composed of gaseous reaction products and the surface remains protected from the etchant as long as these bubbles remain on the silicon surface resulting in the formation of hillocks dubbed “bubble hillocks”. It is not obvious why and how the piranha treatment of silicon wafers prior to and in between etching gets rid of these polymerization of the reaction products or the gaseous reaction products resulting in smooth, mirror like surfaces.

White residue formation on the silicon surface was observed when etched in 45 % KOH concentration. This may be attributed to the dissolution rate of silicon atoms being much higher than the transport rate of the Si(OH)₄ complex into the bulk solution. When the concentration of this complex on the silicon surface becomes high,
polymerization occurs and forms residue on the surface [17]. The white residue was however removed by a piranha cleaning treatment. This is illustrated in Fig. 5.13.

![Image of white residue formation](image)

**Fig. 5.13:** White residue formation observed during silicon etching in 45 % KOH concentration at 50 °C. Wafer diameter is 4”.

A number of deposits were noticed on the etched silicon surface when viewed under the optical microscope which was probably reaction products. The parameters used for silicon etching were 45 % KOH concentration by weight in deionized water and 50 °C etching temperature. However, once the substrate was cleaned and decontaminated, smooth, mirror surfaces were obtained. This is illustrated in Fig. 5.14.

Etching at 20 % KOH concentration and high bath temperature of 80 °C resulted in very rough surfaces as shown in Fig. 5.15 and these observations were consistent with Seidel’s results [17].

The location of trenches for subsequent scribing along the cleavage axis created a significant problem since application of a little bit of extra pressure on the cleavage axis resulted in breakage during handling of silicon wafers. This problem was mitigated by reducing the silicon etch depth from 355 µm to approximately 230 µm. The
nominal silicon wafer thickness used was 475 – 500 µm. The depth was measured using a Tencor 500 alpha step mechanical stylus profiler as shown in Figs. 5.16 and 5.17.

Silicon and silicon dioxide used as etch mask had varying etch rates at different bath temperatures and KOH concentrations. The observed average etch rates are summarized in Table 5.1 and 5.2 respectively. For measurement of these etch rates 10 ml of DI H₂O was added to the solution every 12 hours to compensate for evaporation.

Fig. 5.14: Surface treatment of etched silicon surface. (a) Surface etched in KOH prior to RCA treatment (magnification approximately x 25) (b) Etched silicon surface subjected to RCA treatment resulting in mirror smooth surface and removal of reaction products (magnification approximately x 25).

Fig. 5.15: Rough surfaces observed during silicon etching at 20 % KOH concentration at 80 °C (magnification approximately x 25).
Fig. 5.16: Depth of 355 µm measured using a Tencor 500 alpha mechanical stylus profiler.

Fig. 5.17: Depth of 237 µm measured using a Tencor 500 alpha mechanical stylus profiler.

Table 5.1: Approximate etch rates of (100) silicon in µm/hour for various bath temperature and KOH concentration by weight in deionized water.

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<th>KOH conc.</th>
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<td>50 %</td>
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Table 5.2: Approximate etch rates of silicon dioxide in nm/hour for various bath temperature and KOH concentration by weight in deionized water.

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<th>KOH conc.</th>
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5.4 Observations During Glass Etching

Until the year 2002, the effective depth etched in glass without pinhole formation using a metal mask was 50 µm. Bu et al. [33] however broke this barrier using a novel multilayer metal mask of Cr/Au/Cr/Au and readily achieved depths of 300 µm. Selective etching of glass is challenging in that metal masks must be resistant to HF. In this work, a number of metal layers were tested for their stability against etching solution to be used as etch masks.

The following combinations of metal and photoresist layers were investigated for etching pyrex glass in this research. These are: 1) Cr (200 nm) layer below 20 µm thick AZ® P4620 photoresist layer, 2) Ti/Mo combination (100 nm Ti/600 nm Mo) layers below 1 µm Microposit® S1813 photoresist layer, 3) Mo/Cr/Au combination (600 nm Mo/200 nm Cr/50 nm Au) layers below 20 µm AZ® P4620 photoresist layer, 4) Cr/Au/Cr/Au combination (200 nm Cr/500 nm Au/200 nm Cr/50 nm Au) layers below 20 µm AZ® P4620 photoresist layer, 5) Cr/electroplated Ni combination (200 nm Cr/1 µm Ni) layers below 20 µm AZ® P4620 photoresist layer, 6) Cr/Au/electroplated Ni combination (200 nm Cr/50 nm Au/10 µm Ni) layers below 20 µm AZ® P4620 photoresist layer, 7) Cr/Mo combination (200 nm Cr/600 nm Mo) layers below 20 µm
AZ® P4620 photoresist layer and 8) anodically bonded silicon mask. In each case above, the first listed metal touches the silicon surface and is at the bottom followed by the next listed metal layer. The photoresist layer is on the top.

The 20 µm thick AZ® P4620 photoresist was deposited by spin coating technique. AZ® P4620 resulted in an average thickness of 12 µm when spun at 2500 rpm for 60 seconds. To obtain total thickness of 20 µm, AZ® P4620 was spun at 2500 rpm for 60 seconds, soft baked at 110 °C for 85 seconds, re-spun at 1600 rpm for 60 seconds and soft baked at 110 °C for 165 seconds. The hard baking of AZ® P4620 was carried at 115 °C for 60 minutes. Molybdenum was deposited by RF sputtering technique at 8 mtorr and 300 W RF power for 45 minutes using Edwards 306 A magnetron sputtering system. An average Mo thickness of 612 nm corresponding to a deposition rate of 13.6 nm/minute was obtained using the above deposition parameters. Au was deposited by resistive evaporation technique using NRC 3177 thermal evaporator at a rate of 1.5 nm/sec. Cr and Ti were deposited using DC sputtering at 1.2 x 10⁻² torr and 200 W power at a rate of approximately 10 nm/min. Ni was deposited on pyrex glass substrate by electroplating technique with a deposition rate of 0.85 µm/min. The electrolyte used was a combination of 330 g/l nickel sulfate, 45 g/l nickel chloride and 38 g/l boric acid. The temperature of the bath was maintained at 52 °C. The pH was 3.7. Ni coating of 1 and 10 µm thickness respectively was obtained by this electrodeposition technique.

The 20 µm thick AZ® P4620 photoresist played a vital role in protecting the metal mask from HF attack. Various etchants such as undiluted 48 % HF; 50:5:1 by volume HF:HCl:HNO₃ combination; 10:1 by volume DI H₂O: HF; and 6:1 by volume DI H₂O: BOE were investigated in this research for preferential etching of glass. Undiluted
48 % HF was investigated on all the above-mentioned metal/photoresist layer mask combinations. BOE was investigated on Mo/Cr/Au with AZ® P4620 photoresist mask. Dilute HF (10:1 by volume DI H2O: HF) was investigated on Cr/Mo with AZ® P4620 photoresist mask. 50:5:1 by volume HF:HCl:HNO3 combination was investigated on Cr/electroplated Ni with AZ® P4620 photoresist mask and on Cr/Mo with AZ® P4620 photoresist mask.

Deep isotropic etching of glass was possible only through the use of undiluted 48 % HF. Diluted and buffered HF resulted in poor edges and had very long etch times which will be illustrated later in this section. Commercial solution (Transene Cr 1020 A) was used to etch Cr for opening windows in Cr layer. Aqua regia (3:1 by volume HCl:HNO3) was used to open windows in Ni, Au and Mo. Commercial solution (Transene Au TFA) was also used to etch Au. Commercial solutions Microposit® 354 and AZ® 400 K were used to open windows in the exposed S1813 and AZ® P4620 photoresists respectively. The etch rates of all the metals used in this research as etch masks for preferential glass etching is illustrated in Table 5.3 in section 5.4.8.

5.4.1 Cr with AZ® P4620 Photoresist Mask

It was noticed that with Cr (200 nm)/20 µm AZ® P4620 photoresist combination as a selective etch mask, etch depths in glass up to 60 µm could be achieved without difficulty using undiluted 48 % HF. However, for etch depths greater than 60 µm, seepage of acid was noticed through minute pinholes in the photoresist that eventually attacked the Cr mask and subsequently the glass underneath. These observations are illustrated in Fig. 5.18.
5.4.2 Ti/Mo with Shipley 1813 Photoresist Mask

It has been observed that pinholes on the photoresist can be a serious disadvantage especially for deep glass etching using metal masks. Hence, spinning and baking cycles for photoresist deposition play a vital role in prevention or reduction of pinholes. Here, 100 nm Ti was used as an adhesion layer on glass with 600 nm Mo over the Ti layer. One µm thick Microposit® Shipley 1813 photoresist is deposited over the Mo layer. For this study, undiluted 48 % HF was used as the etchant. It was observed that the 48 % HF seeped through Shipley 1813 mask and attacked both the Mo and Ti layer. It has been observed in this work that Mo can withstand 48 % HF for a few minutes after which HF starts stripping the Mo and attacking the layer underneath. Ti is instantly attacked by 48 % HF at a rate of 2400 nm/minute. It was observed in this research that 48 % HF attacked Ti adhesion layer through the opened windows and stripped both the Ti and Mo layer from underside as illustrated in Fig. 5.19 (a). The extent of HF attack on the protected glass surface is illustrated in Fig. 5.19 (b).

Fig. 5.18: Effect of HF on Cr/ AZ® P4620 mask. (a) Smooth edges achieved using Cr mask (magnification x 15). (b) Pinhole formation on protected glass surface for etch depths beyond 60 µm (magnification x 70). (c) Cross-sectional view along A-A’.
The protected glass surface exposed to HF due to ripping of Ti mask was very rough as shown in Fig. 5.20. A small number of large pinholes were also observed on the protected glass surface when viewed under the optical microscope as shown in Fig. 5.21.

Fig. 5.19: Illustration of HF attack on Ti/Mo layers under 1813 photoresist. Wafer diameter is 4”. (a) Stripping of Mo/Ti mask by 48 % HF. (b) Extent of attack on the protected glass surface after the metal was stripped.

Fig. 5.20: Microphotograph of protected glass surface shown in Fig. 5.19 (b) due to HF attack (magnification approximately x 25).
5.4.3 Mo/Cr/Au with AZ® P4620 Photoresist Mask

Mo/Cr/Au multilayer novel mask combination, developed in this research, has been successful in achieving etch depths in glass greater than 200 µm. The mask comprises of 600 nm Mo in contact with glass with 200 nm of Cr above Mo and 50 nm of Au on Cr followed by 20 µm of AZ® P4620 photoresist. Two etchant solutions were tried. One comprising of undiluted 48 % HF and the other comprising of 6:1 by volume DI H₂O:BOE. The results for 6:1 by volume DI H₂O:BOE is provided in section 5.4.8. The depth and the lateral undercutting were measured using a Tencor 500 alpha step profiler. Figures 5.22 and 5.23 respectively show typical step-profile results of etch depth and lateral undercutting. Undiluted HF could not penetrate this novel mask even after 30 minutes of exposure. However, very high surface roughness was observed on the etched surface areas as shown in Fig. 5.24. This is attributed to the use of 48 % HF. Pinhole free surfaces and smooth edges were achieved in areas masked by this novel mask which is illustrated in Fig. 5.25.
Fig. 5.22: Etch depth of 216 µm measured using Tencor 500 alpha step profiler with undiluted 48 % HF.

Fig. 5.23: Measurement of the lateral width for the etched area in undiluted 48 % HF used for calculating undercutting in glass.
Fig. 5.24: Rough surfaces observed during etching of glass in undiluted 48 % HF (magnification approximately x 25).

In order to investigate the undercutting of glass using this novel mask, the following calculations were done. The nominal designed channel width opening for etching was 3 mm. The width achieved after etching was 3.487 mm. The difference between original and the achieved width is 487 µm. Half of number gives value for estimated lateral undercutting on each end. Therefore, the lateral undercutting is 243.5 µm while the etch depth is 216.3 µm. The aspect ratio, defined as the ratio of the etch depth to the lateral undercutting is 0.88 which is better than that achieved by either using a silicon mask or a Cr/Au/Cr/Au combination mask. The reported aspect ratio for the above two masks are 0.66 [27] and 0.78 [33] respectively.

5.4.4 Cr/Au/Cr/Au with AZ® P4620 Photoresist and SU-8 Polymer Mask

For this case, first 200 nm of Cr is deposited on glass successively followed by 500 nm of Au, 200 nm of Cr and 50 nm of Au. Twenty µm thick AZ® P4620 photoresist is then deposited on the top of these four metal layers. After achieving hard baking of AZ® P4620 photoresist at 115 ºC for 60 minutes, the AZ® P4620 photoresist layer was coated with SU 8-50 polymer using a disposable pipette and soft baked on a hot plate at 110 ºC for 20 minutes. This mask was used in conjunction with etching solution
comprising of undiluted 48 % HF. However, after few minutes of exposure in concentrated HF, the SU 8 polymer along with the top 50 nm Au layer were seen to peel off. This may be attributed to the fact that the SU 8 polymer layer was not hard baked for a sufficiently long time thereby lifting off along with the underlying AZ® P4620 photoresist layer and the Au layer as illustrated in Fig. 5.26. Hence, no further studies were made on this mask in this work.

![Fig. 5.25: Effect of undiluted 48 % HF on areas protected by Mo/Cr/Au with AZ® P4620 mask. (a) Pinhole free protected glass surface upon removal of the mask after etching (magnification approximately x 25). (b) Smooth edges seen on the etched alignment trench using the above novel mask (magnification approximately x 64).](image1)

![Fig. 5.26: Illustration of SU 8 layer lift-off along with underneath Au layer exposing Cr layer. Wafer diameter is 4”](image2)
5.4.5 Electroplated Ni with AZ® P4620 Photoresist Mask

This novel mask developed in this research involved 200 nm Cr on glass followed by electroplated Ni. Both 1 µm and 10 µm thick electroplated Ni were investigated. As before, AZ® P4620 photoresist was used not only for patterning the metal mask but also for providing protection against 48 % HF. With a 10 µm thick electroplated Ni, etch depths greater than 400 µm in glass have been achieved in this work without any pinhole formation as shown in Fig. 5.27 using 48 % HF as etching solution. However, surface roughness on the etched areas was high because of the use of concentrated HF. Thus, the earlier barrier of 300 µm using metal mask has been broken in this work and a novel metal mask has been devised to achieve etch depths greater than 500 µm without any pinhole formation in the mask in this research.

Fig. 5.27: Effect of HF on 10 µm electroplated Ni mask. (a) Absence of pinholes on protected glass areas after removal of mask upon etching. (b) Very high surface roughness on etched glass surface. Magnification approximately x 25 for (a) and (b).

Figures 5.28 and 5.29 show etched area profiles from a stylus profilometer. From Fig. 5.28, it can be seen that the etching profile on one end labeled #1 in Fig. 5.28 seems to be less isotropic compared to the other end labeled #3 in Fig. 5.28. Also, very high surface roughness on the etched areas was observed as illustrated by #2 in Fig. 5.28.
The etched window width shown in Fig. 5.29 was 4.736 mm when compared to the original nominal designed window width of 3 mm. This gives a lateral undercutting of 868 µm for the etch depth of 435.3 µm. Aspect ratio, defined as the ratio of the etch depth to the lateral undercutting is 0.50. Even though the aspect ratio is smaller than that achieved by Bu et al. [33], one has to take into account the higher etch depth achieved using this novel mask.
Unlike glass coated with 10 µm thick electroplated Ni mask which was etched in undiluted 48 % HF, glass coated with 1 µm thick electroplated Ni mask was etched in a combination of 50:5:1 by volume of HF:HCl:HNO₃. The use of this combination resulted in smooth etched surfaces as shown in Fig. 5.30. However, Ni started peeling off after 60 minutes of exposure to the etching solution. This Ni peel-off is attributed to HCl attack limiting the etch depth to 165 µm as shown in Fig. 5.31. The lateral undercutting for the above combination of etch mask and etchant used calculated from Fig. 5.32 was 223.5 µm. The aspect ratio for vertical to lateral etching achieved for this case was 0.74.

Fig. 5.30: Smooth edges achieved using a combination of 50:5:1 by volume HF:HCl:HNO₃ etchant. (a) Microphotograph of edge of cross trench area for scribing (magnification approximately x 25). (b) Microphotograph of edge of alignment trench etched in glass for alignment purpose during anodic bonding (magnification approximately x 100)

Fig. 5.31: Etch depth of 165 µm achieved using 1 µm electroplated Ni mask in a HF/HCl/HNO₃ etchant combination.
5.4.6 Cr/Mo with AZ® P4620 Photoresist Mask

This mask comprises of 200 nm Cr layer on glass followed by 600 nm of Mo layer and 20 µm of AZ® P4620 photoresist layer. Smooth edges were achieved using this mask in 50:5:1 by volume HF:HCl:HNO₃ etchant solution. This is illustrated in Fig. 5.33. A small number of tiny pinholes in glass in the protected area were observed as shown in Fig. 5.34. The etch depth was limited to 75 µm. The depth was measured using a Tencor 500 surface profiler and the measured depth is illustrated in Fig. 5.35. The depth limitation may be attributed to the attack of Mo metal layer by HCl and HNO₃.

5.4.7 Anodically Bonded Silicon Mask

Etch depths greater than 600 µm have been achieved in glass using an anodically bonded silicon mask in this work. This method is expensive and time consuming. The silicon substrate was patterned and etched in 20 % KOH concentration at 45 °C. The oxide mask to protect silicon substrate was 1 µm thick. Hence, the concentration of KOH and bath temperature were key to enable etching through the full thickness of 500 µm of the silicon wafer. This was achieved at 20 % KOH concentration.
and 45 °C bath temperature with few hundreds of nanometer thick oxide still seen on the silicon surface as illustrated in Fig. 5.36.

Fig. 5.33: Smooth edges achieved using Cr/Mo mask using 50:5:1 by volume HF:HCl:HNO₃ etchant solution (magnification approximately x 25).

Fig. 5.34: Tiny pinholes observed in protected areas (magnification approximately x 25).

Fig. 5.35: A maximum depth of 75 µm achieved using the Cr/Mo mask in HF/HCl/HNO₃ combination etchant.
The patterned silicon wafer was anodically bonded to glass and this bonded package is shown in Fig. 5.37. The glass wafer is now etched in 48 % HF. The back side of the glass wafer during HF etching was protected by a 4” silicon substrate. The latter silicon substrate was held to the glass using a paint mask from Harman Corporation. The paint mask must cover the periphery of the wafer and enclose the top edge to protect against HF attack from the sides of the wafer. The greatest advantage of this method is that etch depths greater than 1 mm in glass can be achieved without significant difficulty.

After etching, the anodically bonded silicon mask needs to be separated from the glass wafer. Corman et al. [27] have reported separating the anodically bonded package of glass and silicon by etching in KOH. This observation of separating the bonded wafers by etching in silicon has been proved wrong in this research as anodic bonding is an irreversible process and the only way to debond the package is to completely etch the silicon mask. The major disadvantage of this method is the extremely long duration needed to etch silicon mask. For this case, 31.25 hours were needed to etch
through the 500 µm thick silicon wafer in 20 % KOH solution at 45 ºC and another 48 hours needed to etch away the silicon mask after anodic bonding and etching of the glass in HF. This method is time consuming and tedious as only one glass sample can be etched with one silicon mask. It is a destructive and an expensive method. The etch rate of pyrex glass in 48 % HF was 7 µm per minute. When the etched glass sample was viewed under the optical microscope, smooth edges were observed in the etched windows and the non-etched areas were totally protected against attack by undiluted 48 % HF as illustrated in Fig. 5.38. This method is similar to the procedure used by Corman et al. [27]. They had observed inclined side walls in glass due to the anisotropic KOH etching of silicon mask. The dimensions of the patterned silicon wafer have not been mentioned by them. In this research, anodically bonded silicon was used as mask to etch cavities, 5 x 5 mm, in glass using 48 % HF. Straight walls were observed when compared to inclined walls observed by Corman et al. [27]. This straight wall observation may be attributed to the larger dimensions used in this research. Also depths greater than 600 µm was achieved in less than 2 hours when compared to 475 µm etch depth obtained by Corman et al. [27] having an etch rate of 12 µm/hr using 5:1 HF:H₂O etchant.

Fig. 5.37: Anodically bonded glass substrate to silicon used as an etch mask. Wafer diameter is 4”. 

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5.4.8 Various Etchants Used to Etch Glass

Various etchants such as undiluted 48 % HF, combination of 50:5:1 by volume of HF:HCl:HNO₃, 6:1 by volume DI H₂O: BOE and 10:1 by volume DI H₂O:HF were used for etching pyrex glass in this research. Deep isotropic etching was possible only through the use of undiluted 48 % HF. Smooth edges were obtained only through the use of either 48 % HF or the combination of 50:5:1 by volume of HF:HCl:HNO₃. Concentrated 48 % HF resulted in rough etched surfaces; however this problem was alleviated through the use of a combination of concentrated HF:HNO₃:HCl in the ratio of 50:5:1. All etchings were performed at room temperature. All of the above observations have been illustrated in Fig. 5.39. Table 5.3 summarizes etch rates of all the metals used in this research as etch masks for preferential glass etching. The etch rate is given in nm/min.

5.5 Anodic Bonding and Dicing

The patterned silicon wafers were subjected to RCA cleaning prior to bonding. The pyrex glass wafer was subjected to a second treatment of boiling in nitric acid and rinsing in running DI water for 10 minutes to ensure that there were as few
particles as possible on the glass wafer. After blowing dry in nitrogen, the wafers were dehydrated by heating at 110 °C for 30 minutes and anodically bonded at 380 °C and 1000 V as described in section 2.1. Typical chamber pressure for anodic bonding is 1 Torr. Typical variation in current during anodic bonding is illustrated in Fig. 5.40. The current at the very beginning is high (8 mA) and starts to decay after a few seconds. The initial current peak is attributed to transport of sodium ions from glass to cathode and the current drops as more and more ions move towards the cathode. The total time to complete the bonding from start to finish was 20 minutes. The bonding process alone took 10 minutes and 15 seconds as seen in Fig. 5.40.

Clamping force plays a vital role during anodic bonding. It was noticed that in the absence of optimum clamping force, usually 100 N for a 4” diameter wafer, electrical noise resulted and the system tripped resulting in poor bonds. This phenomenon of electrical noise observed in poorly clamped wafers is illustrated in Fig. 5.41. It is clear from Fig. 5.41 that target of 8 mA was instantly reached but however due to the reduced clamping force of 23 N, electrical noise was noticed which ultimately resulted in the wafer bonder to trip and yielded inferior bond. Under low force there are small cavities formed between the platen and the glass surface. These cavities become filled with gas due to the glass outgassing as the wafers are heated. When the high voltage is applied, electrical discharge is obtained in these cavities. As the force is increased and the glass is pressed more intimately against the platen, these cavities are reduced and the electrical current becomes more stable. The digital images, cross section and top view of the package are shown in Figs. 5.42, 5.43 and 5.44 respectively. Microphotographs of the anodically bonded package, the exposed metal line for communication with the outside
world, non-bonded areas due to the presence of dust particles and 50 µm deep cavities etched at the bottom side of the glass wafer to protect circuitry from high voltages during anodic bonding are illustrated in Fig. 5.45. Number of unbonded areas was observed in the bonded wafers as illustrated in Fig. 5.42. This problem can be mitigated in the near future by thorough cleaning of wafers prior to bonding.

Table 5.3: Approximate values of etch rates observed in this work using different etchants in nm/min at room temperature unless noted otherwise.

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Etch Rate (nm/min.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pyrex 7740</td>
</tr>
<tr>
<td>HF (48 %)</td>
<td>7000</td>
</tr>
<tr>
<td>10:1 HF</td>
<td>204</td>
</tr>
<tr>
<td>6:1 BOE</td>
<td>52</td>
</tr>
<tr>
<td>Aqua Regia</td>
<td>0</td>
</tr>
<tr>
<td>Transene Cr 1020 A</td>
<td>0</td>
</tr>
<tr>
<td>Transene Au TFA</td>
<td>0</td>
</tr>
</tbody>
</table>

+ → Ni peeling off was noticed in concentrated 48 % HF.
N/A → Data not available
* → Etch rate at 40 ºC
S → Etching did occur but etch rate could not be measured as it was very small.
Fig. 5.39: Observed effect of various etchants on pyrex glass. (a) Microphotograph of smooth edges obtained using a combination of 50:5:1 by volume of HF:HCl:HNO₃. (b) Microphotograph of smooth edges obtained using undiluted 48 % HF. (c) Microphotograph of ill-defined edges obtained using 6:1 by volume DI H₂O:BOE. (d) Microphotograph of ill-defined edges obtained using 10:1 by volume DI H₂O:HF. (e) Very high surface roughness observed using fresh undiluted 48 % HF. Magnification approximately x 25 for (a)-(e).
Fig. 5.40: Illustration of current and voltage variation with time during the anodic bonding process.

Fig. 5.41: Electrical noise observed due to low clamping force used during anodic bonding.
Fig. 5.42: Digital images of the anodically bonded package. (a) Top view of the anodically bonded package. (b) Exposed metal line seen on the Si surface.
5.43: Cross section of the anodically bonded package.
Etch depths of 400 µm were achieved in the patterned areas of the glass except at the corners to facilitate scribing of the packaged chip. Etch depth of 200 µm was achieved at both the front and back side of the corner areas of the glass. Front and back side etching at the corner areas of glass was done to facilitate scribing to expose metal lines on silicon. 50 µm deep recess was etched at the bottom side of the glass to protect circuitry from high voltages during anodic bonding. Etch depths of 237 µm was accomplished at the top side of the silicon to facilitate scribing of the packaged chip. Anodic bonding can be done in inert or partial vacuum environment to enable desirable operation of moving mechanical MEMS structures on the chip package. The bonded areas were tested by dipping in IPA. No incursion of IPA was seen to penetrate the bonded areas. Thus, it can be concluded that good bonds have been achieved using the AML 402 wafer bonder.
Fig. 5.45: Microphotographs of the anodically bonded package at magnification approximately x 25 for (b)-(e). (a) Portion of non-bonded areas seen in the package. Magnification x 100. (b) Exposed metal line running across the Si substrate after dicing the corner areas of glass (area H looking from top in Fig. 5.44). (c) Metal line on Si seen through anodically bonded glass wafer along the trench edge D in Fig. 5.43. The 50 µm recess protects circuitry from high voltages during anodic bonding. (d) View from top through the glass looking at a corner of the 50 µm recess (area F in Fig. 5.44) (e) Interface between the bonded and unbonded areas (looking from top across area G in Fig. 5.44).
5.6 Chapter Summary

The objective of developing a fabrication process for WLCSP using a wafer bonder and for electrical communication with the outside world from within the packaged chip has been successfully achieved in this research. The sub-tasks of developing a novel masking technology to etch glass wafers deeply and for developing an anodic bonding process that incorporates electrical feedthroughs at wafer level have been accomplished in this research.

Trenches for subsequent scribing were etched in both glass and silicon substrates to facilitate dicing after anodic bonding was accomplished. A number of metals were investigated as etch masks for etching of pyrex glass in undiluted 48 % HF. Three novel masks for deep etching in glass were developed in this research. They are: 1) anodically bonded silicon mask, 2) Mo/Cr/Au layers with 20 µm thick AZ® P4620 photoresist and 3) Cr/electroplated Ni layers with 20 µm thick AZ® P4620 photoresist. Various other etchants such as 10:1 by volume DI H₂O:HF, 6:1 by volume DI H₂O:BOE and 50:5:1 by volume HF:HCl:HNO₃ combination were investigated to etch glass along with undiluted 48 % HF. Deep etching of glass with sharp edges was only possible with 48 % HF. Dilute and buffered HF resulted in poorly defined edges and also deep etching of glass could not be achieved by their use. Glass etch rates for 10:1 by volume DI H₂O:HF and 6:1 by volume DI H₂O: BOE were low with values of 204 nm/min and 52 nm/min respectively. Glass etch rate of 7000 nm/min in glass was achieved using 48 % HF.

Silicon was etched in 45 % KOH by weight in DI water at 50 °C, the etch mask being 1 µm thick thermally grown oxide. Etch depth of 355 µm was achieved using
the above parameters. The etch rate of silicon was observed to be 11.3 µm/hr in 45 % KOH solution at 50 ºC etch temperature. Smooth etched surfaces, sharp edges and deep trenches were obtained when silicon was etched in 45 % KOH solution at 50 ºC. The etched glass and silicon substrates were decontaminated using conventional hydrogen peroxide based cleaning techniques, dehydrated at 110 ºC for 30 minutes in a conventional oven, aligned in-situ and bonded using an AML 402 wafer bonder. The corner areas of the glass wafer were diced to expose the metal lines on the silicon substrate emanating from within the package. Thus, the concept of WLCSP using anodic bonding has been demonstrated in this research.
6. SUMMARY AND FUTURE WORK

6.1 Summary

The purpose of this research was to develop an in-house processing capability for silicon/glass bonding for microfabrication and wafer level chip scale packaging (WLCSP) using a wafer bonder and to prove the feasibility of electrical communication with the outside world from microsystem enclosed within the anodically bonded package.

Etching trenches in glass and silicon were necessary to facilitate subsequent scribing. Without these trenches, it would be difficult to dice the 1.2 mm thick package. Silicon was etched with KOH etchant at varying weight concentration of 20 %, 30 %, 45 % and 50 % in deionized water at 50 °C, 60 °C, 70 °C and 80 °C. KOH concentration of 45 % and 50 °C etch temperature were chosen as suitable silicon etch parameters as they resulted in deep trenches, smooth mirror like surfaces and sharp side edges in etched pits and channels. Silicon etch depth of 355 µm were achieved at 45 % KOH concentration and 50 °C etch temperature using 1 µm oxide mask. Silicon etch rate observed in 45 % KOH concentration at 50 °C etch temperature was 11 µm/hour.

A novel masking technology for deep etching of glass using a combination of conventional metal layers and standard photosist layer was also investigated. A total of 8 combinations of different metal masks were investigated for deep etching in glass. They were: 1) Cr (200 nm) with 20 µm AZ® P4620 photosist, 2) Ti/Mo layers (100 nm/600 nm) with 1 µm Microposit® S1813 photosist, 3) Cr/Au/Cr/Au layers (200 nm/500 nm/200 nm/50 nm) with 20 µm AZ® P4620 photosist and SU 8 polymer, 4) Mo/Cr/Au layers (600 nm/200 nm/50 nm) with 20 µm AZ® P4620 photosist, 5) Cr/electroplated Ni layers (200 nm/1 µm) with 20 µm AZ® P4620 photosist, 6) Cr/Au/electroplated Ni
layers (200 nm/ 50 nm/10 µm) with 20 µm AZ® P4620 photoresist, 7) Cr/Mo layers (200 nm/600 nm) with 20 µm AZ® P4620 photoresist and 8) anodically bonded silicon mask. The 20 µm thick AZ® P4620 photoresist was used not only for patterning the metal mask but also for providing protection against HF attack. The experimental results indicate that with anodically bonded silicon mask, etch depths greater than 1 mm in glass could be achieved without significant difficulty. However, this method proved to be very expensive and time consuming as the silicon mask had to be patterned and etched which took about 71.21 hours for patterning and another 48 hours for complete removal through etching. The latter is needed in order to separate the etched pyrex glass wafer from the bonded silicon mask. This is the only method currently available to achieve etch depths greater than 1 mm in glass. It takes less than 2 hours of etch time in undiluted 48 % HF at room temperature for etching 600 µm pyrex glass thickness.

The earlier barrier of etching 300 µm depth in pyrex glass [33] using metal mask has been broken in this research using a novel multilayered mask comprising of 200 nm Cr, 50 nm Au and 10 µm thick electroplated Ni in conjunction with 20 µm thick layer of AZ® P4620 photoresist. Depths greater than 400 µm has been achieved without any pinhole formation on the areas masked by the metal.

The surface roughness problem caused by etching in concentrated HF has been eliminated by etching glass in a combination of 50:5:1 by volume of concentrated HF: HNO₃:HCl. However maximum etch depths of only 165 µm can be achieved with the above etchant with Cr/electroplated Ni layers (200 nm/1 µm) in conjunction with 20 µm AZ® P4620 photoresist mask.
Another novel mask developed in this research for deep etching of glass comprised of a multilayer metal combination of Mo/Cr/Au (600 nm/200 nm/50 nm) in conjunction with a 20 µm thick layer of AZ® P4620 photoresist. Aspect ratio of vertical to lateral etching rate of 0.88 was achieved using this novel mask which was superior than that achieved by using a Cr/Au/Cr/Au mask [33] and an anodically bonded silicon mask [27]. The aspect ratios for the latter two cases were found to be 0.78 and 0.66 respectively. Pinholes were successfully eliminated using Mo/Cr/Au layers with AZ® P4620 photoresist novel mask. Etch depths of 216 µm were achieved using the above Mo/Cr/Au mask in undiluted 48 % HF.

Shipley 1813 photoresist and Ti adhesion layer should never be used as it resulted in the rapid attack of the protected glass layer due to failure of the Ti metal mask from the exposed periphery of the windows opened in the photoresist. There was lift-off of Shipley 1813 photoresist after 10 minutes of exposure in undiluted 48 % HF.

Smooth edges and etch depths upto 70 µm could be achieved in glass using a Cr mask and a combination of Cr/Mo mask using undiluted 48 % HF and a combination of 50:5:1 by volume HF:HCl:HNO₃ respectively. However, for etch depths beyond 70 µm, it is not advisable to use these metal masks as they resulted in pinhole formation in the protected areas and hence damage to the glass surface that was protected by the mask.

Mo/Cr/Au layers with AZ® P4620 photoresist, anodically bonded silicon mask and novel multilayered mask comprising of 200 nm Cr, 10 µm thick electroplated Ni in conjunction with 20 µm thick layer of AZ® P4620 photoresist should prove very valuable in the field of MEMS for deep etching of pyrex glass and for fabrication of optical devices and MEMS structures utilizing glass wafers. Thus, the earlier barrier of
300 µm etch depth in glass using metal mask [33] has effectively been broken and a new limit of 600 µm using anodically bonded silicon mask and 430 µm using electroplated Ni has been successfully achieved in this research.

The patterned silicon and glass wafers were decontaminated using hydrogen peroxide based cleaning techniques, placed in a wafer bonder, aligned in-situ and bonded at 380 ºC and 1 kV at 1 Torr using an AML 402 wafer bonder. The problem of high electric field on the circuitry during anodic bonding could possibly be mitigated by etching borofloat glass wafer with 50 µm deep cavities [34] over the CMOS chip locations. The patterned glass wafer was diced at the corners to expose the aluminum metal lines on the silicon. In this way, communication to the outside world from within the package was established. Thus, not only an effective wafer level chip scale packaging technology has been demonstrated in this thesis research but a novel masking technology for deep etching in glass has also been developed.

6.2 Future Work

Future work includes forming etched pits in silicon to accommodate a combination of silicon MEMS dies and CMOS circuitry and utilize the technology of ultrasonic wire bonding to facilitate connection between the enclosed dies and to the metal lines running along the silicon substrate surface for communication to the outside world. This is followed by anodic bonding and dicing of the package.

Tungsten is known to have zero etch rates in concentrated HF. This could be a viable etch mask for deep etching in glass. It has been observed that silicon is highly resistant to HF and it is the key to achieving deep trenches and channels in glass. SiC and
polycrystalline silicon may be sputtered on the glass, patterned by RIE and the exposed glass can be wet etched in undiluted 48 % HF.

The feasibility of silicon fusion bonding for packaging could also be explored in the near future with annealing at lower temperature and longer times.
BIBLIOGRAPHY


Dear Ms. Daniele,

I would appreciate if you could kindly grant me permission to use figures 5.2 a. Hydroxyl groups on an oxidized silicon wafer. b. Siloxane bond after bonding pg 161. and 5.4 Schematic diagram showing the mechanism of Si//Si bonding, pg 165, from the book "Sensor technology and devices" by Ljubisa Ristic.

I am planning to use these figures in my thesis report "Wafer level chip scale packaging using wafer bonder". I greatly appreciate your reply.

Thanks

Regards

Kailash

From: “Christine Daniele” <cdaniele@artechhouse.com>
To: “Kailash Upadhyaya” <kupadh1@lsu.edu>
CC: 
Subject: Re: Permission to use figures
Date: Tue, 3 May 2005 10:44:20 -0400

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Regards,

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Editorial Assistant, Acquisitions

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Kailash Upadhyaya was born in 1976 in Madras (now Chennai) in Tamil Nadu, a southern state of India. He completed his Bachelor of Engineering in Electrical and Electronics Engineering at the University of Madras, India, in August 2001. He is currently a candidate for the Degree of Master of Science in the department of Electrical and Computer Engineering at Louisiana State University.