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# First order sigma-delta modulator of an oversampling ADC design in CMOS using floating gate MOSFETS

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# FIRST ORDER SIGMA-DELTA MODULATOR OF AN OVERSAMPLING ADC DESIGN IN CMOS USING FLOATING GATE MOSFETS

A Thesis

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering

in

The Department of Electrical and Computer Engineering

by
Syam Prasad SBS Kommana
Bachelor of Technology, Nagarjuna University, 2001
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# Abstract

We report a new architecture for a sigma-delta oversampling analog-to-digital converter (ADC) in which the first order modulator is realized using the floating gate MOSFETs at the input stage of an integrator and the comparator. The first order modulator is designed using an 8 MHz sampling clock frequency and implemented in a standard 1.5μm n-well CMOS process. The decimator is an off-chip sinc-filter and is programmed using the VERILOG and tested with Altera Flex EPF10K70RC240 FPGA board. The ADC gives an 8-bit resolution with a 65 kHz bandwidth.

# Chapter 1
# Introduction

## 1.1 Introduction

Advancement in VLSI technology, has allowed a phenomenal growth of the silicon integrated circuits. As there is a remarkable progress in the fabrication, the MOS transistors have been scaled down [1]. According to Moore's prediction in 1965, the total number of devices on a chip double every 12 months [2]. Though it is getting increased, a number of severe limitations like increased interconnections, hot carrier phenomena and increase in electric field due to scaled down dimensions have lead to degradation of device performance and life time. To increase the functionality of a MOS transistor, a structure was proposed by Shibata and Ohmi [3] defining it as a floating-gate MOSFET, which allowed for the enhancement in the basic function of a transistor. In a floating-gate transistor, the charge on the gate of a MOSFET is controlled by two or more inputs through poly-poly capacitors between each input and the floating-gate as shown in the Figure 1.1. $C_1$ and $C_2$ are the input capacitors for the floating gate MOSFET. By using one input for the signal and one for a bias voltage, the floating-gate potential can be partly set by the bias voltage, $V_{bias}$.

The floating gate MOSFETs have been used in digital circuits primarily as storage devices. Even though the flash memories and other NVMs have been using the 1T floating gate (FG) transistor, recently multi-input floating gate (MIFG) MOSFETs have been used as circuit elements [4]. The concept of multi-input floating gate was first derived from the biological neurons and hence the floating gate MOSFET was initially

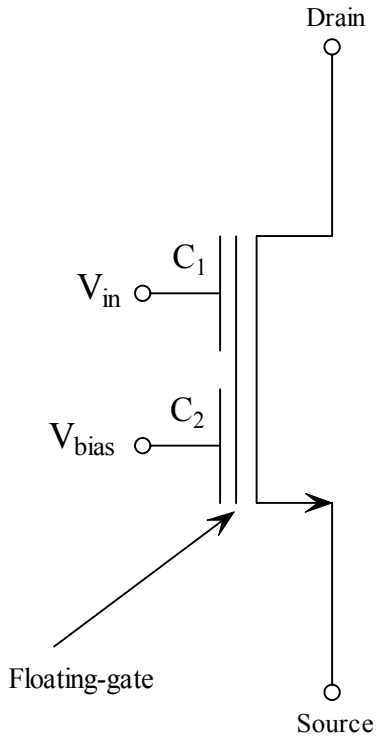



Figure 1.1: Floating-gate MOSFET.

called a neuron MOSFET or υMOSFET [3]. The MIFG-MOSFET operation depends on the weighted sum of voltages at input nodes, which are capacitively coupled to the floating gate. This leads to a negligible amount of charging and discharging currents and results in low-power dissipation [3]. The floating gate MOSFETs have been used in design of data converters [5-7], low voltage op-amp with rail-to-rail input [8] and the four quadrant multiplier [9] circuits in low-voltage analog signal processing. By making a particular choice of capacitive couplings into floating gate devices, a wide range of trans-linear functions can be computed. However, there is no reported work on use of floating gate MOSFETs in sigma-delta ADC for low power analog signal processing.

Depending on the ratio of sampling, the analog to digital converters can be divided into two categories. The first category is the Nyquist rate ADCs in which the input data is sampled at the Nyquist rate. Nyquist sampling states that the frequency of sampling must be at least twice the bandwidth of the signal in order for the signal to be recovered. The second type called an oversampling ADCs, samples the signal at a rate much higher than the Nyquist rate.

Usually successive approximation or dual slope converters are used when high resolution is desired. But to achieve higher accuracy, trimming is required. Dual-slope converters require high-speed and high accuracy integrators that are only available using a high-$f_T$ bipolar process. The main constraint using these architectures is to design a high precision sample and hold circuits. Because digital signal processing techniques are used in place of complex and precise analog components, the second category under ADCs *viz*., the over sampling converters, gives scope to achieve much higher resolution than the Nyquist rate converters. The accuracy of these converter types does not depend on the

component matching, precise sample and hold circuitry or trimming but require only a small amount of analog circuitry.

The typical block diagrams for Nyquist rate converters and oversampling ADCs are shown in Figs. 1.2 (a) and (b) [10]. However, because of the amount of time required to sample the input signal, the throughput time is considerably less than the Nyquist rate ADCs. Throughput time is the total time it takes for an A/D converter to complete consecutive measurements and generate the output code. Oversampling converters typically employ switched-capacitor circuits and therefore do not need sample and hold circuits. Sigma delta modulators shown in the Fig. 1.3 [11], come under the over sampling converters. The output of a modulator is a pulse density modulated signal that represents the average of the input signal. As seen from Fig. 1.3 [11], the function of comparator is that the1-bit data tells the output voltage in which direction to go based upon what the input signal is doing.

The comparator compares the input signal against its last sample, to see if this new sample is larger than the last one. If it is larger, then the output is increasing and if it is smaller, then the output is decreasing. As the Greek letter-Δ (delta) is used to show the deviation or small incremental change, the process came to be known as "delta modulation". Delta modulation is based on quantizing the change in the signal from sample to sample rather than the absolute value of the signal at each sample. Sigma stands for summing or integrating, which is performed at the input stage on the digital output with the input signal before the delta modulation as shown in Fig 1.4 [12]. Hence the analog to digital conversion of this technique is called sigma-delta modulation. The $1^{st}$ order sigma-delta modulator design of Fig. 1.4 consists of mainly an integrator,

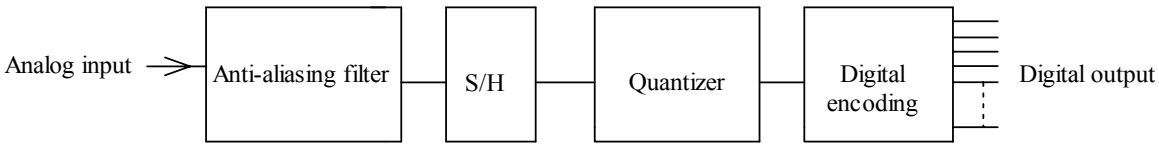



Figure 1.2: (a) Block diagram of Nyquist rate converters [10].

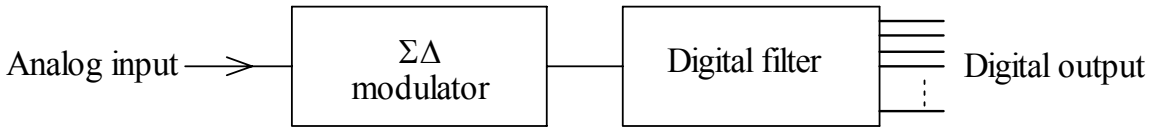



Figure 1.2: (b) Block diagram of oversampling ADCs [10].

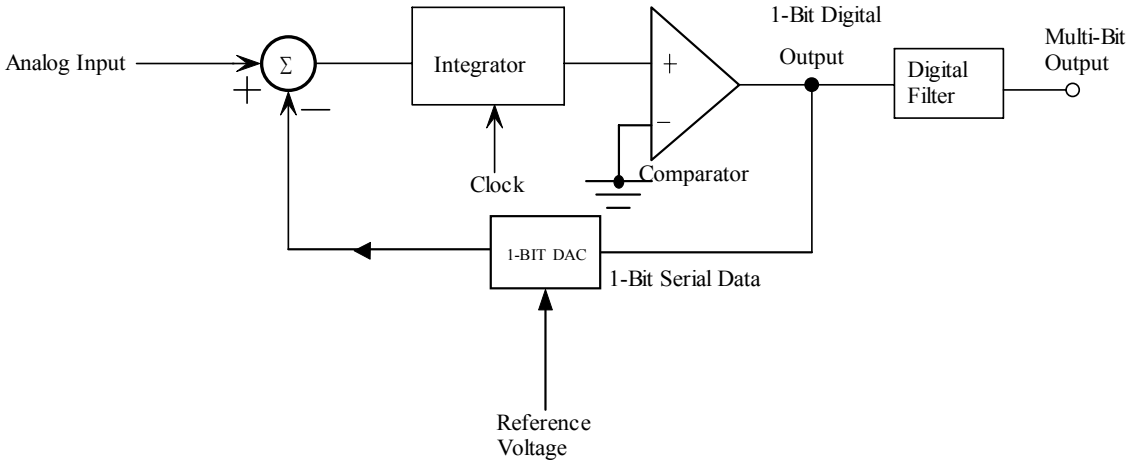



Figure 1.3: Block diagram of a sigma-delta ADC [11].

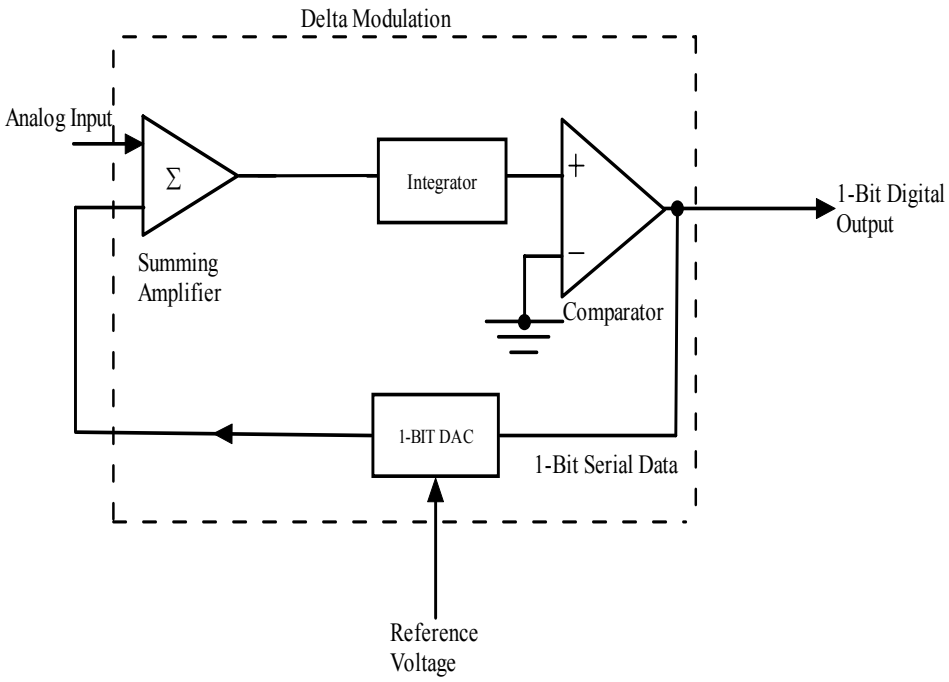



Figure 1.4: Block diagram of a 1st order modulator [12].

comparator and D/A converter. The single-bit feedback D/A converter (DAC) output is subtracted from the analog input signal, in the summing amplifier.

The resultant error signal from the summing amplifier output is low-pass filtered by the integrator and the integrated error signal polarity is detected by the single comparator. This comparator is effectively a 1-bit A/D converter (ADC). This architecture achieves a wide range of resolution and a higher bandwidth. Settling time is an important parameter which determines the resolution of an ADC. It is defined as a small amount of time required for an ADC to reach certain accuracy and stay within the specified range of accuracy. If the settling time is linearly dependent on the input signal, a high-resolution performance can be achieved even if the integrator does not settle to the full resolution of the converter. Due to the saturation of the input stage and slew rate limitation of the output stage, the settling error in the converter can be nonlinear which can be a dominant factor in limiting its performance. One way to avoid saturation limitations in the input stage is to use a large overdrive voltage for the input transistors of the differential pair in the operational amplifier, which cannot be afforded for low voltage design. Another way out, to reduce saturation limitations, is attenuating the input voltage. This can be physically implemented by using floating gate transistors at the input stage of the op-amp. The use of floating gate transistors provides a mean to alter the input DC bias voltage for proper biasing of the input stage and optimization of the dynamic range [5].

In the present work, an 8-bit sigma-delta ADC is designed in standard 1.5 μm n-well CMOS technology, in which the first order modulator is realized using the floating gate MOSFETs at the input stage of an integrator and a comparator operating at a

sampling clock frequency of 8 MHz. The power supplies are $\pm$ 2.5V. Decimation is an important component of oversampled analog-to-digital conversion. It transforms the digitally modulated signal from short words occurring at high sampling rate to longer words at the Nyquist rate [13]. The decimator in the present work is an off-chip sinc-filter and is programmed using the VERILOG and tested with Altera Flex EPF10K70RC240 FPGA board. The ADC gives an 8-bit resolution with a 65 kHz bandwidth.

## 1.2 Literature Review

Mohieldin *et al.* [5] have designed an incremental A/D converter using floating gate technique. In this architecture, the design relies on using floating gate technique in order to reduce the effect of nonlinear settling time of converter output due to possible saturation of the input stage and to achieve good performance under low-voltage operation. The converter operates at a clock frequency of 500 kHz and consumes less than 1 mW. A regenerative latch has been implemented for the comparator design. Ruotsalainen *et al.* [14] have presented the design of a CMOS op-amp with floating gate input transistors. The main benefit of using floating gate MOSFET in this design is to increase the input common-mode voltage range of the op-amp. The measured gain of the op-amp was 65 dB with a phase margin of 62°. However, the design used 4 pF as input capacitors at the input stage and so the large part of chip is occupied by the capacitors itself. Our present design implemented a 0.5 pF as input capacitors at the input stage and the architecture of A/D is based on sigma-delta modulation in which the converter can operate at higher clock frequency. Nandhasri *et al.* [15] proposes the hysteresis tunable voltage comparator using floating gate MOSFET. The circuit is basically a simple voltage comparator embedded with a positive feedback scheme to create the hysteresis.

Angulo *et al.* [16] have conducted research on low-voltage circuits building blocks using multi-input floating gate transistors. In this design, a continuous-time scheme to operate op-amps with a single supply voltage close to just one transistor's threshold voltage and with rail-to-rail input and output voltage swings are implemented. It is based on the use of multiple-input floating gate transistors combined with a low voltage class-AB op-amp architecture. Furth and Ommani [17] have achieved voltage amplification using an operational amplifier with capactive feedback through multiple-input floating gate transistors for micro-power applications. The designed amplifier uses a self-biased cascode transistors operating in the subthreshold region for near rail-to-rail output voltage range.

Table 1.1 summarizes op-amp design using floating gate transistors. Yin *et al.* [7] designed a single floating gate MOS device as a D/A converter. A parallel 8-bit D/A architecture using floating gate MOS transistors was presented in this work. Chen *et al.* [9] proposed a low-voltage four-quadrant multiplier using floating gate MOSFETs. The circuit is implemented in a 0.8 μm double-poly double metal CMOS process.

Keskin *et al.* [18] designed a 13-bit CMOS sigma-delta modulator using unity gain reset op amps. Due to the feedback structure, the op-amps do not need to switched off during the reset phase of the operation and hence can be clocked at high rate. A signal-to-noise distortion ratio of 78 dB for 20-kHz signal bandwidth, and a dynamic range of 74 dB are achieved with a 1-V supply voltage. However the switched capacitors (SC) band-pass modulators at 1-V operation can only achieve an experimentally reported operation speed up to 3 MHz, which is far lower than the attainable performance of SC circuits at higher supply voltages. In addition, the designs of high-frequency SC

modulators require high-gain and high-bandwidth op-amp, which dissipate a lot of power.

Bacrania [19] designed a 12-bit successive approximation register (SAR) type ADC with digital error correction. In this design, the correction algorithm gives almost a two fold improvement in conversion speed without loss of accuracy or changes to the analog circuitry of a slower design. In Table 1.2, a comparison of characheristics of different ADC architectures are presented.

## 1.3 Chapter Organization

The subsequent chapters give details and the design of a 1st order sigma-delta modulator using floating gate MOSFETs in 1.5μm n-well CMOS technology. The structure and operation of floating gate MOSFETs and the inverter is explained in Chapter 2. Chapter 3 covers analysis and design of sigma-delta ADC using floating gate MOSFETs. Chapter 4 presents the design methodology, technology, post-layout simulations and experimental results. Chapter 5 concludes the work. Appendix A summarizes the SPICE MOS modeling parameters used in simulations. Appendix B gives how to simulate a floating-gate MOS transistor. Appendix C shows the implementation of decimator which is an off-chip. Appendix D summarizes the testability of fabricated chip.

Table 1.1: Comparison of op-amps using floating gate MOSFETs

| | Mohieldin et al. [5] | Ruotsalainen et al. [14] | Angulo Et al. [16] | Furth and Ommani [17] |
|---|---|---|---|---|
| Power Supply | ± 1V | ± 1.2V | +1.2V | ± 1.25V |
| DC Gain | 91 dB | 65 dB | 60 dB | 77 dB |
| Phase Margin | - | 71° | 70° | 59° |
| GBW | 3 MHz | 230 kHz | 5 MHz (3 dB BW) | 72 kHz |
| Technology | 0.5 µm CMOS | 0.35 µm CMOS | 0.8 µm CMOS | 1.2 µm CMOS |
| Slew Rate | 10 V/µS | 184 mV/µS | 7 V/µS | 0.024 V/µS |

Table 1.2: Comparison of characteristics of different ADC architectures

| | Mohieldin *et al.* [5] | Nandhasri *et al.* [15] | Bacrania [19] | Pelgrom *et al.* [20] | Choi *et al.* [21] |
|---|---|---|---|---|---|
| ADC Type | Incremental | Sigma-delta | SAR | Flash | Flash |
| Resoultion | 11-bit | 13-bit | 12-bit | 8-bit | 6-bit |
| Clock Rate | 500 kHz | 10 MHz | 4 MHz | 4.43 MHz | - |
| Active Area | 0.2 $mm^2$ | 0.41 $mm^2$ | - | 2.8 $mm^2$ | - |
| Technology and Power Supplies | 0.5 µm CMOS and $\pm$ 1V | 0.35 µm CMOS double poly, triple metal and 1V | 5 µm CMOS self- aligned junction isolated and $\pm$ 15V | 1 µm CMOS and 5 V | 0.8 µm CMOS and 4.5 to 5.5 V |

# Chapter 2
## Multi Input Floating Gate (MIFG) MOSFETS

### 2.1 Introduction

Floating gate is a basic MOSFET except that the gate, which is built on the conventional poly-1, is floating and is then called as a "Floating Gate". The multi-input floating gate MOSFET is a transistor that switches to an ON or OFF state depending on the weighted sum of all input signal applied at its input node which is capacitively coupled to the gate. This leads to only a negligible amount of charging and discharging currents and ultimately leading to low power dissipation. Besides simple implementation of linear weighted voltage addition and analog memory capabilities, the other attractive features offered by MIFG transistor circuits are low voltage rail-to-rail operation, linearity improvement and with rail-to-rail swings [8].

### 2.2 Structure of MIFG MOSFET and Device Physics

The basic structure of the multi input floating gate MOSFET is illustrated in Fig 2.1 [22]. The floating gate in the MOSFET extends over the channel and the field oxide. A number of control gates, which are inputs to the transistor, are formed over the floating gate using a second poly-silicon layer (poly 2). In a floating gate transistor, the charge on the gate of a MOSFET is controlled by two or more inputs through poly-poly capacitors between each input and the floating gate. The capacitive coupling between the multi-input gates and floating gate and the channel is shown in the Fig. 2.2. In the Fig. 2.2, $C_1$, $C_2$, $C_3$… …$C_n$, are the coupling capacitors between the floating gate and the inputs. The corresponding terminal voltages are $V_1$, $V_2$, $V_3$….$V_n$, respectively. $C_0$ is the capacitor between the floating gate and the substrate. $V_{SS}$ is the substrate voltage. The charges are

stored in the corresponding capacitors $C_1$, $C_2$, $C_3$… …$C_n$. At any time, the net charge $Q_F(t)$ on the floating gate is given by the following equations [3, 22].

$$Q_F(t) = Q_0 + \sum_{i=1}^{n}(-Q_i(t)) = \sum_{i=0}^{n} C_i(\Phi_F(t) - V_i(t)) \tag{2.1}$$

or $$Q_F(t) = \Phi_F(t)\sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i(t) \tag{2.2}$$

Where n is the n is the number of inputs, $Q_0$ is the initial charge present on the floating gate, $Q_i$ (t) is the charge present in capacitor $C_i$ and $\Phi_F(t)$ is the potential at the floating gate. The potential of the floating gate $\Phi_F$ is determined as

$$\Phi_F = \frac{C_1V_1 + C_2V_2 + ..... + C_nV_n}{\sum_{i=0}^{n} C_i} \tag{2.3}$$

$$\Phi_F(t) = \frac{\sum_{i=1}^{n} CiVi(t)}{\sum_{i=0}^{n} Ci} \tag{2.4}$$

Here, the substrate potential and the floating gate charge are assumed to be zero for simplicity. The equation (2.4) is obtained as follows:

Setting $V_{ss}$ to 0 and applying the law of conversation of charge at the floating gate, we obtain,

$$\Phi_F(0)\sum_{i=0}^{n} C_i - \sum_{i=1}^{n} C_i V_i(0) = \Phi_F(t)\sum_{i=0}^{n} C_i - \sum_{i=1}^{n} C_i V_i(t) \tag{2.5}$$

or

$$\Phi_F(t)\sum_{i=0}^{n} C_i - \Phi_F(0)\sum_{i=1}^{n} C_i = \sum_{i=0}^{n} C_i V_i(t) - \sum_{i=1}^{n} C_i V_i(0) \tag{2.6}$$

or

$$\Phi_F(t) = \Phi_F(0) + \frac{\sum_{i=1}^{n} C_i V_i(t) - \sum_{i=1}^{n} C_i V_i(0)}{\sum_{i=0}^{n} C_i} \tag{2.7}$$

Assuming zero initial charge on the floating gate in Eq. (2.1), Eq. (2.7) reduces to

$$\Phi_F(t) = \frac{\sum_{i=1}^{n} CiVi(t)}{\sum_{i=0}^{n} Ci} \tag{2.4}$$

When the value of $\Phi_F$ exceeds $V_{TH}$, threshold voltage on the floating gate, the transistor turns-on. Thus, the "ON" and "OFF" states of the transistor are determined whether the weighted sum of all input signal is greater than $V_{TH}$ or not. The behavior is quite analogous to that of biological neurons [3], and hence is called neuron MOSFET or υMOSFET. The value of $\Phi_F$ determined by Eq. (2.4) holds true, as long as all the input capacitive coupling co-efficients remain unchanged during the device operation. The oxide capacitance, $C_0$ is assumed to be constant. The Fig. 2.3 (a-b) shows the symbols of MIFG MOSFET of both p and n-MOSFETs.

## 2.3 Floating Gate CMOS Inverter

A multi-input floating gate CMOS inverter is shown in Fig. 2.4. From the Fig. 2.4, $V_1$, $V_2$, $V_3$, $V_4$,…..,$V_n$ are input voltages and $C_1$, $C_2$, $C_3$, $C_4$,…..,$C_n$ are corresponding input capacitors. To determine the voltage on the floating gate of the inverter, Eq. (2.4) is used. Weighted sum of all inputs is performed at the gate and is converted into a multiple-valued input voltage, $V_{in}$ at the floating gate. The switching of the floating gate CMOS inverter depends on whether $V_{in}$ obtained from the weighted sum, is greater than or less than the inverter threshold voltage or inverter switching voltage ($\Phi_{in}$).

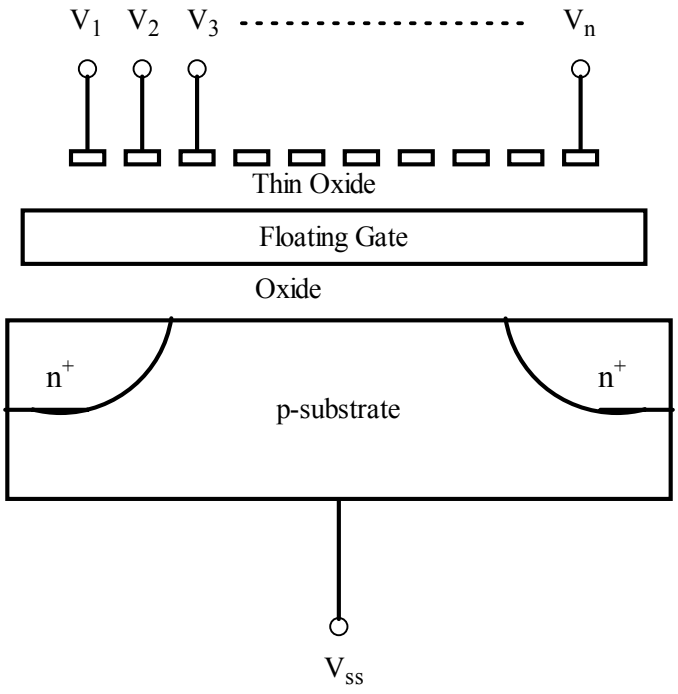



Figure 2.1: Basic structure of a multi-input floating gate MOSFET.

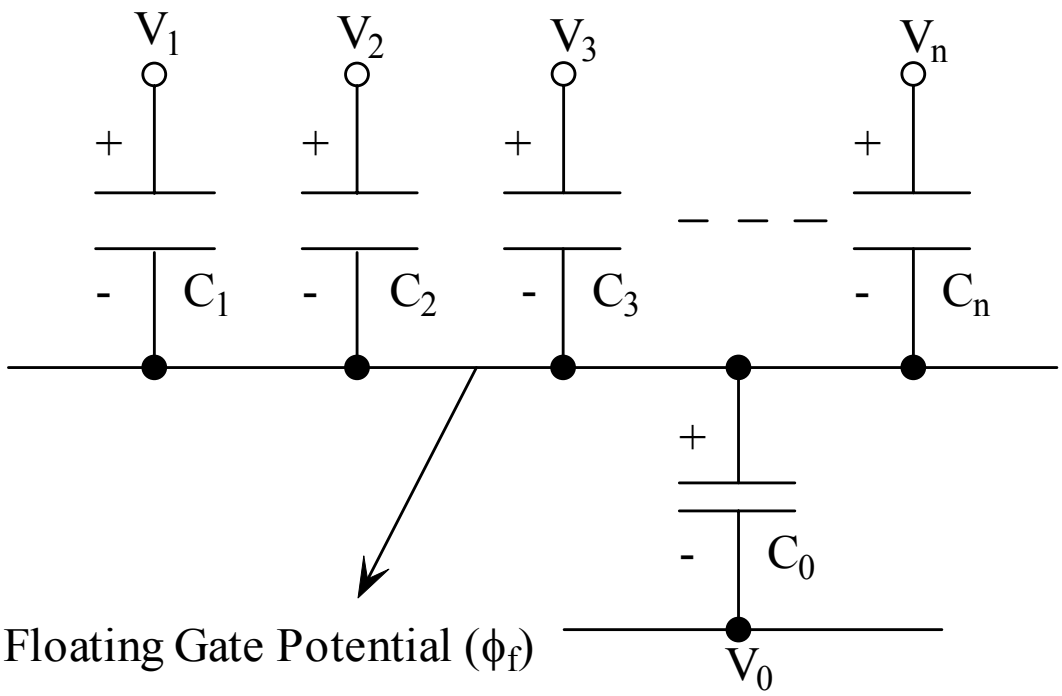



Figure 2.2: Terminal voltages and coupling capacitances of a multi-input floating gate MOSFET.

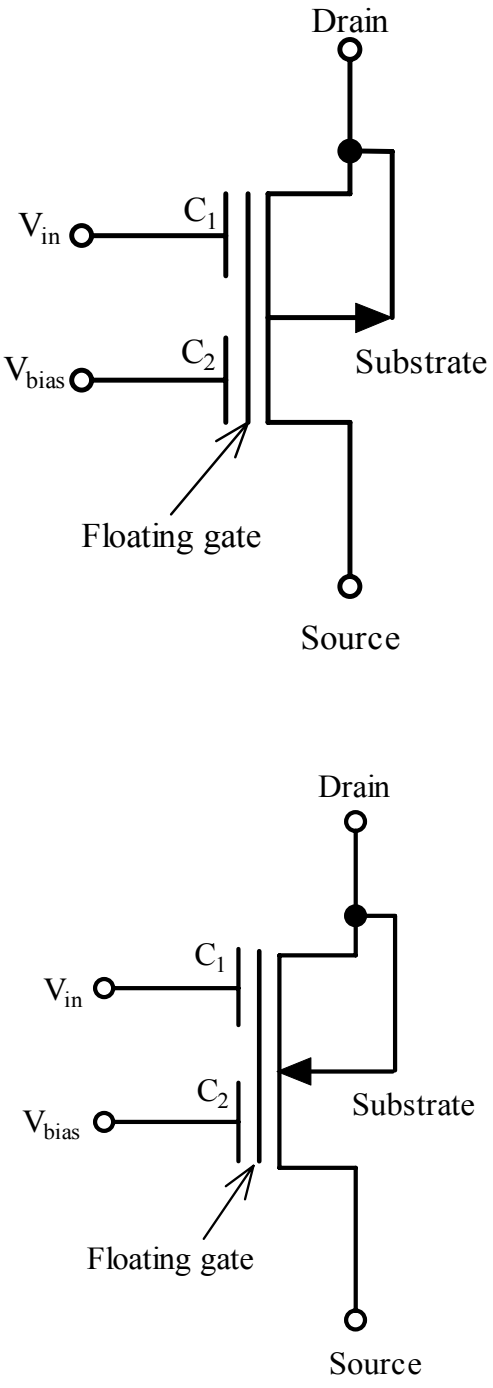



Figure 2.3: (a) MIFG p-MOSFET. (b) MIFG n-MOSFET.

The switching voltage is computed from the voltage transfer characteristics of a standard CMOS inverter and is given by the following equation [23].

$$\Phi_{inv} = (\Phi_{go} + \Phi_{s1})/2 \quad (2.9)$$

Where $\Phi_{go}$ and $\Phi_{s1}$ are the input voltages at which $V_{out}$ is $V_{DD}$-0.1V and 0.1V, respectively. Hence the output ($V_{out}$) of a multi-input floating gate CMOS inverter is

$V_{out}$ = HIGH (3V) if $\Phi_F < \Phi_{inv}$

= LOW (0V) if $\Phi_F > \Phi_{inv}$ (2.10)

The capactive network of an n-input floating gate CMOS inverter is shown in Fig 2.5 [24]. The gate oxide capacitance of a p-MOSFET, $C_{oxp}$ is between the floating gate and n-well connected to $V_{DD}$. $C_p$ is the capacitance formed between poly-silicon floating gate and the substrate connected to $V_{SS}$. The voltage on the floating-gate is given by in an earlier work [24] and analysis is presented. Figure 2.6 shows the circuit diagram and the transfer characteristics of a 4-input floating-gate CMOS inverter as an illustration of Eq. (2.10).

The uniqueness of multi-input floating gate inverter lies in the fact that the switching voltage can be varied. Ordinarily, varying the $W_p/W_n$ ratios of the inverter does the adjustment of threshold voltage. However, in multi-input floating gate inverter, varying the coupling capacitances to the gate can vary the switching point in DC transfer characteristics.

## 2.4 Unit Capacitance

The floating gate CMOS circuit design layout faces certain shortcomings in fabrication process. Due to fabrication process variations in runs employed, designed capacitors may not be of exact right values since capacitors are expressed in integral

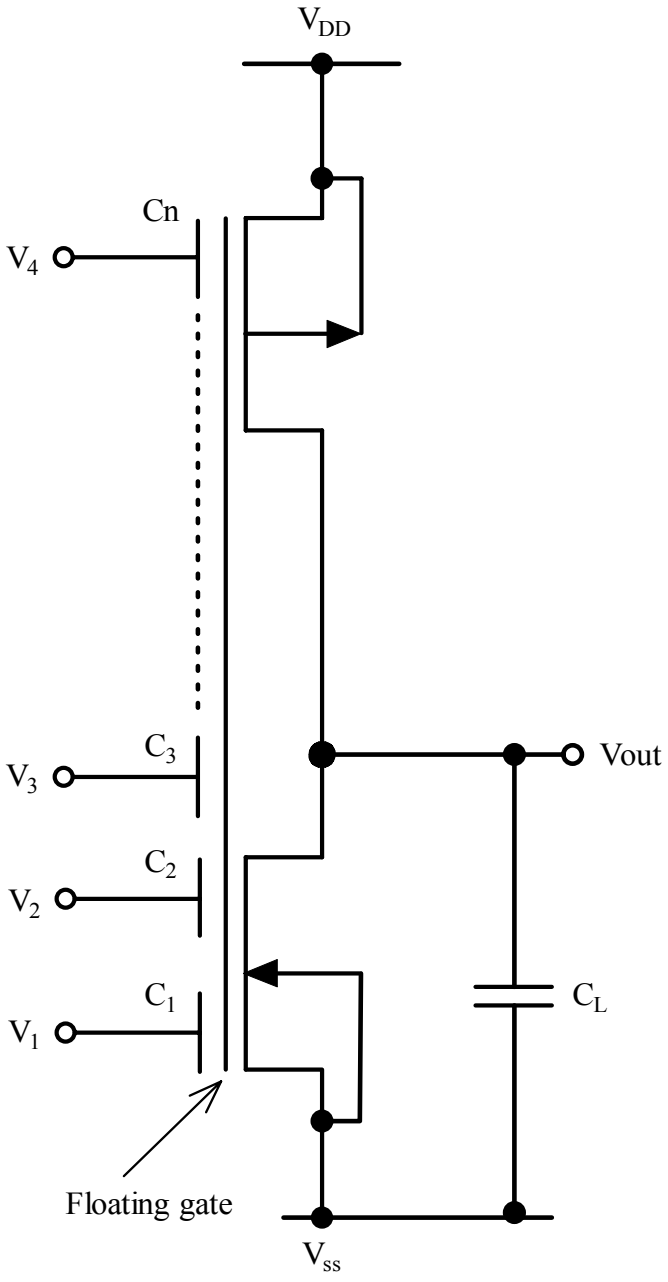



Figure 2.4: Multi-input floating gate (MIFG) CMOS inverter.

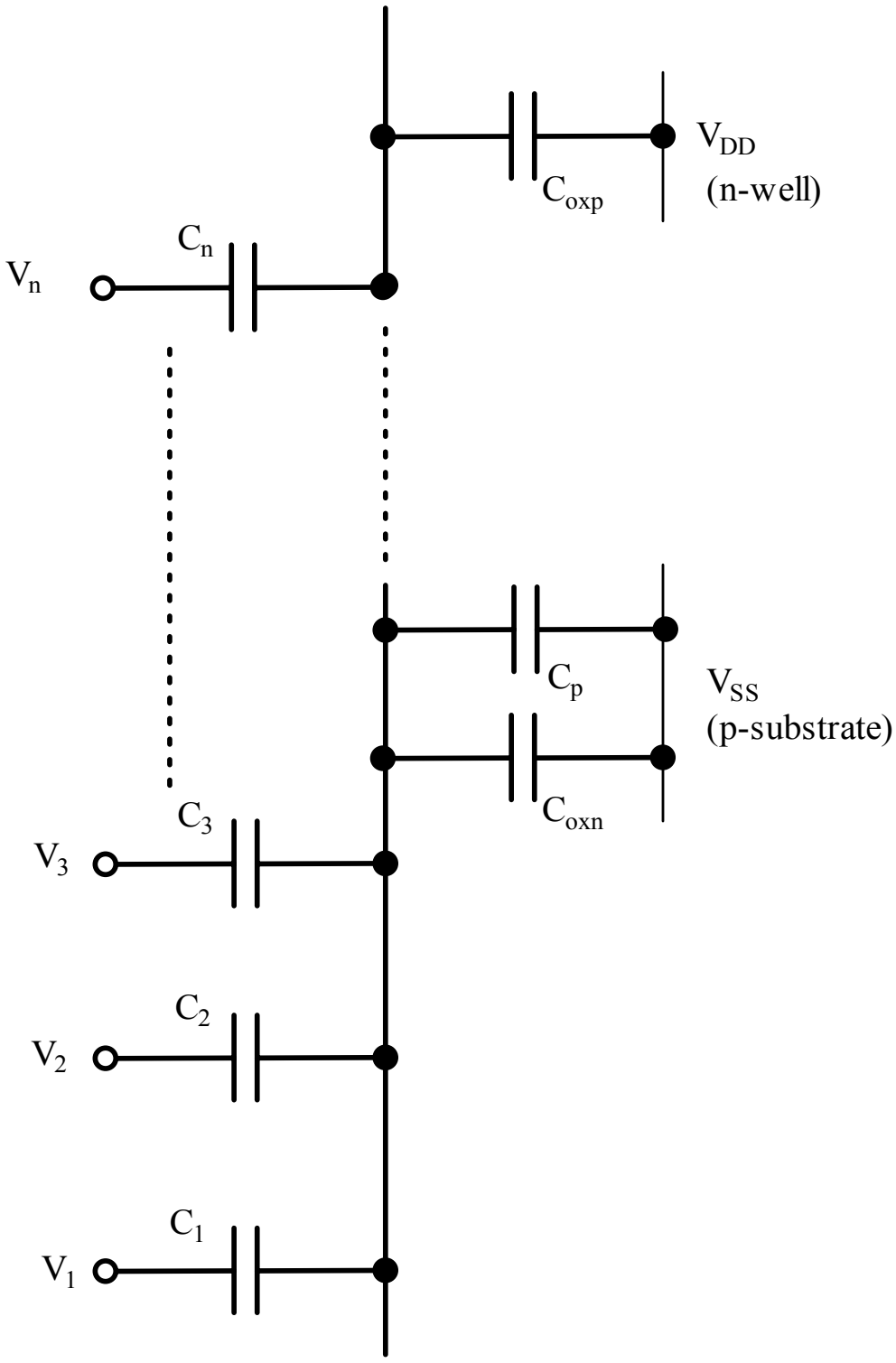



Figure 2.5: The capacitive network for a multi-input floating gate CMOS inverter [24].

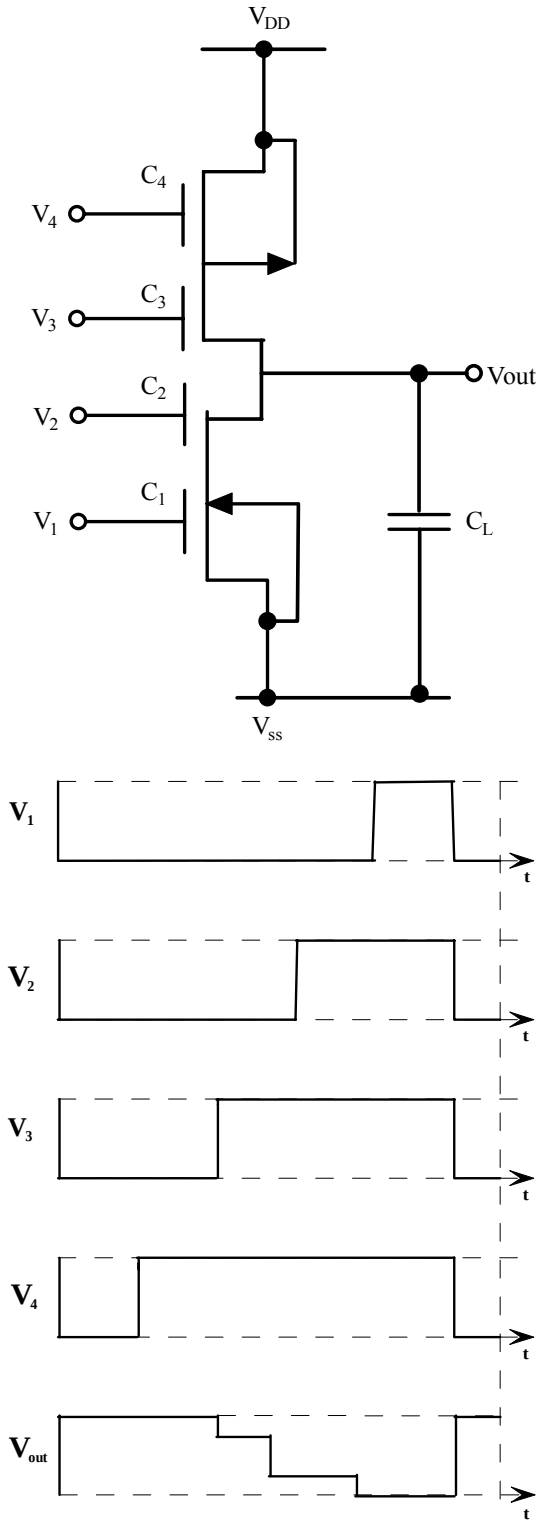



Figure 2.6: Transfer characteristics of a 4-input floating gate CMOS inverter.

multiples of a unit size capacitor. The capacitance between poly1 (poly) and poly2 layers in 1.5 μm standard CMOS process [25] varies from 580 aF/μm$^2$ to 620 aF/μm$^2$ for different runs. Since we do not have prior knowledge of which run would be used in fabrication of our design, an average value has been used. In our design, we have used 596 aF/μm$^2$.

## 2.5 Design Issues

Simulation techniques used for multi-input floating gate CMOS circuits are different from a standard CMOS inverter. Simulation using SPICE gives the problem of DC convergence. It views the capacitors as open circuits initially and stops the simulation run. To overcome the problem different approaches have been explained in [7, 26, 27]. These techniques employ additional use of resistors and voltage controlled voltage sources for specifying the initial floating gate voltage. We have used the method suggested by Yin et al [7], which is described in Appendix B.

# Chapter 3
# Sigma Delta A/D Converter Architecture and Operation

Analog-to-digital converters provide the link between the analog signal world and the binary digital computational systems and is so needed in all digital signal processing applications. The analog signal domain to be converted to digital domain can originate from many types of transducers that convert physical phenomena, temperature, pressure, position, motion, sound, images, etc; to electrical signals [12]. The applications of A/D converters include DC instrumentation, process control, automatic test equipment, weigh scales, thermo-couple sensors, strain gauges, modems, audio recording for compact disc and digital audio tape, workstations, digital radio, video signal acquisition and storage oscilloscopes. These A/D converters are easily implementable in present day technology such as CMOS VLSI technology. The signal frequency ranges from DC to 10's or 100's of MHz and required resolutions are from 6-8 to 20 + bits [28].

## 3.1 Quantization and Sampling

The main distinction of DAC and ADCs are, ADCs must be sampled. It is not possible to continuously convert the incoming analog signal to a digital output data. Therefore, the ADC is a sampled data circuit. Figure 3.1 shows the general block diagram for an ADC [29]. It consists of prefilter, sample and hold, quantizer and encoder blocks. A prefilter also called the anti-aliasing filter is necessary to avoid the aliasing of higher frequency signal back into the base-band of the ADC. The prefilter is followed by a sample-and-hold circuit that maintains the input analog signal to the ADC constant during the time this signal is converted to an equivalent output digital code. This period of time is called the conversion time of the ADC, which is accomplished by quantization

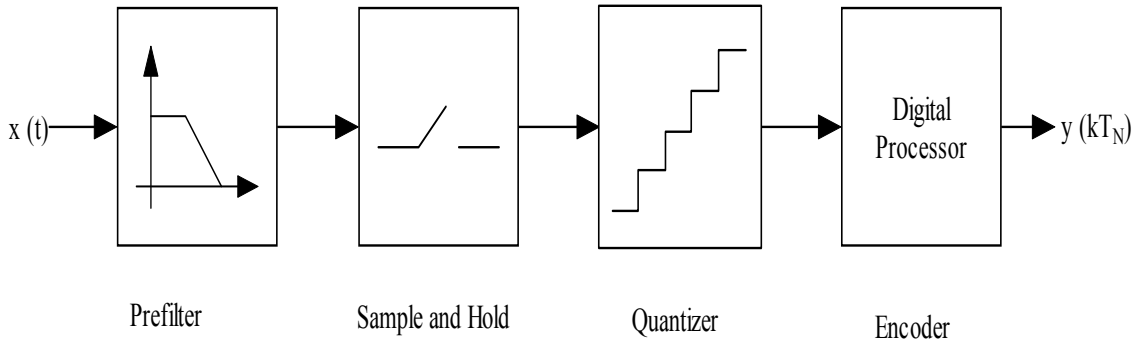



Figure 3.1: Block diagram of general ADC [29].

step. The quantizer divides the reference into sub-ranges. Generally, there are $2^N$ sub-ranges, where N is the number of bits of the digital output data. The quantization block finds the sub-range that corresponds to the sampled analog input. Consequently, the encoder i.e., digital processor in the block diagram encodes the corresponding digital bits. Within the conversion time, a sampled analog input signal is converted to an equivalent digital output code.

The frequency response of the above ADC block diagram shown in the Fig. 3.1, has frequency response shown in Fig 3.2 (a) [29]. From the figure, let us assume $f_B$ is the highest frequency of the analog input signal. Fig 3.2 (b) shows the frequency response when the analog input signal is sampled at a frequency of $f_s$. The spectrum of the input signal is aliased at the sampling frequency and each of its harmonics. If the bandwidth of the signal, $f_B$, is increased above $0.5f_S$, the spectra begin to overlap as shown in Fig 3.2 (c). Now at this point it is not possible to recover the original analog input signal. According to Nyquist theorem, the sampling frequency must be at least twice the bandwidth of the signal in order for the signal to be recovered from the samples [29]. This phenomenon is called Nyquist frequency or rate. Fig 3.2 (d) clearly shows the prefilter in the block diagram is necessary to eliminate signals in the incoming analog input that are above $0.5f_S$. The overlapping of the folded spectra also will occur if the band-width of the analog input signal remains fixed but the sampling frequency decreases below $2f_B$. Even if $f_B$ is less than $0.5f_S$ as in Fig 3.2 (b), then we need an anti-aliasing filter to eliminate the aliasing signal in the upper pass-bands into the base-band which is from 0 to $f_B$ [29]. Consecutively, to make the input bandwidth of the ADC to maximum, $f_B$ should be close to $0.5f_S$.

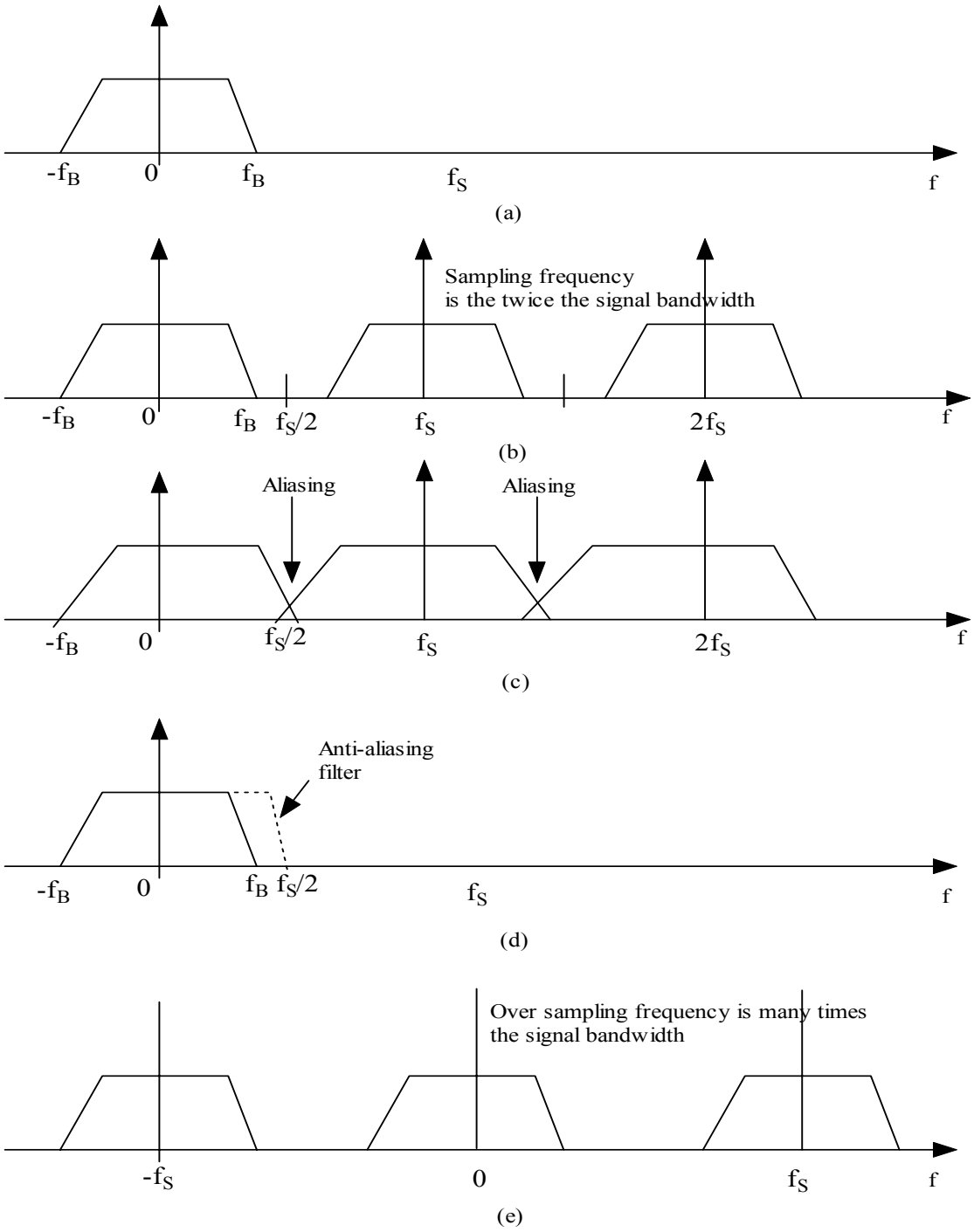



Figure 3.2: (a) Continuous time frequency response of the analog input signal. (b) Sampled-data equivalent frequency response. (c) Case where $f_B > 0.5f_S$, causing aliasing. (d) Use of an anti-aliasing filter to avoid aliasing. (e) Frequency domain of oversampling converter [29].

This requires a very sharp cutoff for the anti-aliasing filter and so this filter design becomes difficult and complex. The types of ADCs that operate in this manner are called *Nyquist ADC's*. We can also make $f_B$ much less than $0.5f_S$. These ADCs are called *oversampling analog-to-digital converters*.

## 3.2 Analog-to-Digital Converter Types

The architecture for A/D converters mainly span around the spectrum of high speed and resolution. There are four different types of architectures available for A/D converters as follows:

1. Flash type ADC's
2. Pipeline ADC's
3. Successive approximation ADC's
4. Oversampled ADC's

In the following sections, the above architectures are discussed. Table 3.1 gives the classification of various types of ADCs that will be discussed in the following sections [29].

The f*lash analog-to-digital converters*, also known as parallel ADC's uses the distributed sampling to achieve a high conversion speed. These are the simplest and potentially the fastest of the entire ADC's available. The flash ADC's do not need explicit front end sample and hold circuits and their performance is determined primarily by that of their constituent comparators. Since comparators do not achieve much higher speeds than sample and hold amplifiers (SHA's), flash ADC's can operate faster than front end SHA's.

Table 3.1: Classification of ADC architectures

| Conversion Type | Nyquist ADCs | Oversampled ADCs |
|---|---|---|
| Slow | Integrating (serial) | Very high resolution >14-bits |
| Medium | Successive approximation<br>(1-bit pipeline architecture) | Moderate resolution > 10-bits |
| Fast | Flash<br>(Multiple-bit pipeline) | Low resolution > 6-bits |

Though flash type ADCs has advantages, on the other hand it suffers from a number of drawbacks due to massive parallelism and lack of front end sampling circuit. Since the number of comparators grows exponentially with the resolution, these ADC's require excessively large power and area for resolutions above 8-bits. Furthermore, the large number of comparators gives rise to problems such as dc and ac deviation of the reference voltages generated by the ladder, large nonlinear input capacitance, and noise at the analog input [30].

In *pipeline ADC's*, each stage carries out an operation on a sample, provides the output for the following sampler and once that sampler has acquired the data begins the same operation on the next sample. As every stage incorporates a sample and hold function, the analog data is preserved, allowing different stages to process different samples concurrently. Thus, the conversion rate depends on the speed of only one stage, usually the front end. While the concurrent operation of pipelined converters makes them attractive for high speeds, their extensive linear processing of the analog input relies heavily on operational amplifiers, which are relatively slow building blocks in analog design. A main advantage of the for an N-stage pipeline converter is its high throughput. After an initial delay of N clock cycles, one conversion will be completed per clock cycle. The disadvantage is having the initial N clock cycle delay before the first digital output appears. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion.

The *successive approximation converter* performs a binary search through all possible quantization levels before converging on the final digital data. The simplicity of

the design allows for both high speed and high resolution while maintaining relatively small area.

### 3.2.1 Oversampling ADC Architecture

Oversampling converters are more commonly called delta-sigma converters or charge balancing A/D converters. Delta-sigma converters differ from other ADC approaches by sampling the input signals at a much higher rate than the maximum input frequency. Typically, non-oversampling converters like successive approximation converters discussed in Section 3.2, perform a complete conversion with only one sample of the input signal [11]. Some of the advantages of sigma delta converters include relaxed requirements for anti-alias filters, relaxed requirements for component matching, high resolution and compatibility with digital VLSI technology [31].

The advantage of this architecture is they trade greatly reduced analog circuit accuracy requirements for increased digital circuit complexity. This is a distinct advantage for 1 to 2 μm technologies [12]. The oversampling converters have been used for high accuracy, 12-bits and beyond, A/D conversion of DC through moderately high AC signals. The block diagram of oversampled sigma-delta A/D converter is shown in Fig. 3.3 [12]. This is also called an integrating type of A/D converter.

The single-bit feedback D/A converter output is subtracted from the analog input signal, $V_A$ in the summing amplifier. The resultant error signal from the summing amplifier output is low-pass filtered by the integrator and the integrated error signal polarity is detected by the single comparator. This comparator is effectively a 1-bit A/D converter. The output of comparator drives the 1-bit D/A converter to a ‘1’ or ‘0’; a ‘1’ if during the previous sample time, the integrator output was detected by the comparator as

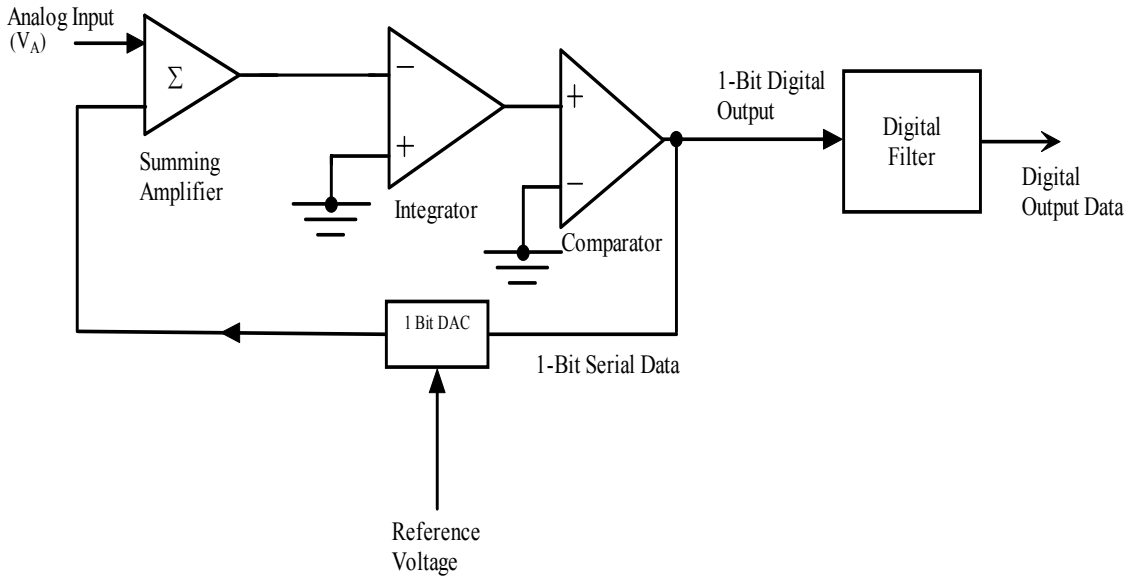



Figure 3.3: Oversampled sigma-delta ADC.

being too low, that is, below 0-V, a '0' if the difference detected during the previous sample was too high, that is, above the 0-V reference of the comparator.

The 1-bit D/A converter, as in successive approximation A/D converters, provide the negative feedback. This negative feedback for a '1' in the D/A converter is always in a direction to drive the integrator output toward 0V. The D/A converter output for a '1' input would be the reference voltage. The reference voltage would be equal to or exceed the expected full-scale analog input signal voltage. Then for a small value of $V_A$, the integrator would take many clock pulses to cross 0V, after a single '1' was generated, during which time the comparator is sending 0's to the digital filter. If $V_A$ were at full scale, the integrator would cross zero every clock time and the comparator output would be a string of alternate '1's and '0's. The digital filter's function is to determine a digital number at its output that is proportional to the number of '1's in the previous bit stream from the comparator. Various types of digital filters are used to perform this computational function, which is the most complex function in this type of A/D converter.

These oversampled converters sample at much higher rates than the Nyquist rate. The oversampling ratio is equal to the actual sampling rate divided by the Nyquist rate. The oversampling rate can be hundreds to thousands of times the analog input signal frequency bandwidth. Since each sample is a one bit (1-bit) low accuracy conversion, sampling rates can be very high.

The bandwidth of signals converted can be significantly increased by a delta-sigma A/D converter at a given clock sampling rate by using a multibit A/D and D/A converter rather than a single bit A/D and D/A converter [12]. Digital filter design is also

a variable affecting the bandwidth of signal that can be accurately converted for a given oversampling rate.

## 3.3 Delta Modulation

The work on sigma-delta modulation was developed as an extension to the well established delta modulation. Figure 3.4 (a) shows the block diagram for delta modulation and demodulation structure for the A/D conversion process. In delta modulation, the knowledge of past information is used to simplify the coding technique and the resulting signal format. The signal is first quantized into discrete levels, but the size of each step in the staircase approximation to the original function is kept constant [32]. Therefore, the quantized signal is constrained to move by only one quantization level at each transition instant. Delta modulation is based on quantizing the change in signal from sample to sample rather than the absolute value of the signal at each sample. The quantized signal must change at each sampling point. Once the quantization is performed, the modulator transmits a string of 1's and 0's. A '1'can indicate a positive transition, and a '0' indicates a negative transition.

The output of the integrator in the feedback loop tries to predict the input x(t). Here the prediction error is given by $x(t) - \bar{x}(t)$. This term in the current prediction is quantized and used to make the next prediction. And the difference is quantized into one of two values + Δ or – Δ depending on the difference as shown in the Figure 3.4 (b) [33]. The delta modulation output is integrated in the receiver just as it is in the feedback loop. Therefore the receiver predicts the input signals as shown in the Figure. The predicted signal is then passed through a low-pass filter.

Delta Modulation requires two integrators for modulation and demodulation as we seen in the Figure 3.4 (a). Since integration is a linear operation, the second integrator can be moved before the modulator without altering the input and output characteristics. Now, the two integrators can be combined into a single integrator by the linear operation property. This arrangement is called Sigma-Delta Modulation.

## 3.4 Comparison of Different Architectures

In the previous sections, we have briefly mentioned the four major circuit architectures used in A/D converter (ADC) design and outline the role they play in converter choice for various kinds of applications. An overwhelming variety of ADCs exist on the market today, with differing resolutions, bandwidths, accuracies, architectures, packaging, power requirements and temperature ranges, as well as host of specifications, covering a broad range of performance needs. And indeed, there exists a variety of applications in data-acquisition, communications, instrumentation and interfacing for signal processing, all having a host of differing requirements. In this section, we will have a brief overlook of all four architectures and discussed the advantages and disadvantages of each architecture over other.

The flash architecture has the advantages of being very fast, because the conversion occurs in a single ADC cycle. The disadvantage of this approach is that it requires a large number of comparators that are carefully matched and properly biased to ensure that the results are linear. Since the number of comparators needed for an n-bit resolution ADC is equal to $2^n$-1, limits of physical integration and input loading keep the maximum resolution fairly low. For example, an 8-bit ADC requires 255 comparators and 16-bit ADC with flash architecture require 65,535 comparators [34].

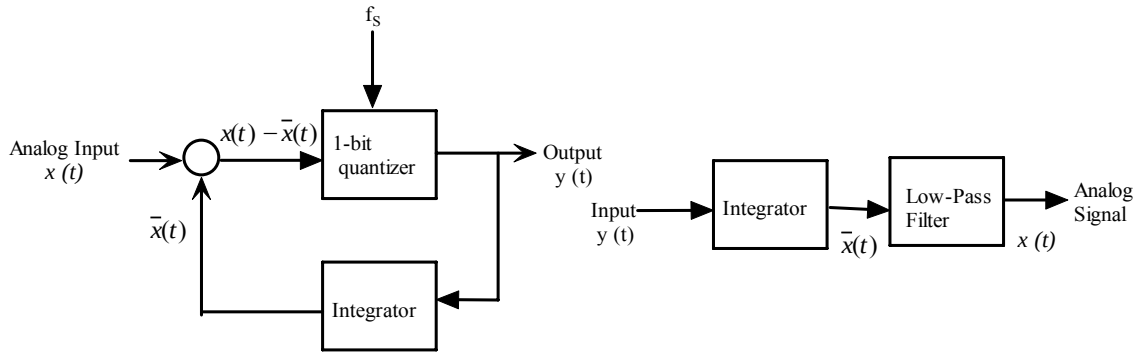



Figure 3.4 (a): Delta Modulation and Demodulation.

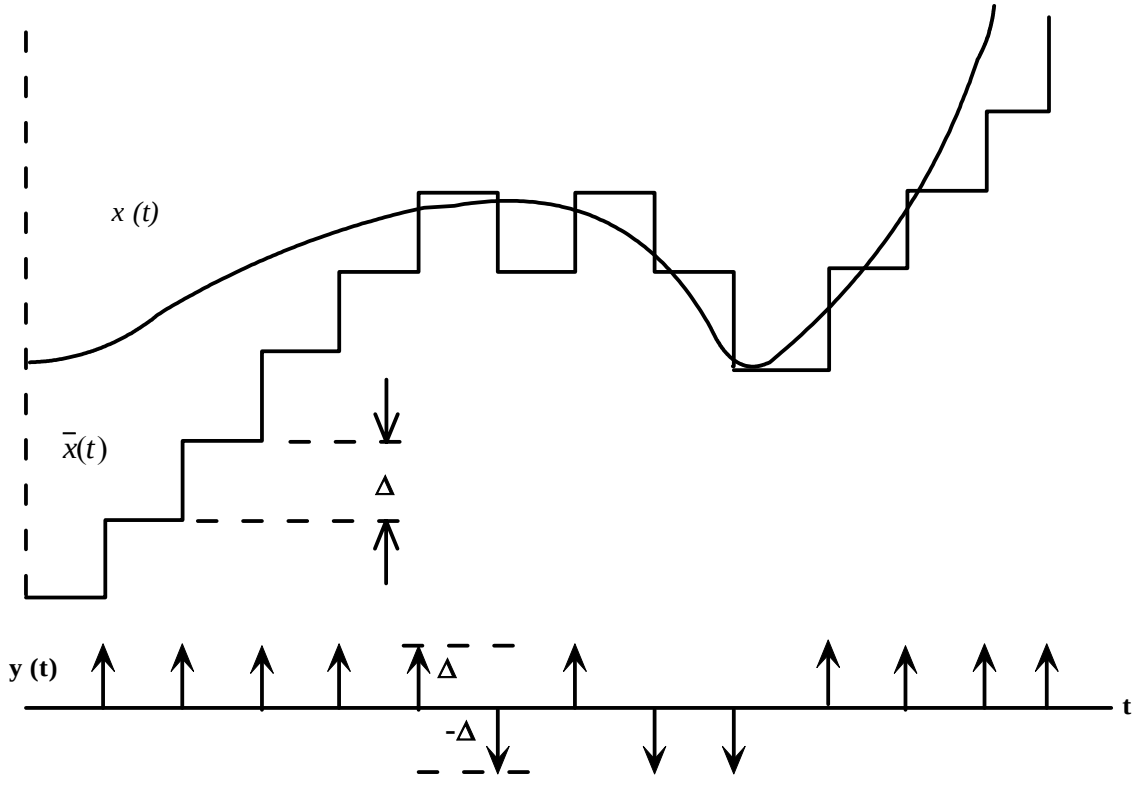



Figure 3.4 (b): Delta Modulation waveforms [33].

The pipelined architecture effectively overcomes the limitations of flash architecture. Pipelined architectures achieve higher resolutions than flash converters containing a similar number of comparators. This comes at the price of increasing the total conversion time from one cycle to p cycles, where p is the number of pipelined stages. But since each stage samples and holds its input, p conversions can be underway simultaneously. The total throughput can therefore be equal to the throughput of a flash converter, i.e. one conversion per cycle. The difference is that for the pipelined converter, we have now introduced latency equal to p cycles. Another limitation of the pipelined architecture is that conversion process generally requires a clock with fixed period. Converting rapidly varying non-periodic signals on a traditionally pipelined converter can be difficult because the pipeline typically runs at a periodic rate [34].

The successive approximation architectures can be thought of as being at the other end of the spectrum from the flash architecture. While a flash converter uses many comparators to convert in a single cycle; a SAR converter, conceptually uses a single comparator over many cycles to make its conversion. So a SAR converter uses a single comparator to realize a high resolution ADC. But it requires n comparison cycles to achieve n-bit resolution, compared to p cycles for pipelined converter and 1 cycle for a flash converter. Since a SAR converter uses a fairly simple architecture employing a single SAR, comparator, and DAC and the conversion is not complete until all weights have been tested, only one conversion is processed during n comparison cycles. For this reason, SAR converters are also well suited for applications that have non-periodic inputs, since conversions can be started at will. So this architecture is ideal for converting a series of time-independent signals. A single SAR converter and an input multiplexer are

typically less expensive to implement than several sigma-delta converters. For every doubling of sampling rate, the effective resolution improves by 3dB or ½ bit [34].

One of the most advantageous features of the sigma-delta architecture is the capability of noise shaping, a phenomenon by which much of the low-frequency noise is effectively pushed up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low-bandwidth high resolution ADCs for precision measurement. Also, since the input is sampled at a high "oversampled" rate, unlike the other architectures, the requirement for external anti-alias filtering is greatly reduced. A limitation of this architecture is its latency, which is substantially greater than that of the other types. Because of oversampling and latency, sigma-delta converters are not often used in multiplexed signal applications. To avoid interference between multiplexed signals, a delay at least equal to the decimator's total delay must occur between conversions. These characteristics can be improved in sophisticated sigma-delta ADC designs by using multiple integrator stages or multi-bit DACs [34].

The sigma-delta and SAR architectures have similar resolution and throughput performance. Yet the differences in their underlying architectures make one or the other a better choice, depending on the application. The following Table 3.2 summarizes the relative advantages of flash, pipelined, SAR, and sigma-delta architectures [34]. A rank of 1 in the performance category indicates that the architecture is inherently better than the others in that category. And for the last three characteristics, the table lists which architecture has the capability of that performance.

Table 3.2: Comparison of the performance characteristics for four major ADC architectures.

| Characteristics | Flash | Pipeline | SAR | Sigma-delta |
|---|---|---|---|---|
| throughput | 1 | 2 | 3 | 4 |
| resolution | 4 | 3 | 2 | 1 |
| latency | 1 | 3 | 2 | 4 |
| suitability for converting multiple signals per ADC | 1 | 2 | 1 | 3 |
| capability to convert non-periodic multiplexed signals | 1 | 2 | 1 | 3 |
| simplified anti-aliasing | - | - | - | better |
| can undersample? | Yes | Yes | Yes | - |
| can increase resolution through averaging? | Yes | Yes | Yes | - |

Note: 4 to1 toward better characteristics.

## 3.5 The First Order Sigma-Delta Modulator

The block diagram of a first order sigma delta modulator is shown in Fig. 3.5, which consists of a integrator, a comparator, which acts as an ADC and 1-bit DAC, which is placed in the feedback loop. The name first order is derived from the information that there is only one integrator in the circuit, placed in the forward path. When the output of the integrator is positive, the comparator feeds back a positive reference signal that is subtracted from the input signal of the integrator. Similarly, when the integrator output is negative, the comparator feeds back a negative signal that is added to the incoming signal. The integrator therefore accumulates the difference between the input and quantized output signals from the DAC output which is in feedback loop and makes the integrator output around zero. A zero integerator output implies that the difference between the input signal and the quantized output is zero [29].

Oversampling analog to digital converters generally use switched-capacitor techniques and hence do not use sample and hold circuits unlike in other ADC architectures. The output of the modulator is a pulse density modulated signal that represents the average of the input signals. The modulator is able to construct these pulses in real time, and so it is not necessary to hold the input value and perform the conversion. The modulator provides the quantization in the form of a pulse density modulated signal. The density of pulses represents the average value of the signal over a specific period. Figure 3.6 demonstrates the modulator operation for a sine wave input signal. The amplitude of sine wave is 2V p-p and the quantizer levels are at ±2.5V. When the input signal approaches the value 2V, the modulator output is dominated by positive pulses. On the other hand, when the input is around -2V, the output has few positive

pulses. It primarily consists of negative pulses. For inputs around zero, the output oscillates between two levels. The average of the output can efficiently be computed by decimator. Here the input range must be kept in between the two quantizer levels. Beyond this range, the modulator output saturates and cannot accurately represent the average value of the input. From the Fig. 3.6, we can clearly observe that for the peak of the sine wave, most of the pulses are high and as the sine wave decreases in value, the pulses become distributed between high and low according to the sine wave value. If the frequency of the sine wave represented the highest frequency component of the input signal, a Nyquist rate ADC would take only two samples. On the other hand, the oversampling converter, take hundreds of samples over the same period to produce this pulse-density signal.

### 3.5.1 Design of Integrator

The integrator is the most important component in a sigma-delta modulator. As discussed earlier, oversampling converters typically use switched-capacitor circuits and therefore do not need sample-and-hold circuits. In many analog and mixed-signal devices, SC circuits perform linear analog signal processing. They are used in various practical applications, such as data converters, analog filters, sensor interfaces, etc. [15]. The basic building block of most SC circuits is the stray insensitive integrator as shown in Fig. 3.7 [35]. It is the conventional non-inverting SC integrator which is used in our analog to digital converter architecture. The frequency response of the integrator is sensitive to the various parasitic capacitances presented on all the nodes in the circuit. However, there are some limitations on the operation of switches with low supply

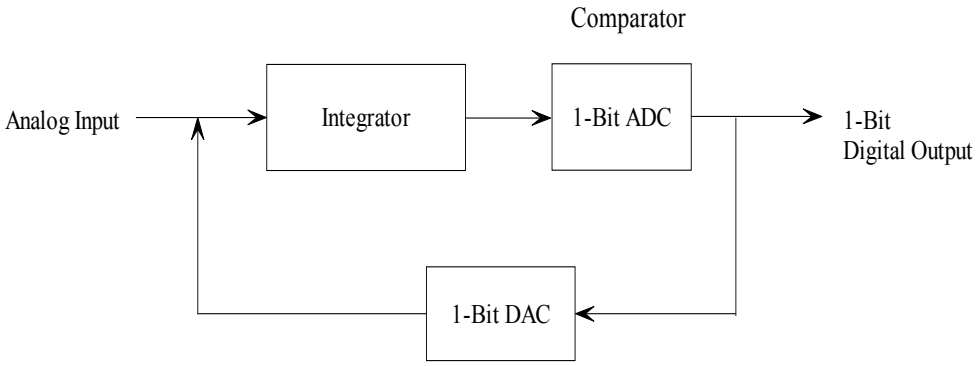



Figure 3.5: Block diagram of a first order sigma-delta modulator.

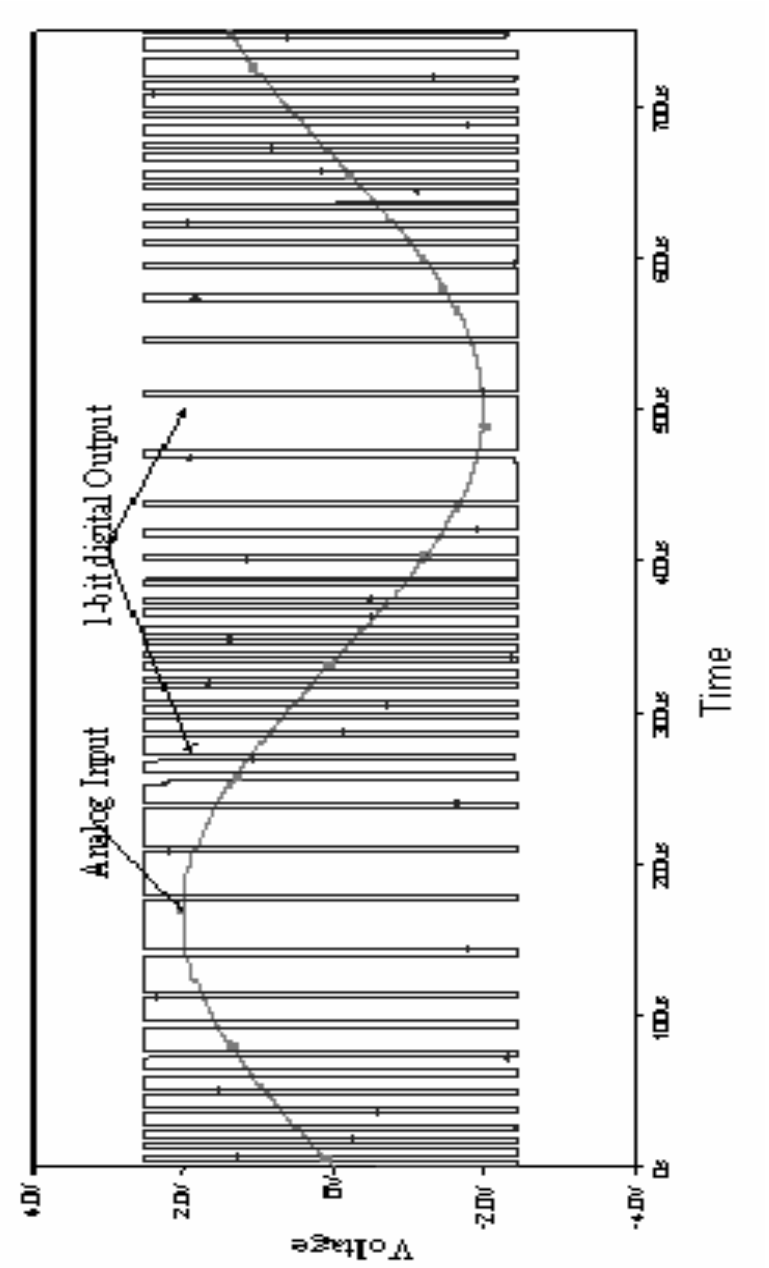



Figure 3.6: Pulse density output from a sigma-delta modulator for a sine wave input.

voltages. The low supply voltage may not allow enough overdrive to turn on the transistors used as switches even if complementary switches are used.

As seen from Fig. 3.6, the SC integrator consists of an op-amp, a sampling capacitor $C_S$, an integrating capacitor $C_I$, and four MOS transistor switches. Figure 3.8 shows the timing diagram of two non overlapping clock signals, $\Phi_1$ and $\Phi_2$, which control the operation of the circuit. The common mode voltage $V_{CM}$ is halfway between the mixed signal systems high reference voltage (+2.5V) and low reference voltage (-2.5V). Hence the common mode voltage, $V_{CM}$ is 0V.

During the interval when clock phase $\Phi_1$ is high, switches $S_1$ and $S_3$ operate and serve to charge the sampling capacitor, $C_S$ to a voltage that is equal to the input voltage. Subsequently, clock signal $\Phi_1$ falls. Then clock signal $\Phi_2$ rises, causing switches $S_2$ and $S_4$ to turn on and the sampling capacitor, $C_S$ to be connected between the inverting op-amp input, which is sometimes called the summing node, and ground. If the op-amp is ideal, the resulting change in the summing-node voltage causes the op-amp output to change so that the summing-node voltage is driven back to ground. After the transient has gone to completion, the voltage across $C_S$ is driven to zero.

To find the relationship between the input and output, a charge-conservation analysis is used. After switch $S_1$ opens, the charge on the plates of the capacitors connected to node top and the inverting op-amp input is conserved until switch $S_1$ closes again. Now define two points [n] and [n+1/2] as the time indices at which $\Phi_1$ and $\Phi_2$ first fall as shown in Fig. 3.8. Point [n+1] is defined as the next time index at which $\Phi_1$ falls. The points [n] and [n+1] are separated by one clock period T. If the switches and the op-amp are ideal, the charge stored at time index [n] is [36],

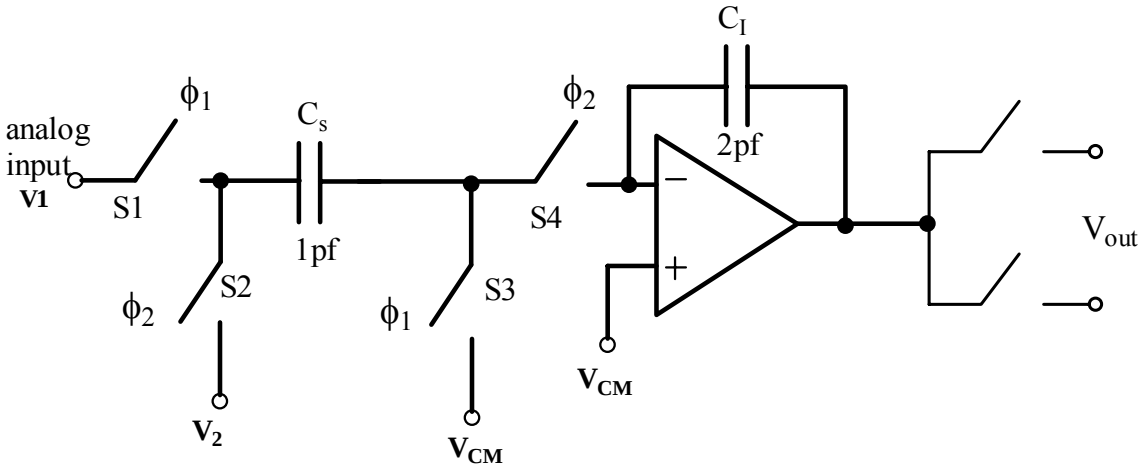



Figure 3.7: A conventional noninverting integrator.

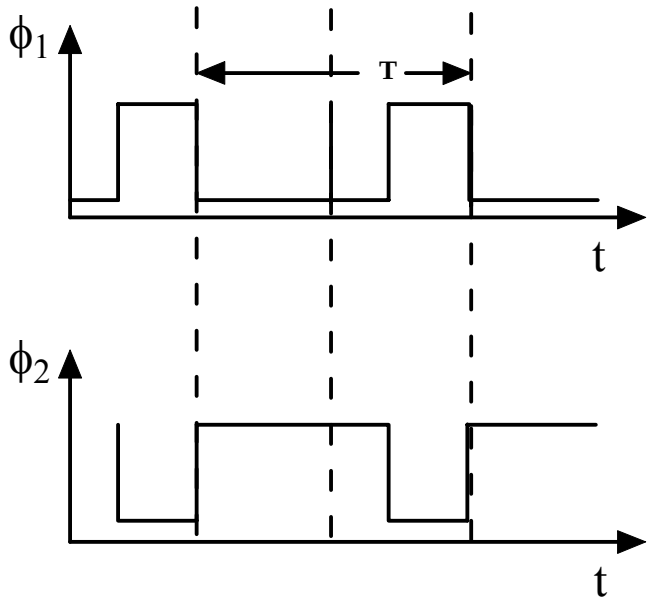



Figure 3.8: Timing diagram for the two clock signals.

$$Q[n] = (0-V_S[n])\, C_S + (0-V_O[n])C_I \qquad (3.1)$$

Where, $V_S$ represents the input voltage at the end of $\Phi_1$ and $V_O$ represents the output voltage at the end of $\Phi_2$. Here, if the op-amp is ideal, the voltage $V_i$ from the inverting op-amp input to ground is driven to zero by negative feedback during $\Phi_2$.

At the same conditions, the charge stored at time index [n+1/2] is

$$Q[n+1/2] = (0)C_S + (0-V_O\,[n+1/2])C_I \qquad (3.2)$$

For charge conversation, Q[n+1/2] = Q[n]. Also, the charge stored on $C_I$ is constant during $\Phi_1$under these conditions, therefore, $V_O$ [n+1] = $V_O$ [n+1/2]. Combining these equations gives,

$$V_O\,[n+1] = V_O\,[n] + (C_S/C_I)\, V_S[n] \qquad (3.3)$$

Thus, one complete clock cycle results in a change in the integrator output voltage that is proportional to the value of the input voltage and to the capacitor ratio.

The above equation is used to find the frequency response of the integrator by using the fact that the signal is delayed by a clock period T in the time domain. The equation in z-domain results in [36],

$$v_o(z)(1-z^{-1}) = \frac{C_S}{C_I}(v_1(z).z^{-1} - v_2(z).z^{-1/2}) \qquad (3.4)$$

The transfer function of the DAI with the output connected to the $\Phi_1$ switches is given by [32],

$$v_o(z) = \frac{C_S}{C_I}.\frac{(v_1(z).z^{-1} - v_2(z).z^{-1/2})}{1-z^{-1}} \qquad (3.5)$$

Note that if $v_2(z) = V_{CM}$, this equation can be written as [32],

$$v_{out}(z) = \frac{C_S}{C_I} \cdot \frac{z^{-1}}{1 - z^{-1}} . v_1(z) \qquad (3.6)$$

The equation (3.6) is used for the integrator in the design of modulator. The values of capacitances are shown in the figure i.e. $C_S$ = 1 pF and $C_I$ = 2 pF so that the gain of the integrator is 0.5. Here the gain is kept less than 1 to make the first order modulator loop stable and also to avoid the integrator from saturating. The capacitance ratio is important than the individual values of the capacitors. Even smaller capacitances can be used but to avoid charge leakage problem they are taken high.

### 3.5.2 Design of Operational Amplifier with Floating Gates at Input Stage

The op-amp is the key element of most analog subsystems particularly in switched capacitor techniques and the performance of many circuit is influenced by the op-amp performance [37]. Operational amplifiers have sufficiently high voltage gain so that when the negative feedback is applied, the closed-loop transfer function can be made practically independent of the gain of the op-amp. This principle is employed in many useful analog circuits and systems. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement the negative feedback concept. One of the popular op-amp is a two stage op-amp. The two stage op-amp introduces an important concept of compensation. The primary goal of compensation is to maintain stability when negative feedback is applied around the operational amplifier. The block diagram of a typical two stage op-amp is shown in Fig. 3.9 [10].

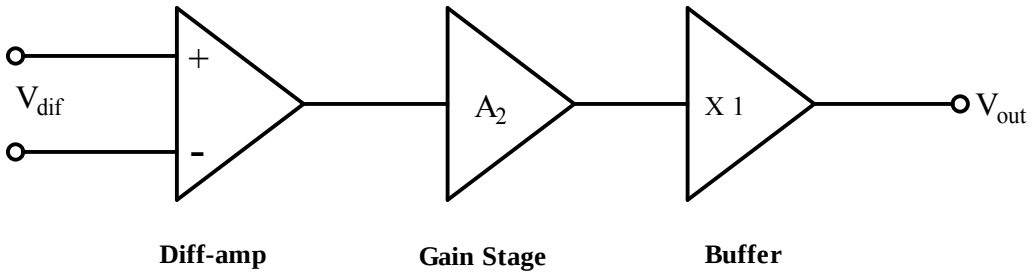



Figure 3.9: Block diagram of a two stage op-amp with output buffer.

From the Fig. 3.9, the first stage of an op-amp, is a differential amplifier. This is followed by another gain stage, such as common source stage, and finally an output buffer. If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. On the other hand, if the op-amp is to drive a resistive load or a large capacitive load, the output buffer is used. Design of op-amp consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp loop gain, common-mode range (CMR) on the input, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), output voltage range and power dissipation. In our design, the differential amplifier has floating gate MOSFETs at the input stages as shown in the Figure 3.10. This input differential gain stage amplifies the voltage difference between the input voltages, which is independent of their common mode voltage. The additional gain is achieved in second gain stage.

The differential pair in Fig. 3.10 is formed by p-channel MOSFETs, M1 and M2. The first stage gives a high differential gain and performs the differential to single ended conversion. This first stage of op-amp also had the current mirror circuit formed by an n-channel MOSFETs, M3 and M4. The transistor M6 serves as an n-channel common source amplifier which is the second stage of op-amp and is aided by current load M5. The bias of the op-amp circuit is provided by M8 and M9 transistors.

To sustain a constant transconductance from a simple differential pair, we must ensure that the common mode input voltage stays adequately far above ground so that the gate-to-source voltage of the input transistors is large enough to pass a significant

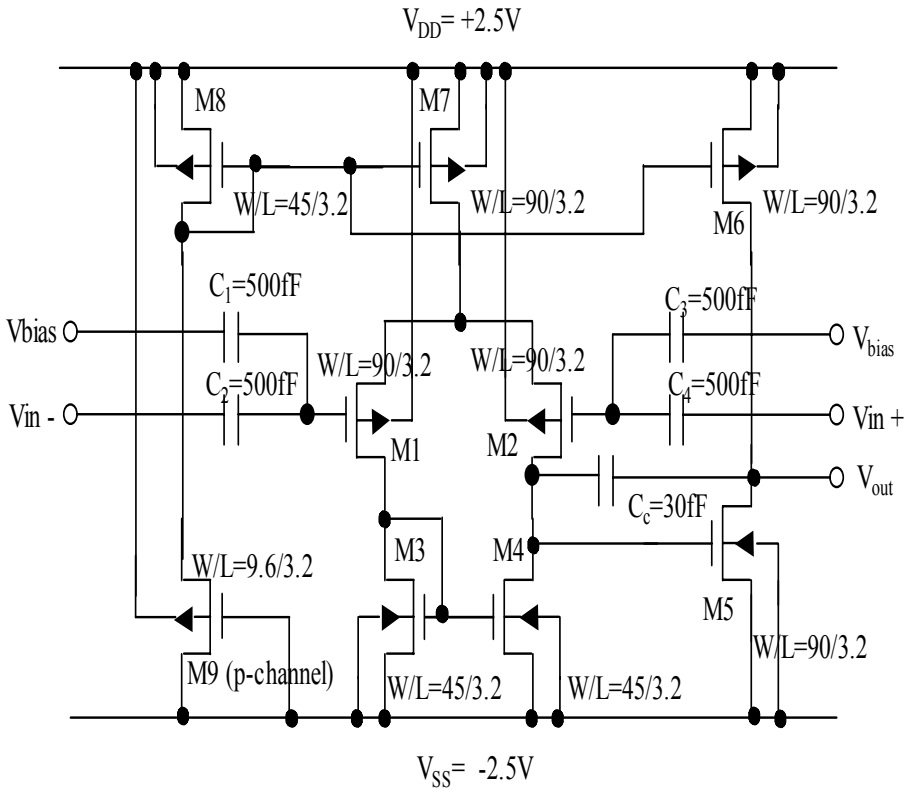



Figure 3.10: Circuit Diagram of a two-stage CMOS operational amplifier.

fraction of $I_b$ as shown in Fig 3.11 and so that the transistor that sinks the bias current remains in saturation.

For bias currents at or near threshold, the input common-mode voltage must remain greater than $V_{TO} + V_{DSsat}$ [38]. One method to overcome the limitation is by using the Floating Gate MOS (FGMOS) transistors. The main benefit of the FGMOS transistors is that we can use the amount of charge, Q, stored on the gates of the FGMOS transistors to shift their threshold voltages, effectively making the FGMOS transistors into depletion mode devices [38]. In this case, the common mode control gate input voltage can be at ground while the common mode floating gate voltage is higher than $V_{TO} + V_{DSsat}$, permitting proper operation of the differential pair. We can increase the charge on the floating gates by adding an extra control gate to each FGMOS transistor, to which we apply a positive bias voltage, $V_{b,}$ as shown in Fig 3.11 [38]. The current mirros using multi-input floating gate transistors have been shown in Fig 3.12 (a), (b) [22].

In Fig. 3.10, a reference current is obtained from the combination of transistors M9 and M8 which is equivalent to a standard resistor diode combination. It is designed to produce a current of 100 μA. The equation (3.7) governs the current flow though the transistors M6, M7 and M8. The current ratio is determined by the aspect ratio of the transistors.

$$\frac{I_7}{I_8} = \frac{W_7 / L_7}{W_8 / L_8} = 200\ \mu\text{A}$$

$$\frac{I_6}{I_8} = \frac{W_6 / L_6}{W_8 / L_8} = 200\ \mu\text{A} \qquad (3.7)$$

All transistors are assumed to be in saturation and neglect the channel length modulation effects.

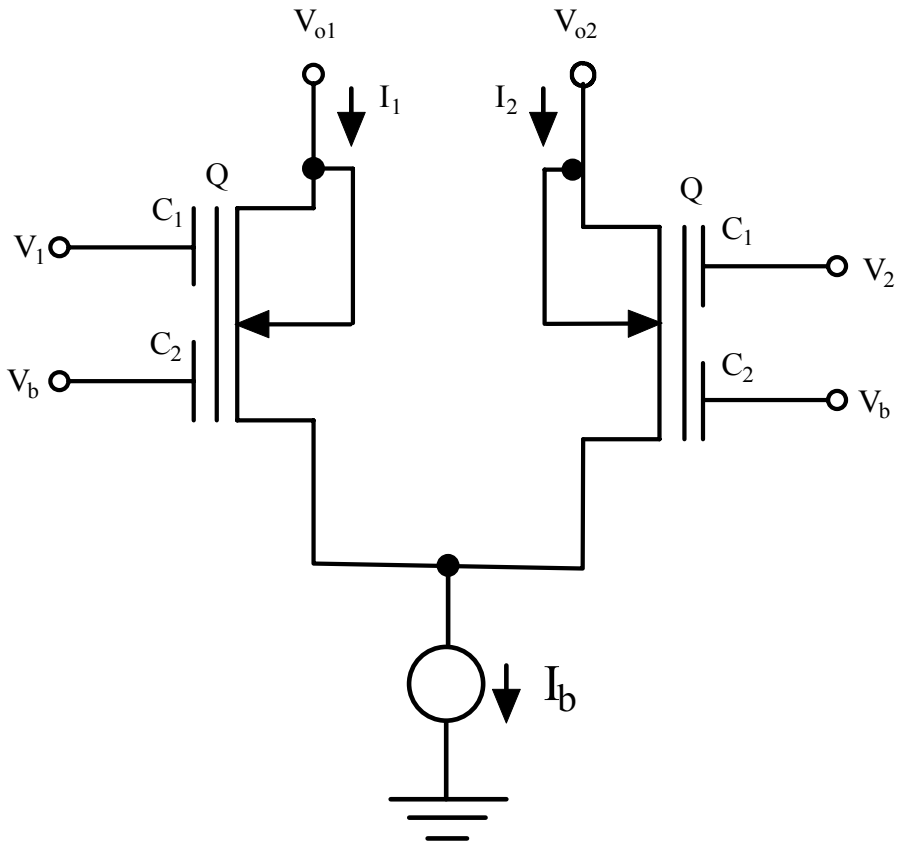
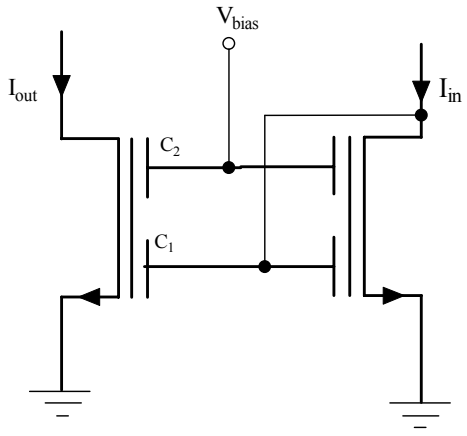
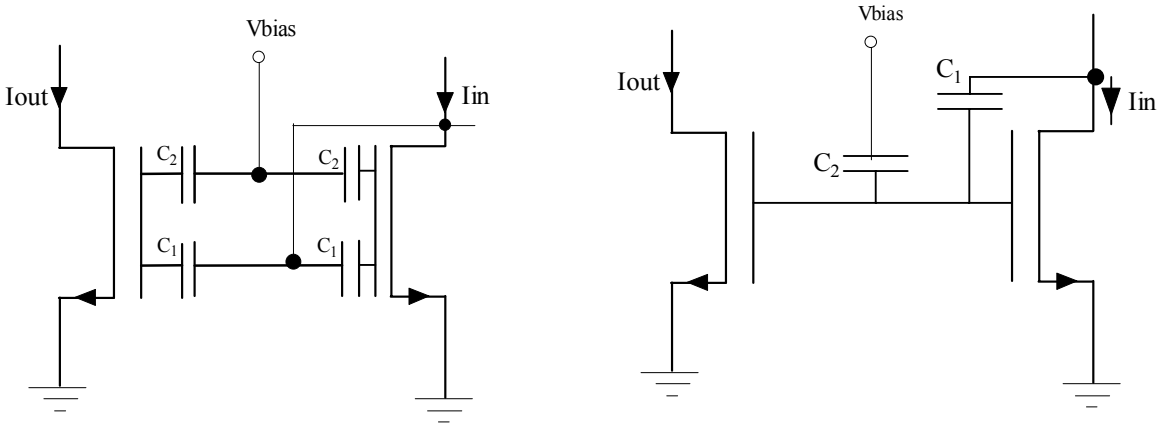



Figure 3.11: A floating gate MOS differential pair [38].




(a)




(b)

Figure 3.12: Building blocks using MIFG transistors [22].
(a) Current Mirror, (b) Implementations.

The input resistance of the OP-AMP is infinite since the inputs are connected to the gates of the transistors. The output resistance is the resistance looking in to the second stage with the OP-AMP inputs connected to small-signal ground and is given by

$$R_O = r_{06} \parallel r_{05} \tag{3.8}$$

The small signal voltage gain of the first stage is given by,

$$A_{v1} = g_{m1}(r_{02} \parallel r_{04}) \tag{3.9}$$

where $g_{m1}$ is the transconductance of $M_1$,

$r_{02}$ and $r_{04}$ are the output resistance of $M_2$ and $M_4$ , respectively.

Similarly the second stage voltage gain is

$$A_{v2} = g_{m6}(r_{06} \parallel r_{05}) \tag{3.10}$$

The overall gain of the amplifier is

$$A_v = A_{v1}A_{v2} = g_{m1}(r_{02} \parallel r_{04})g_{m6}(r_{06} \parallel r_{05}) \cong (g_m r_0)^2 \tag{3.11}$$

As discussed earlier, the differential amplifier needs to be biased by a constant current source, which is provided by the $M_9$ transistor. This current is supplied to the two stages of the operational amplifier by the p-channel current mirrors ($M_8$, $M_7$, $M_6$ ) which provide the bias current for the two stages. In the differential amplifier stage, the differential to single ended conversion is also done which makes the output to taken only from one of the drains of the transistors. Transistor $M_5$ is biased at $I_{D5}$ = 200 μA. The input pair is biased at $-I_{D7}$ = 200 μA. To avoid input offset voltage, transistors $M_3$ and $M_4$ are dimensioned according to

$$\frac{\left(W/L\right)_5}{2\left(W/L\right)_{3,4}} = \frac{-I_{D6}}{I_{D7}} = \frac{200\mu A}{200\mu A} = 1 \rightarrow \left(\frac{W}{L}\right)_{3,4} = \frac{1}{2}\left(\frac{W}{L}\right)_5 = 15 \tag{3.12}$$

where $(W/L)_5 = 30$.

Therefore the W = 45 μm for the transistors $M_3$, $M_4$ to obtain the bias current of 100 μA. The n-channel transistors $M_3$ and $M_4$ acts as load for the p-channel transistors and are used for the single ended conversion also. The second stage of the op-amp provides the additional gain and also the level shift for the output. The second stage is also biased by a current source, which is used to maximize the gain of the second stage. The op-amp device sizes are chosen to get a high gain with high output resistance. The maximum width of the transistors in the op-amp design is 90 μm and the minimum channel length used in the design is 3.2 μm.

The operational amplifier is made stable by using the compensation capacitor. The capacitor introduces a dominant pole and decreases the gain so that the phase margin is positive. Phase margin is defined as how far the phase of the circuit is away from $180^o$ at a gain of 0 dB. A negative phase shift implies that a negative feedback loop acts as positive feedback loop and hence making the loop unstable. In this design, the capacitor introduces a dominant pole, which allows having a phase margin of $56^o$.

Figure 3.13, shows the transfer characteristics obtained from DC sweep analysis. The input offset voltage is approximately 0.276 mV. Figure 3.14 shows the transient analysis of operational amplifier. Figure 3.15 shows the frequency response characteristics. The DC gain of the amplifier is 85 dB. The unity gain bandwidth of the amplifier obtained is approximately 40 MHz. The specification of the floating gate op-amp used in the design of integrator and comparator is shown in the Table 3.3.

Table 3.3: Specifications of the simulated op-amp using post-layout spice simulations

| Specifications | Value |
|---|---|
| DC Gain | 85 dB |
| GBW | 40 MHz |
| Slew Rate | 3.76 V/μS |
| Phase Margin | 56 ° |
| Input offset | 0.276 mV |
| Power Dissipation | 84 μW |

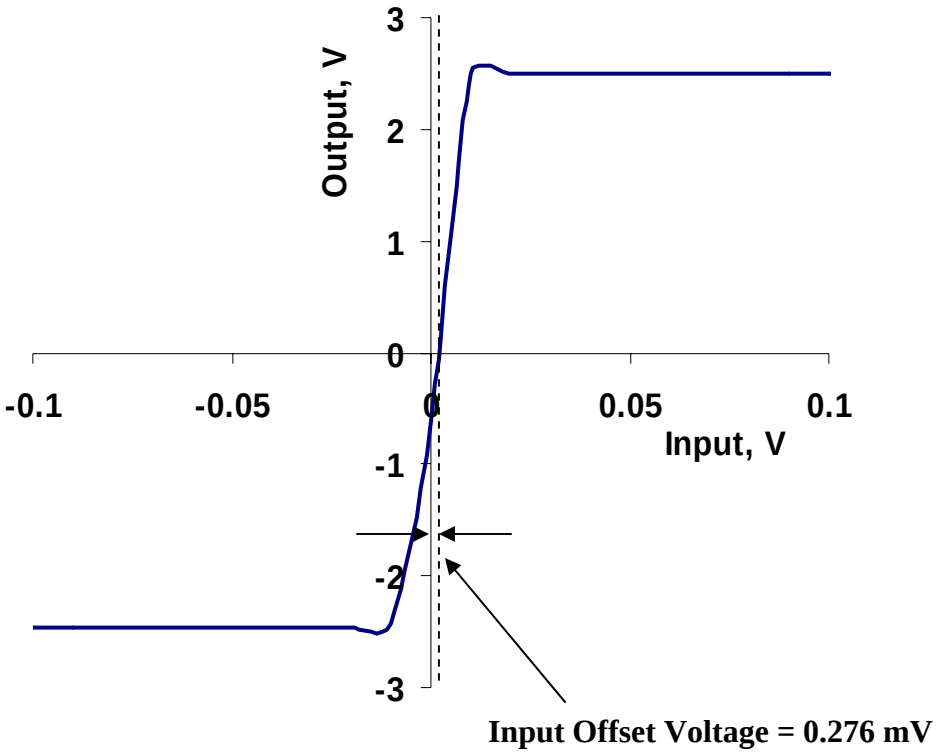
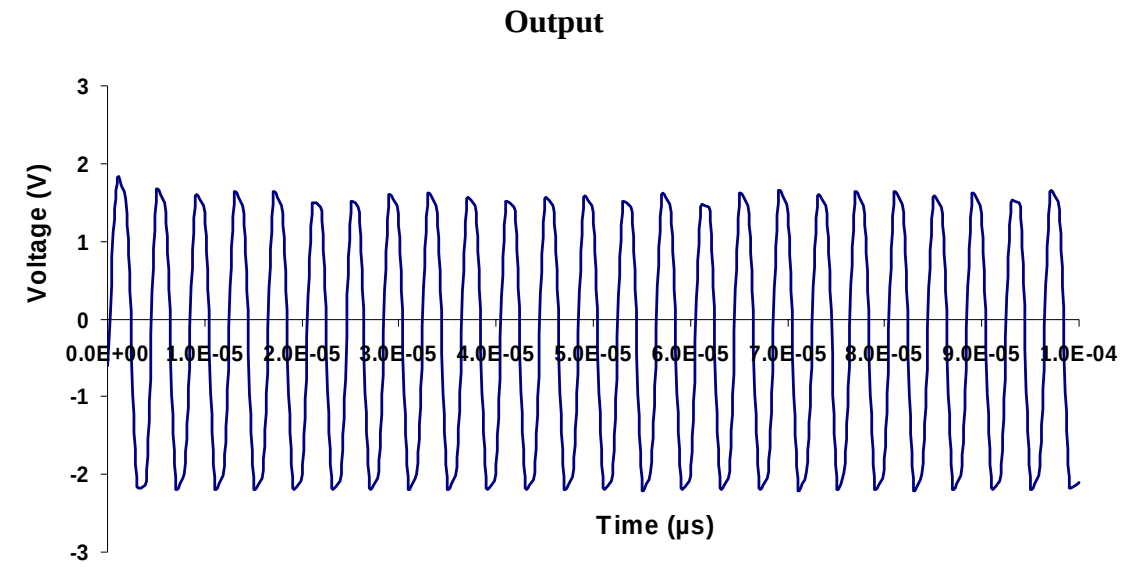



Figure 3.13: Transfer characteristics of op-amp circuit of Fig. 3.9 obtained from post-layout simulations.



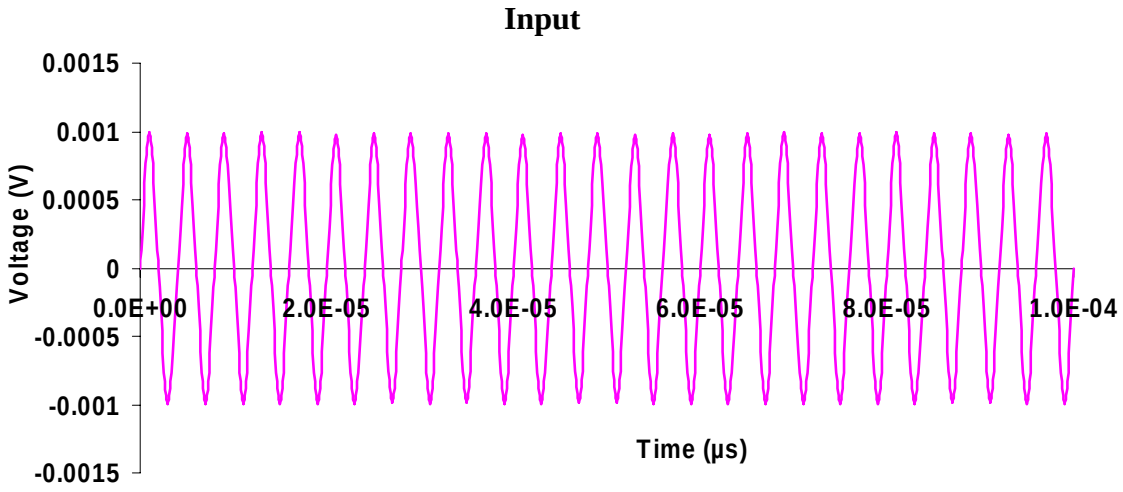




Figure 3.14: Transient analysis of op-amp circuit of Fig. 3.9 obtained from post-layout simulations.

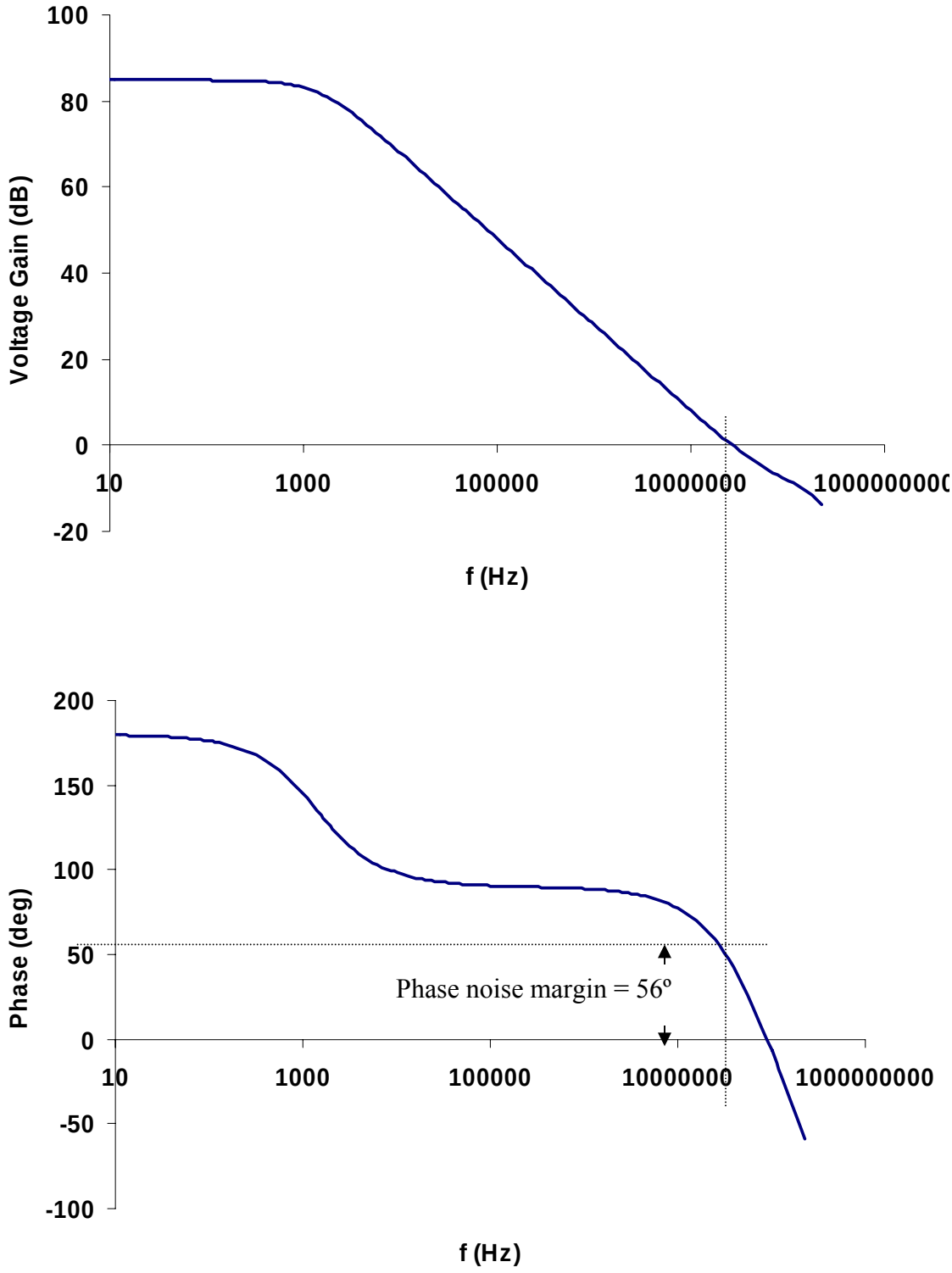



Figure 3.15: Frequency response of op-amp circuit of Fig. 3.9 obtained from post-layout simulations.

### 3.5.3 Design of Comparator

The comparator is widely used in the process of converting analog signal to digital signals. In an analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. In its simplest form, the comparator can be considered as a 1-bit analog-to-digital converter. Hence, in the first order sigma-delta modulator, the comparator i.e. 1-bit analog-to-digital converter acts as the quantizer.

If the output of the previous stage in first order modulator i.e. integrator's output is greater than the reference voltage then comparator has to give an output of '1' and if the integrator output is less than the reference voltage then the output of the comparator should be a '0'. As we observed, 1-bit analog-to-digital converter is of 1-bit, the output will have two levels, a one ('1') or zero ('0'). As $V_{DD}$ in our design is +2.5V, so '1' equals to $V_{DD}$. Similarly a '0' implies $V_{SS}$ which is -2.5V. For a given reference level, the comparator gives an output of $V_{DD}$ when the signal is greater than the reference level and an output of $V_{SS}$ when signal is less than the reference level. A reference level $V_{CM}$ = 0V is used in our design.

The above functionality can easily be implanted by using a simple comparator. The comparator circuit is shown in Fig.3.16. The operational amplifier discussed in the previous section can be used for the design of 1-bit analog-to-digital converter. The basic difference between a comparator and an operational amplifier is that the comparator does not have to be compensated for closed loop feedback as there is no necessity for stability.

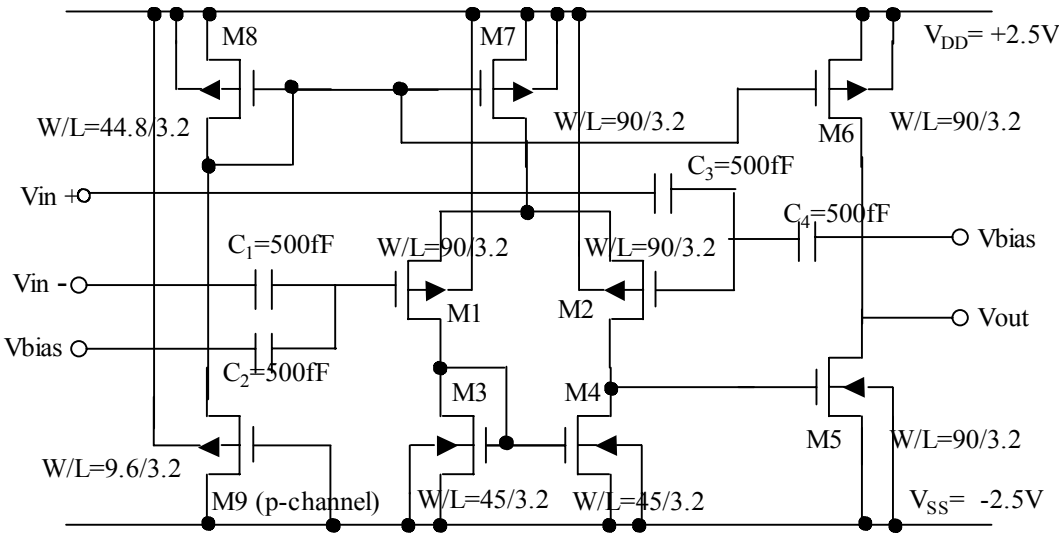



Figure 3.16: Circuit diagram of a CMOS comparator using floating gate MOSFETs.

This means that the internal compensation capacitor is not needed, and this results in an increased output slew rate. Here the comparator uses the operational amplifier with floating gate MOSFETs at the input stages, which is similar to the op-amp in integrator stage. $C_1$, $C_2$, $C_3$ and $C_4$ from the figure represent the floating gate capacitors. The $V_{bias}$ in the circuit of Fig.3.16 is set to +2V.

Comparators are characterized by their voltage gain, slew rate and an offset voltage for a given over drive. Over drive refers to the amount of differential voltage at the input pins, and generally it has a significant effect on the response time. Slew rate (V/μs) is defined as the rate of change of output voltage in the region of constant slope. In typical A/D converter applications, the comparator must slew its output quickly, and without oscillation once the input thresholds are crossed.

The clock frequency of the first order modulator depends on the slew rate of the comparator. The slew rate for the comparator is measured by giving a step input signal and measuring the time it takes for the comparator to reach the final output value. The clock frequency should be less than the slew rate of the comparator. The clock takes half cycle to switch from -2.5V to +2.5V. The maximum allowed clock frequency for the above slew rate would be 10 MHz. When the clock frequency is more than 10 MHz, the comparator output will be distorted. The clock frequency for the modulator was chosen to be 2 MHz taking the parasitic capacitances in to consideration. Apart from voltage gain and slew rate, the other limitation that has to be discussed for the comparator is the offset voltage. Care should be taken to keep the offset voltage very less. If the offset voltage is 'high' the comparator will be unable to switch for that input voltage. The modulator may

show an output of '1' for '0' and '0' for '1', when the integrator output falls within the offset voltage of the comparator.

### 3.5.4 1-bit Digital-to-Analog Converter

The comparator designed as a two-stage CMOS operational amplifier, will give an output of 1-bit digital input to the DAC. This DAC converts the 1-bit digital to an analog signal and fed back to the SC-integrator again as shown in the block diagram of first order modulator of Fig. 1.4. Figure 3.17 shows the circuit level diagram of 1-bit DAC. As the number of bits is only 1-bit, the corresponding analog output will also have two levels and similar to the digital output. The present 1-bit digital-to-analog converter has two reference voltages as shown in Fig. 3.17, a positive reference voltage of $+V_{REF}$ and a negative reference voltage of $-V_{REF}$. The corresponding voltages of $+V_{REF}$ and $-V_{REF}$ are +2.5V and -2.5V, respectively. There are following two cases,

Case 1: If the digital input = '1' then DAC output = $+V_{REF}$

Case 2: If the digital input = '0' then DAC output = $-V_{REF}$

The above logic can easily designed by using a simple multiplexer circuit. The operation of this multiplexer is to select $+V_{REF}$ and $-V_{REF}$ signals depending on the 1-bit digital input signal. Here the DAC is not designed using floating gate MOSFETs, it is designed using a CMOS transmission gates as shown in Fig. 3.17.

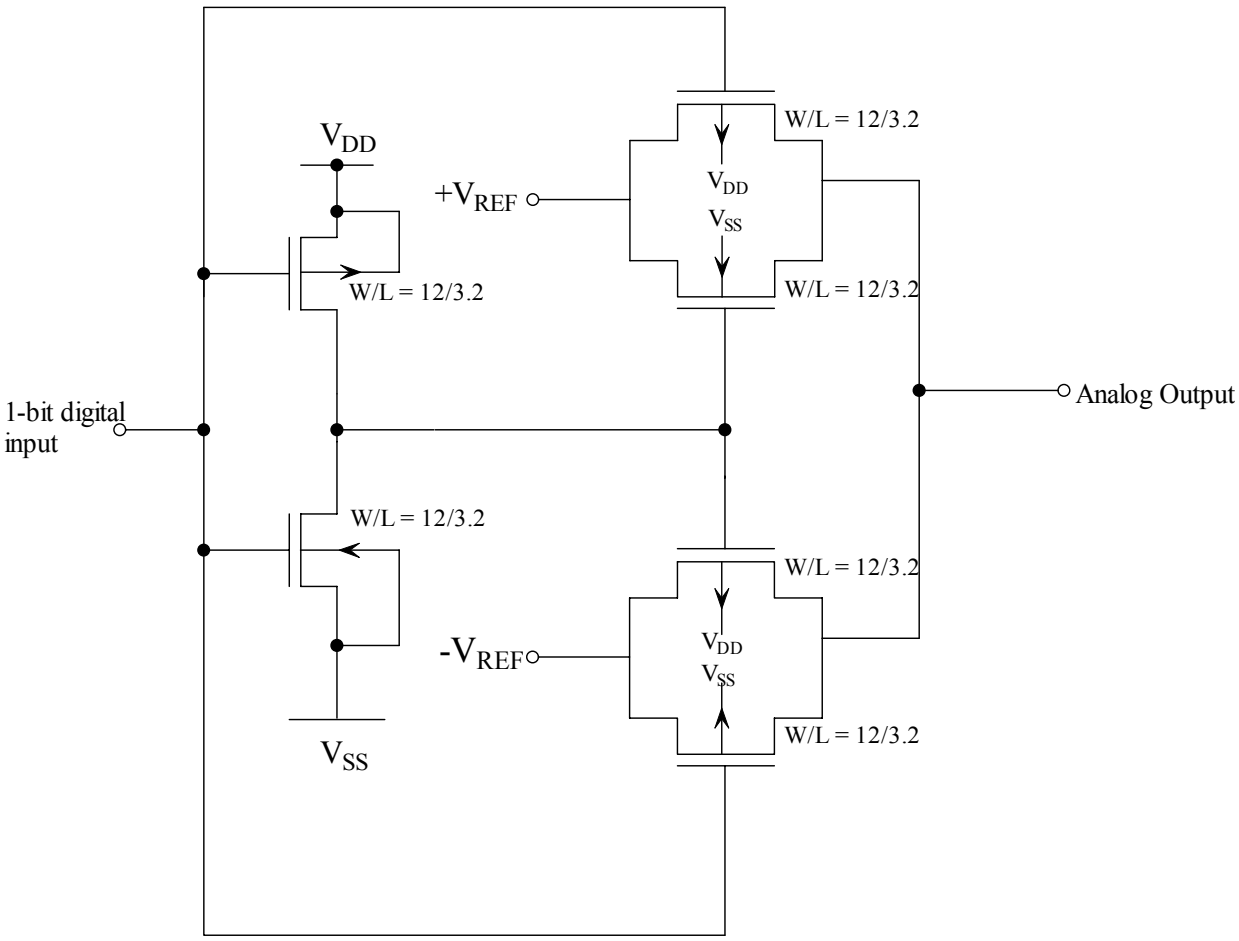



Figure 3.17: Circuit diagram of an 1-bit DAC.

## 3.6 Implementation and Analysis of Modulator

The linearized sampled data equivalent circuit of the first order modulator is shown in Fig.3.18 . From the Fig. 3.18, we notice that the quantization is represented by an additive error (q), defined as the difference between the modulator output, y, and the quantizer input, v. The input-output relation of the modulator for the Fig. 3.18 can be written in terms of a difference equation [29] as,

$$y[nT_S] = x[(n-1)T_S] + q[nT_S] - q[(n-1)T_S] \tag{3.13}$$

The output contains the delayed version of the modulator input and the first order difference of the quantization error. The z-domain equivalent of above equation is given by [29],

$$Y[z] = z^{-1}X[z] + (1 - z^{-1})Q[z] \tag{3.14}$$

here X(z), Y(z) and Q(z) are the z-transforms of the modulator input and output, and the quantization error, respectively. The multiplication factor of X(z) is called the signal transfer function (STF), whereas that of Q(z) is called the noise transfer function (NTF). Note that in the above equations $z^{-1}$represents a unit delay. On the other hand $(1-z^{-1})$ has a high-pass characteristic, allowing noise suppression at low frequencies.

Because of the entirely different quantization process of sigma-delta ADCs, performance metrics of these ADCs cannot be described in terms of integral and differential nonlinearity as in the case of Nyquist rate ADCs. Instead, performance measures such as signal-to-noise ratio, (SNR) and dynamic range (DR) can be used to evaluate the effective number of bits. SNR is defined as the ratio of the signal power to the base band noise power. DR, on the other hand, is the ratio of the power of a full scale sinusoidal input to the power of a sinusoidal input for which SNR is one. DR is also

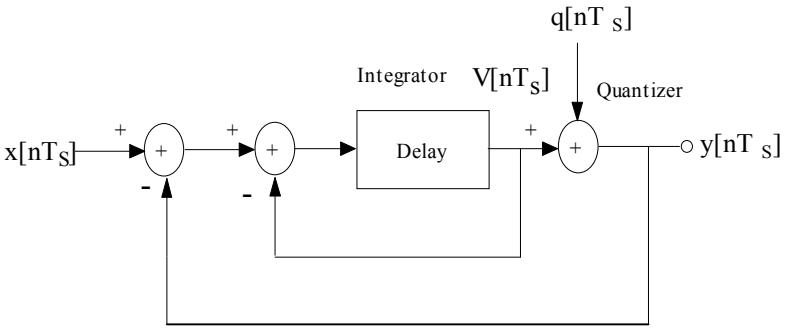



Figure 3.18: Sampled data model of a first order sigma-delta modulator.

called the useful signal range. For a single-bit quantizer with level spacing Δ, that the dynamic range for a first order modulator is given by [29]

$$DR^2 = \frac{3}{2}\frac{3}{\pi^2}M^3 \tag{3.15}$$

where M is the oversampling ratio.

On the other hand, the dynamic range of an N-bit Nyquist rate ADC is given by [29],

$$DR = 6.02N + 1.76 \tag{3.16}$$

For an 8-Bit ADC the dynamic range from the above formula is 49.92 dB. Oversampling ratio (M) to achieve DR= 49.92dB is calculated to be 59.96. To simplify the decimator design, the oversampling ratio is usually chosen in powers of 2 and hence 64 have been chosen as the oversampling ratio.

The complete circuit diagram of the first order modulator is shown in Fig. 3.19 and in Fig. 3.20. The SNR for a modulator assuming an ideal low pass filter at the modulator output is given by [10],

$$SNR_{ideal} = 6.02N+1.76-5.17+30\log M \tag{3.17}$$

In this case N=1 and M=64 and hence $SNR_{ideal}$ =56.79dB.

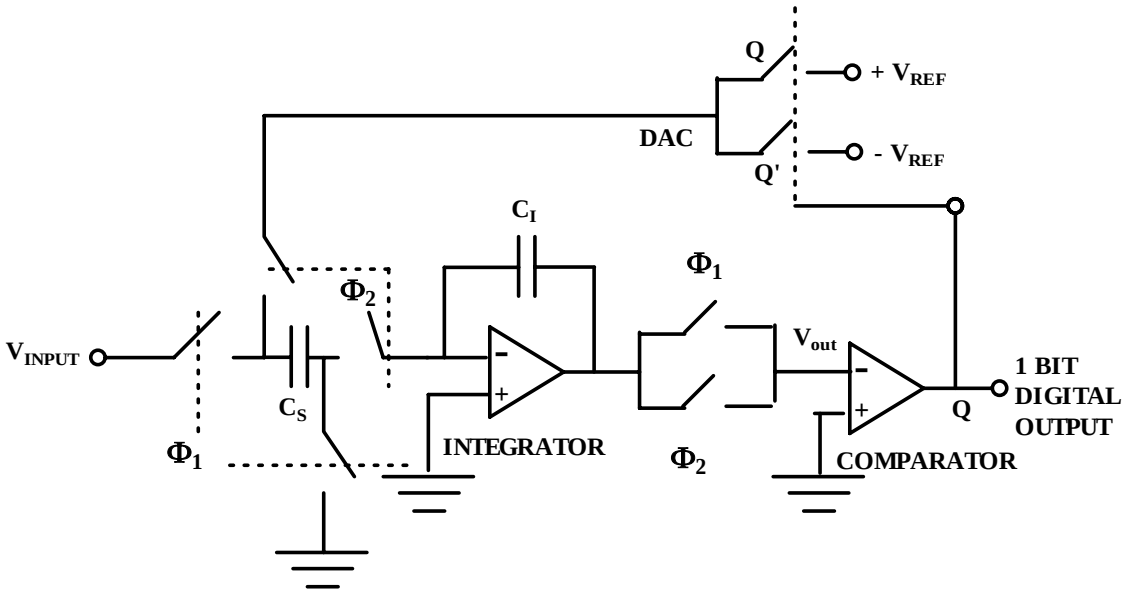
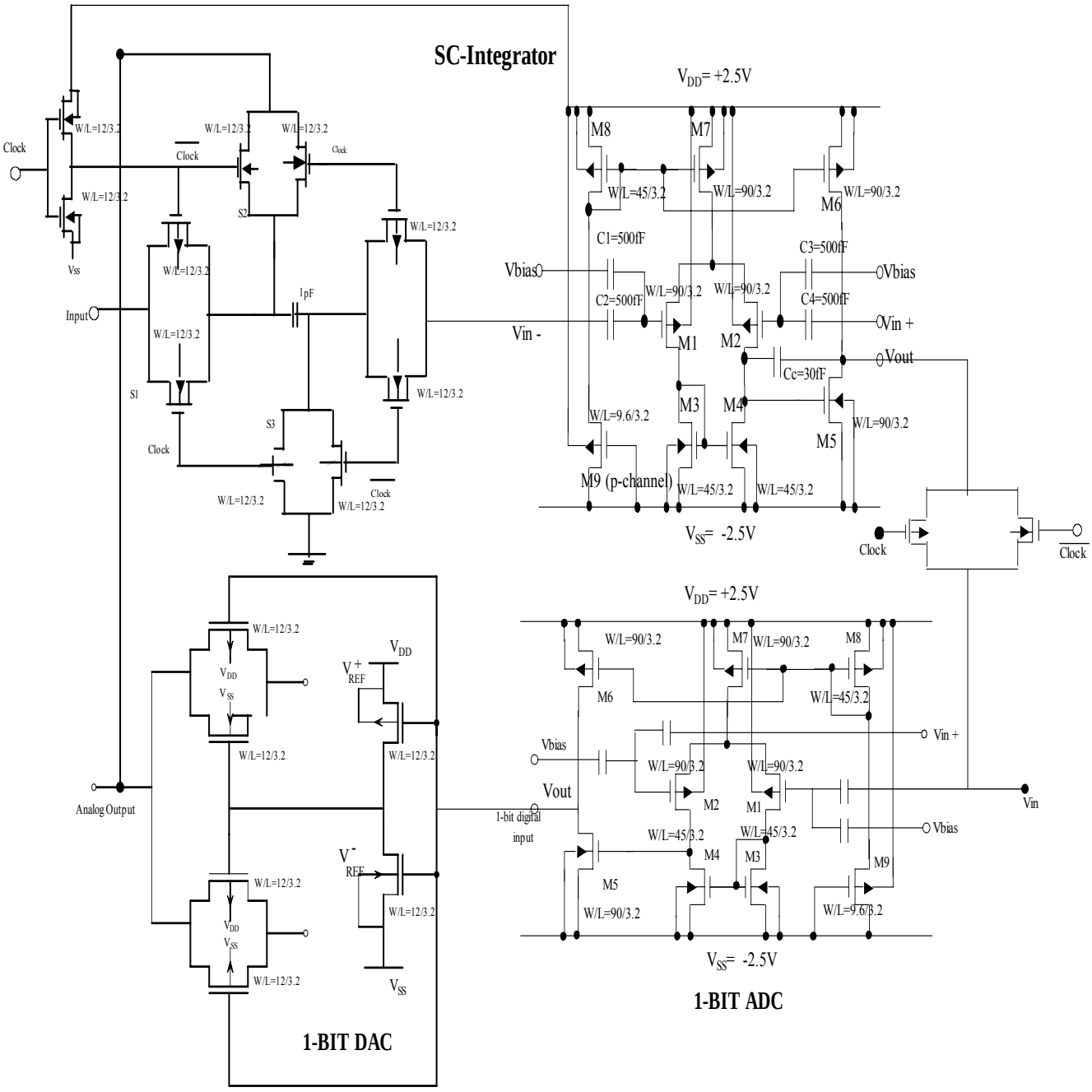



Figure 3.19: A complete first-order sigma-delta modulator.




Note: $V_{DD}$= +2.5V, $V_{SS}$= -2.5V unless otherwise not mentioned.

Figure 3.20: Circuit diagram of a first order modulator with floating gate MOSFETs.

# Chapter 4
# Theoretical and Experimental Results

This chapter discusses the measured theoretical and experimental results for the first order sigma delta modulator using floating gate transistors. The theoretical results are obtained from post-layout PSPICE (Cadence PSD 15.0, PSPICE A/D Simulator) simulations using SPICE level-3 MOS model parameters, which are summarized in Appendix A. The chip is designed using L-EDIT V.8.03 in standard 1.5 μm n-well CMOS technology. The first order modulator design is put in 40-pin pad frame, 2.25 mm × 2.25mm size and the fabricated chip (MOSIS T37C-BS) is tested using Tektronix TDS 3052 oscilloscope. The decimator is coded in Verilog and the design is transferred into an Altera Flex EPF10K70RC240 FPGA board. The decimator is interfaced with the modulator by hardwiring the chip with the FPGA board and the system is tested using an HP 1660CS logic analyzer. In the subsequent sections, theoretical results simulated from PSPICE and experimentally measured values will be presented and discussed.

Figure 4.1 shows the chip layout of a first order sigma delta modulator using floating gate transistors in standard 1.5 μm n-well CMOS process. Figure 4.2 shows the chip layout of the first order modulator within a pad frame of 2.25 mm × 2.25 mm size. Figure 4.3 shows the microphotograph of the fabricated modulator chip and Figure 4.4 shows the clear picture of modulator.

Figure 4.5 shows the SPICE simulated output from the modulator. The modulator is given a sine wave at a 1.5 kHz with peak-to-peak amplitude of 2 V. The clock input is a square wave at 700 kHz frequency and -2.5V to +2.5V amplitude. The power supply voltages are given as $V_{DD}$ (+2.5V) and $V_{SS}$ (-2.5V).

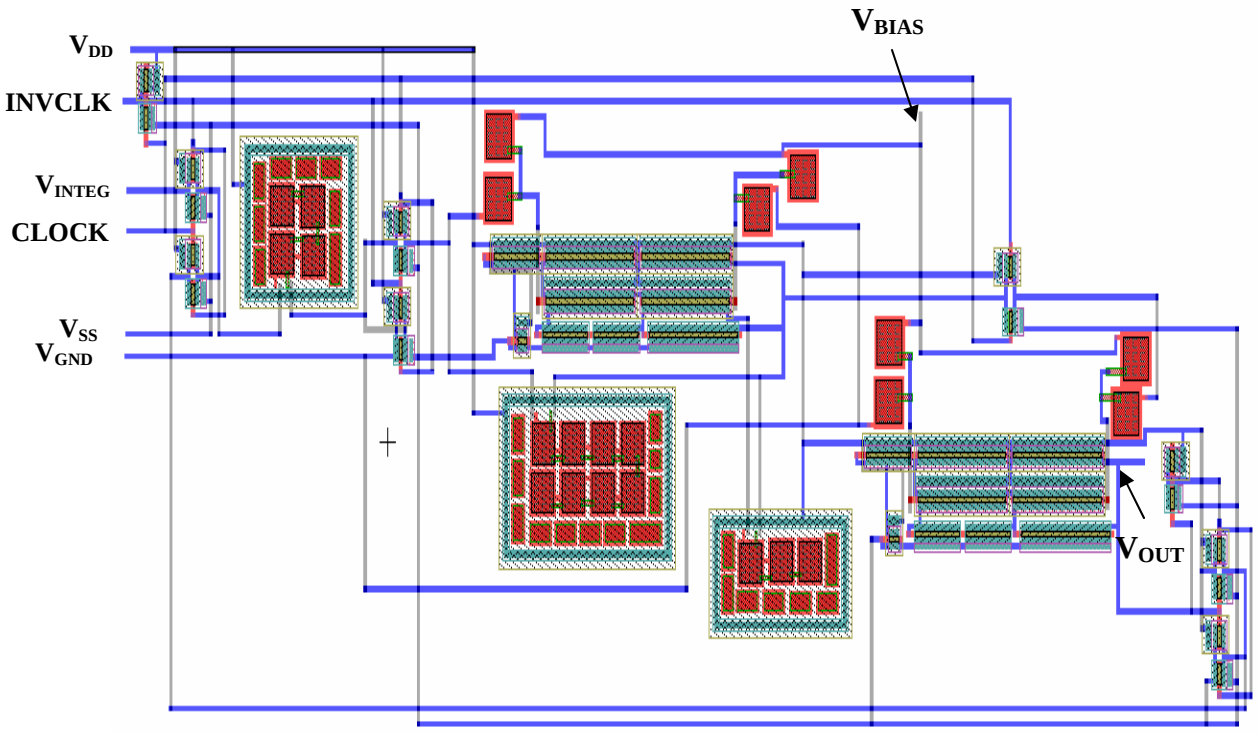



Figure 4.1: CMOS chip layout of a first order sigma delta modulator using floating gate transistors.

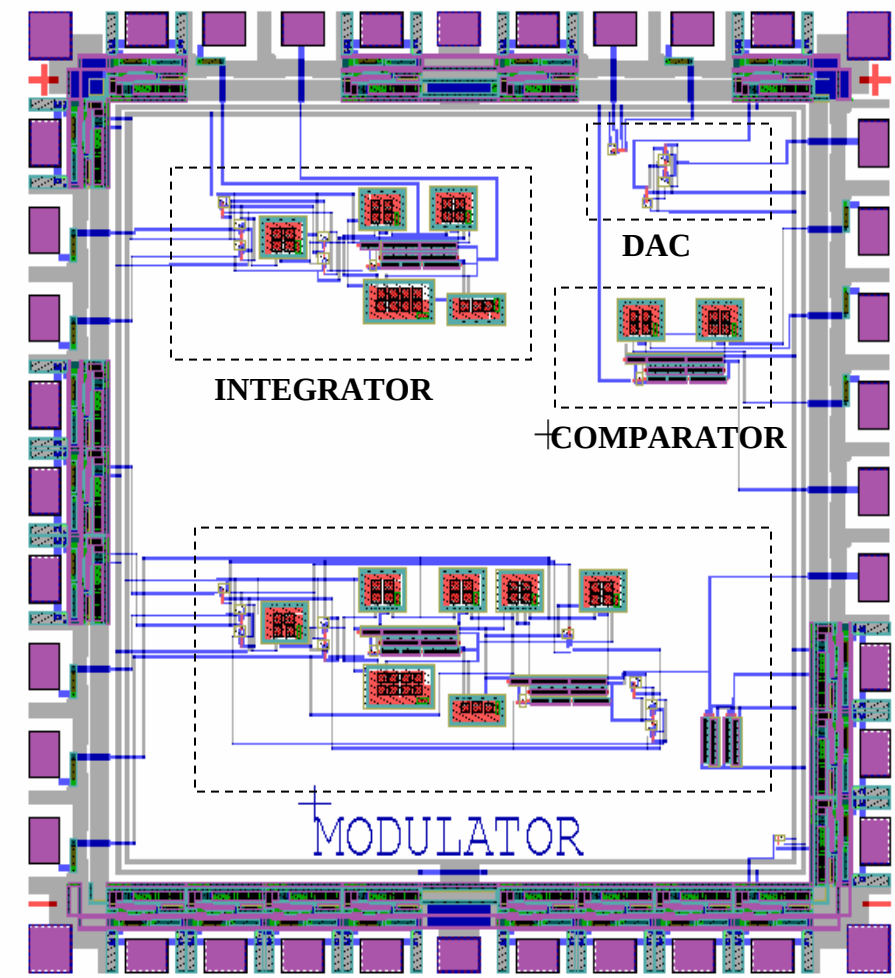



Figure 4.2: CMOS chip layout of a 1st order sigma delta modulator in a pad frame of 2.25 mm × 2.25 mm size.

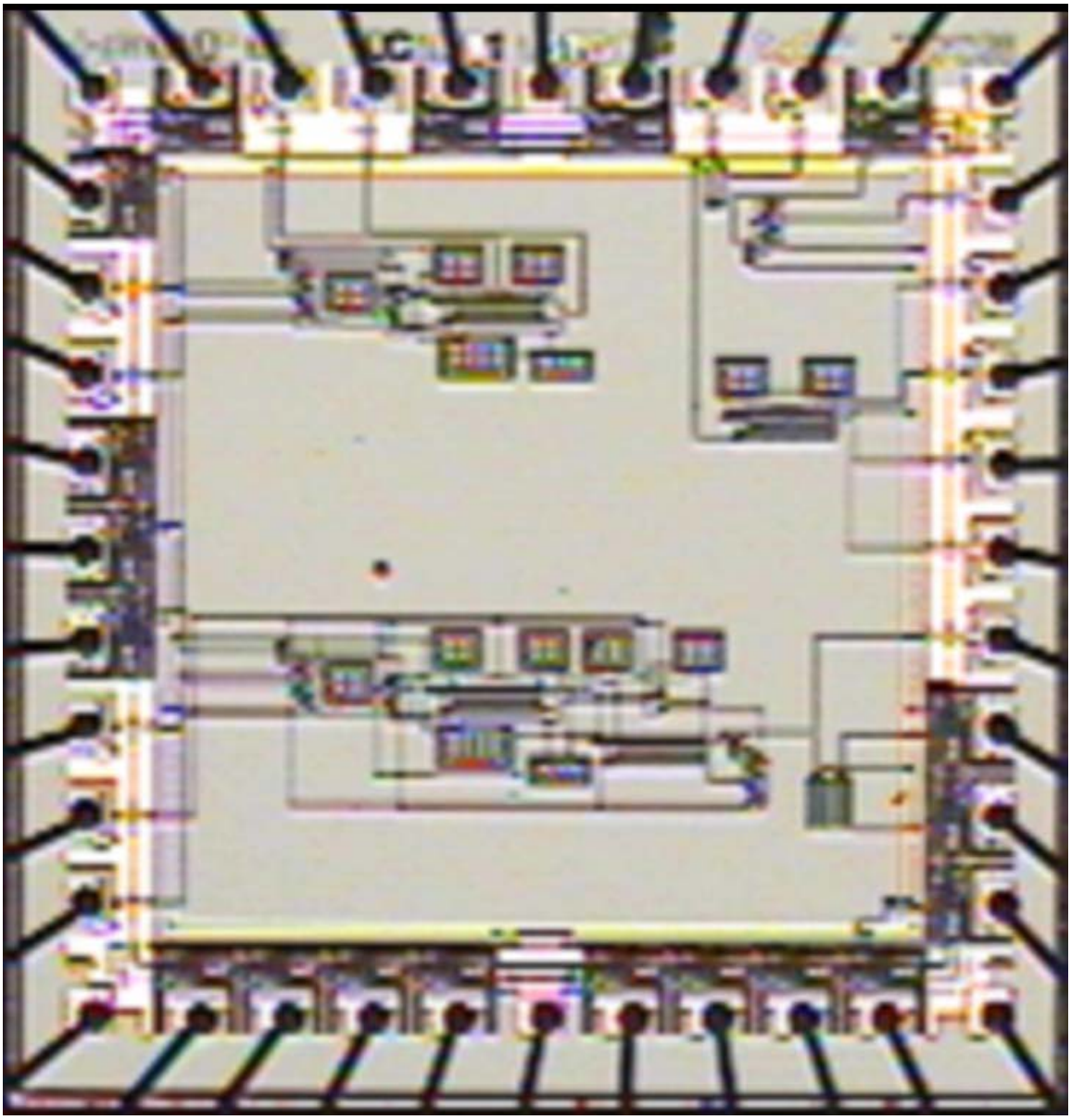


Figure 4.3: Microphotograph of the fabricated 1st order modulator chip.

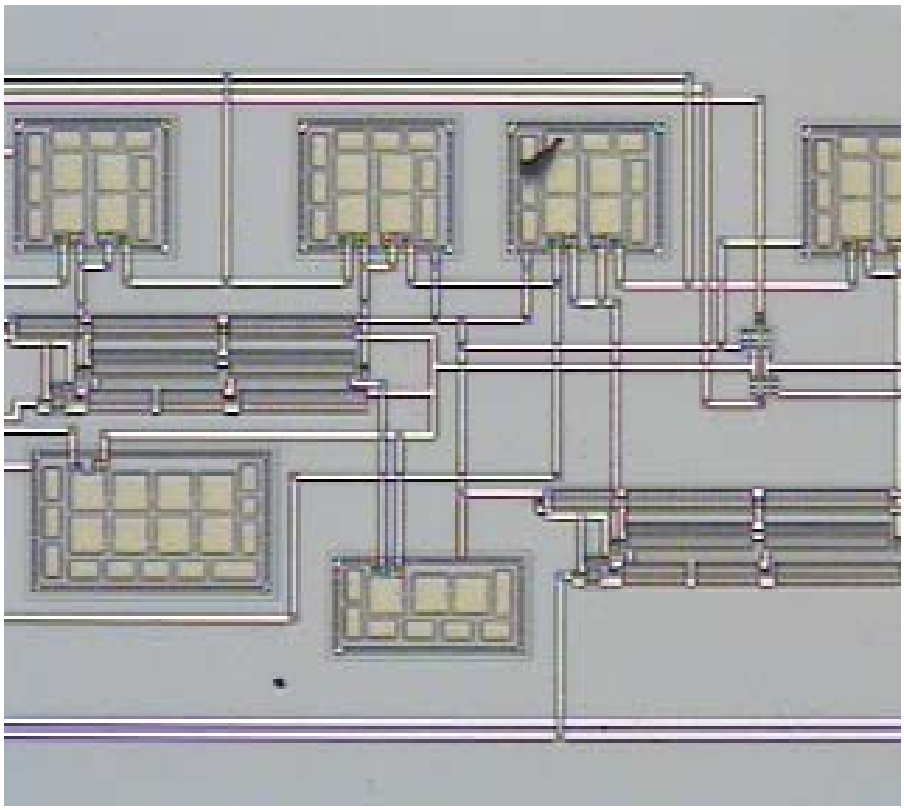


Figure 4.4: Microphotogrpah of the modulator part in fabricated chip.

The bias voltage ($V_{BIAS}$) shown in Fig. 4.1 is given as 2 V. The measured output of the sigma delta A/D converter using floating gate MOSFETs after the buffer is obtained as shown in the Figure 4.6.

The analog input given at the modulator input is sampled at rates higher than Nyquist rate (130 kHz). The output of the modulator is then passed through a filter to decimate the 1-bit output, which gives an 8-bit digital output. The decimator is designed in Verilog and tested with Altera Flex EPF10K70RC240 FPGA board. Figure 4.7(a), (b) and (c) show the output of the 8-bit sigma delta A/D converter after decimation. In Fig. 4.7 (a), the measured 8-bit digital output $(10110100)_2$, equivalent to $(180)_{10}$, from an integrated sigma-delta ADC system corresponding to a 1 V analog input is shown. Similarly, the measured 8-bit digital outputs $(11011001)_2$ and $(00101011)_2$ , equivalent to $(217)_{10}$ and $(39)_{10}$ from an integrated sigma-delta ADC system corresponding to 1.7 V and -1.7 V analog inputs are shown in Figs. 4.7 (b) and (c) respectively. The results are tabulated in Table 4.1.

As we discussed earlier in Chapter 3, the sigma delta ADC consists of two parts, an analog sigma delta modulator, which gives a 1-bit digital output, and a low-pass digital decimation filter, which resolves the 1-bit digital output from a modulator into an 8-bit digital output. The block diagram of a modulator shown in chapter 3, consists of a SC- integrator, a comparator, which acts as an ADC and 1-bit DAC, which is placed in the feedback loop. The integrator, comparator and the 1 bit D/A converter shown in Figure 4.1 are tested individually and the results are followed. The 1-bit digital output at the modulator has high frequency content with analog signal as its mean value.

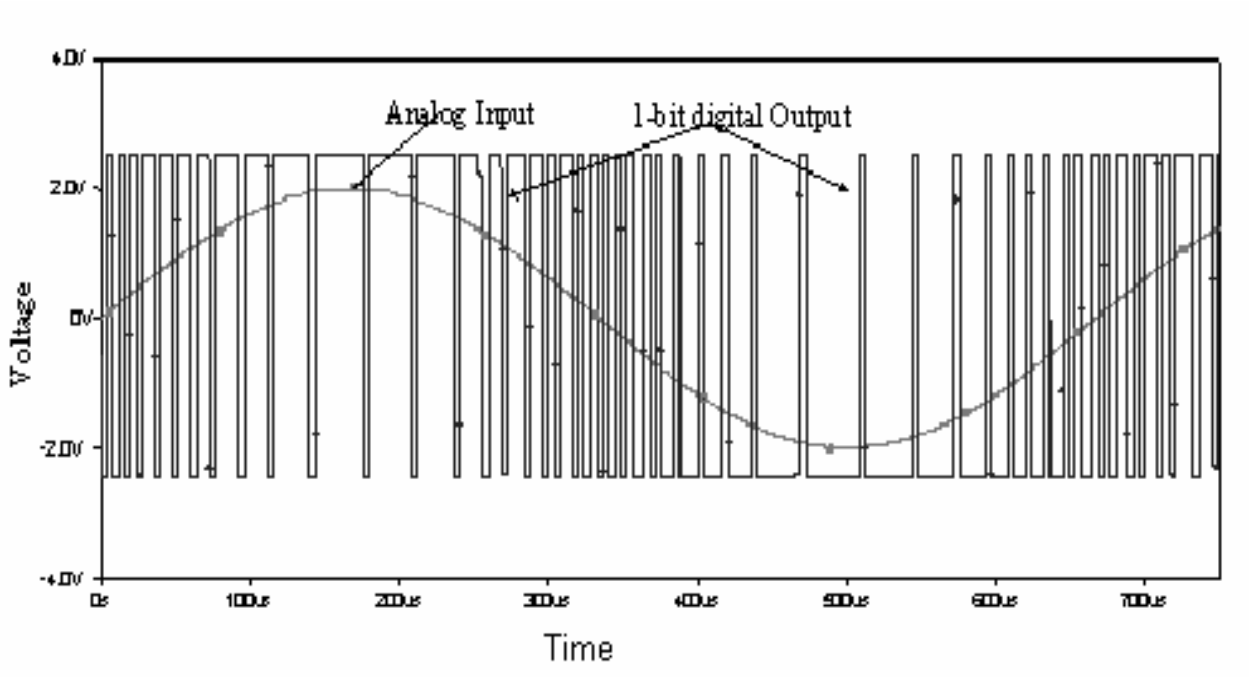



Figure 4.5: SPICE simulation results of a 1-bit modulator (ADC).

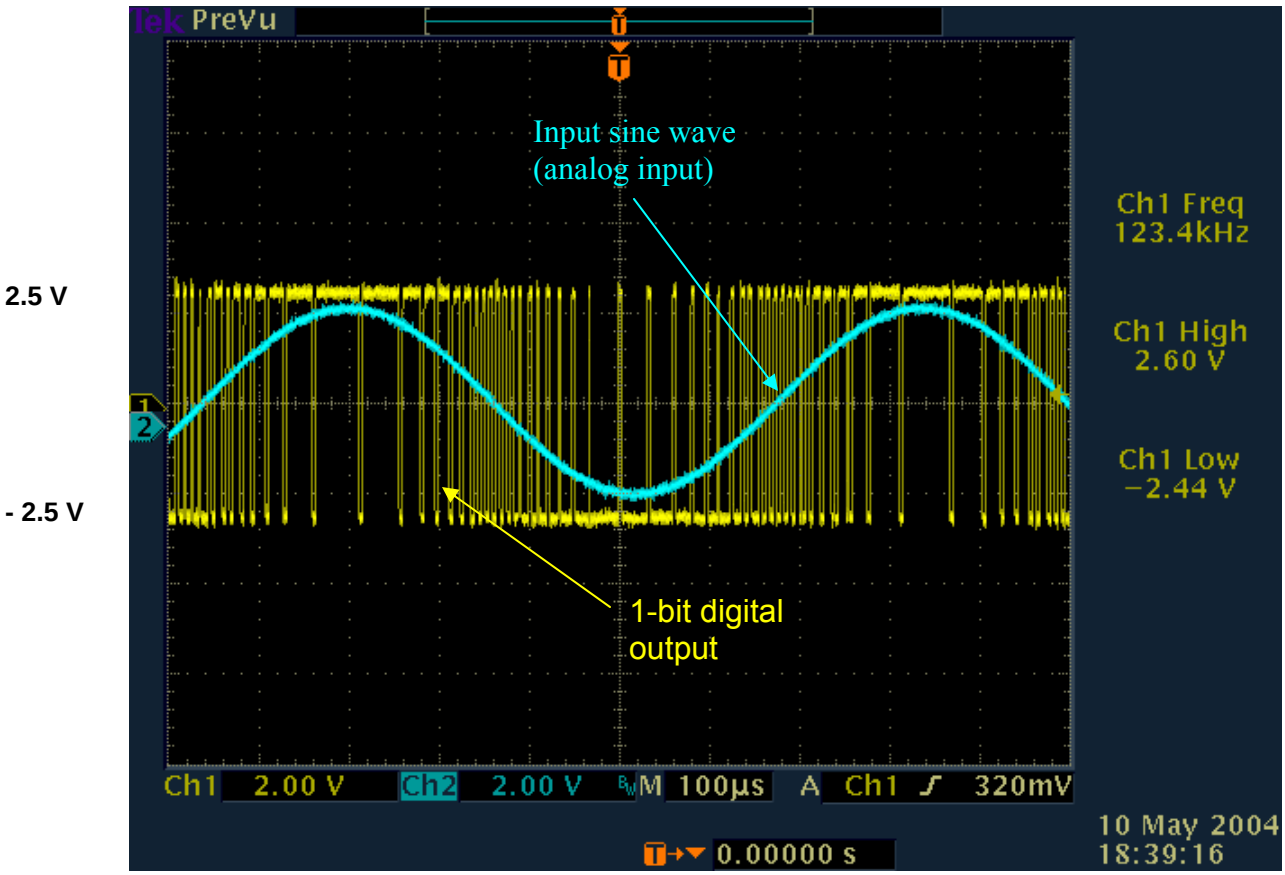



Figure 4.6: Measured 1-bit digital output from the fabricated chip.

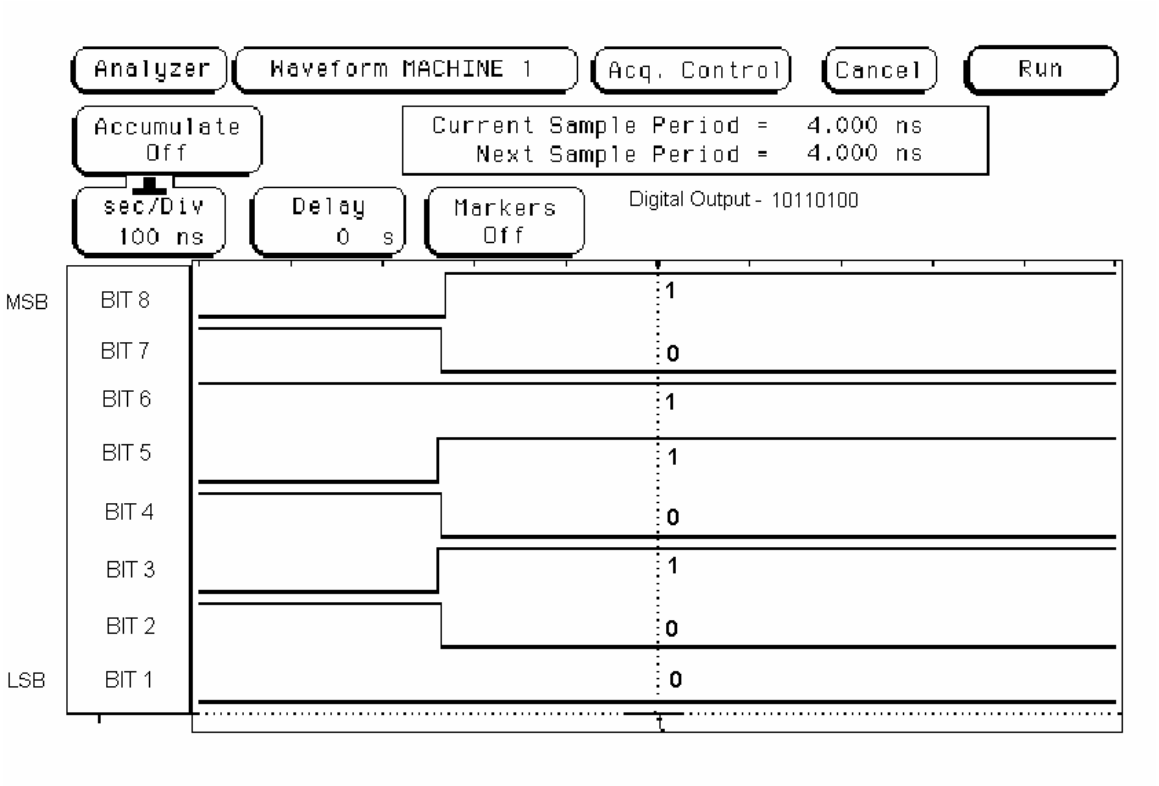



Figure 4.7 (a): Measured digital output $(10110100)_2 \equiv$ 1.0156 V of an integrated 8-bit sigma-delta ADC for an anlaog input of 1 V.

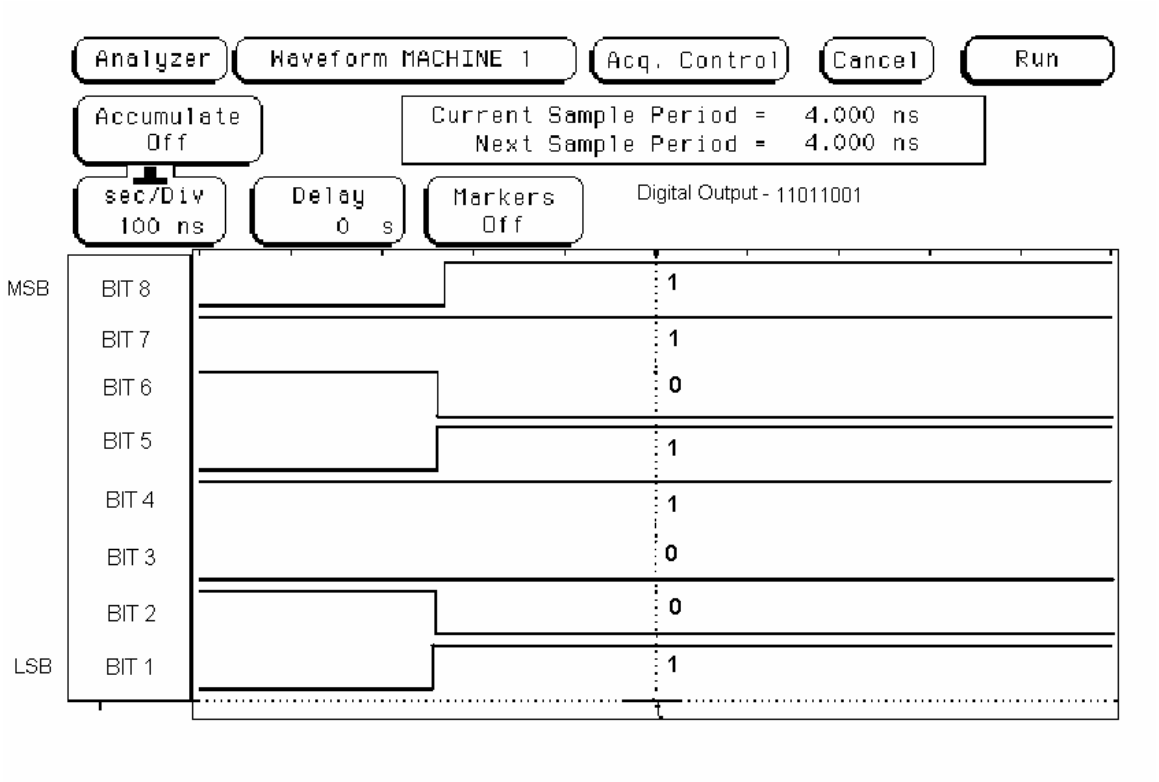



Figure 4.7 (b): Measured digital output $(11011001)_2 \equiv$ 1.7382 V of an integrated 8-bit sigma-delta ADC for an anlaog input of 1.7 V.

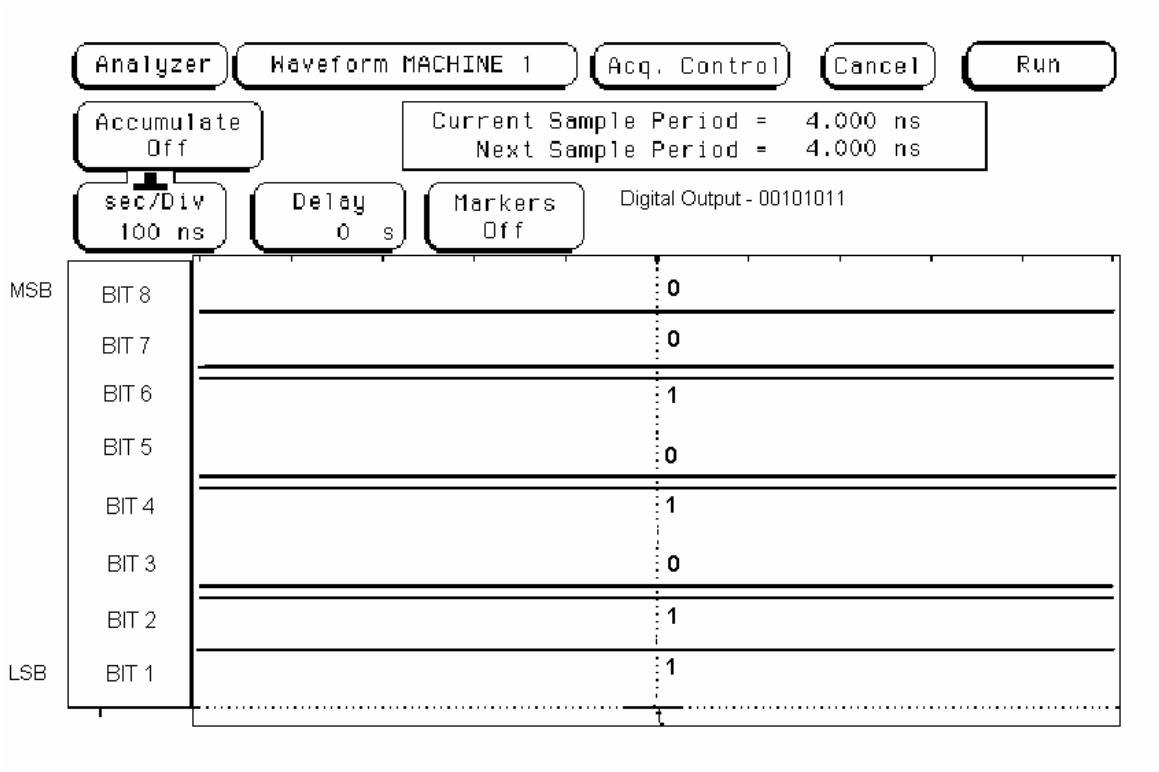



Figure 4.7 (c): Measured digital output $(00101011)_2 \equiv$ -1.7382 V of an integrated 8-bit sigma-delta ADC for an analog input of -1.7 V.

Table 4.1: Input and measured output from the designed ADC

| **Input, V** | **Measured Digital Output** | **Analog Value (equivalent), V** |
|---|---|---|
| 1 | 10110100 | 1.0156 |
| 1.4 | 11001000 | 1.4062 |
| -1.4 | 00111000 | -1.4062 |
| 1.7 | 11011001 | 1.7382 |
| -1.7 | 00101011 | -1.7382 |

The integrator is designed using the switched capacitor technique where the op-amp inputs are floating gate MOSFETs. The layout of integrator is shown in the Fig. 4.8 and the post layout simulated output characteristics are shown in Fig. 4.9.

The comparator is also designed as a two-stage CMOS operational amplifier, which gives a 1-bit digital input to the DAC. The layout for the comparator is shown in Figure 4.10. The post layout simulated output characteristics of the comparator are shown in Fig. 4.11. Figure 4.12 shows the observed output characteristics of the comparator. Figure 4.13 shows the layout of DAC. Similarly, Fig. 4.14 depicts the output characteristics of DAC. Figure 4.15 shows the measured output characteristics of DAC.

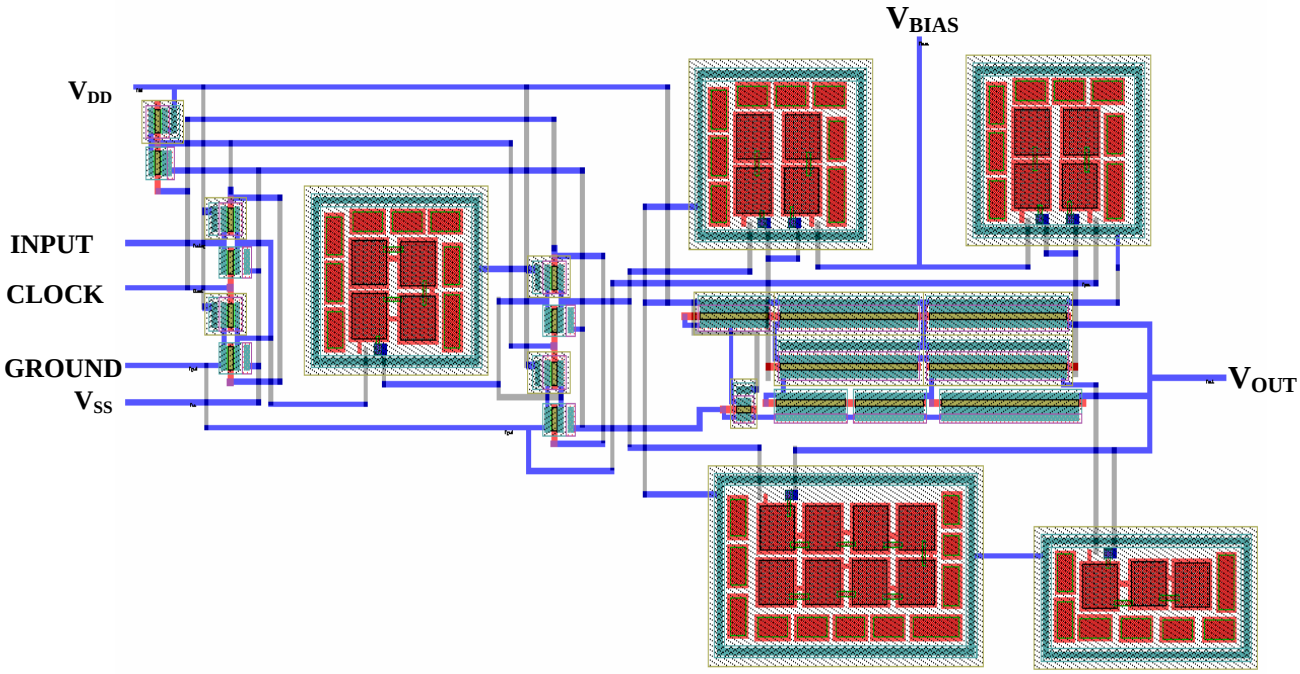



Figure 4.8: The layout for sc-integrator.

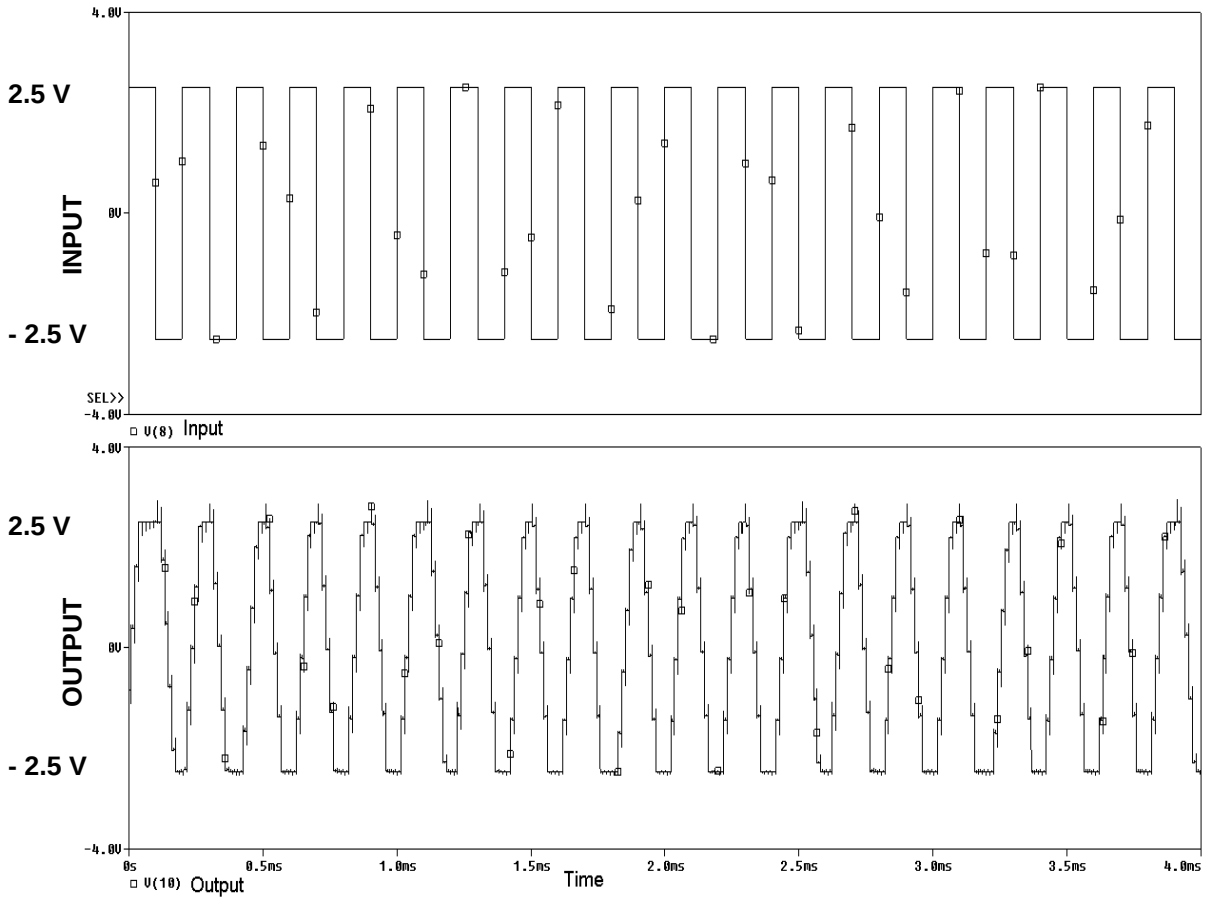



Figure 4.9: The output characteristics of post layout simulation of the integrator of Fig. 4.8.

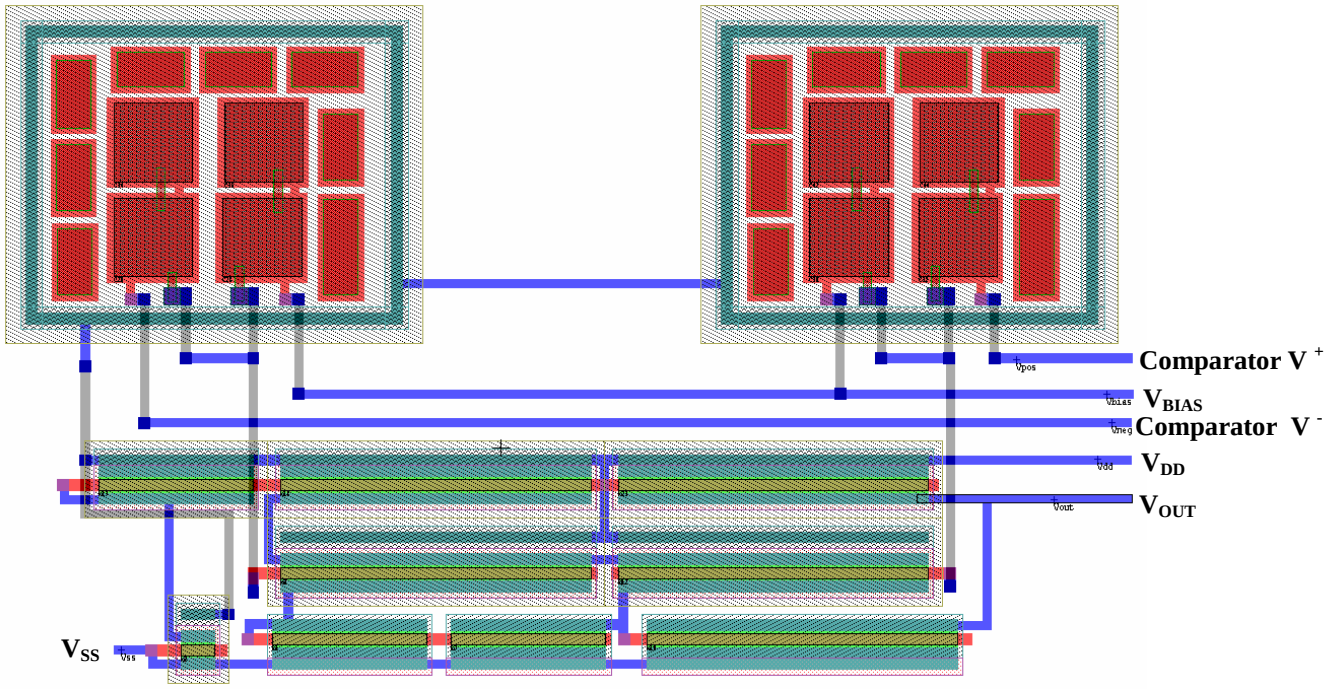



Figure 4.10: The layout for comparator using floating gate transistors.

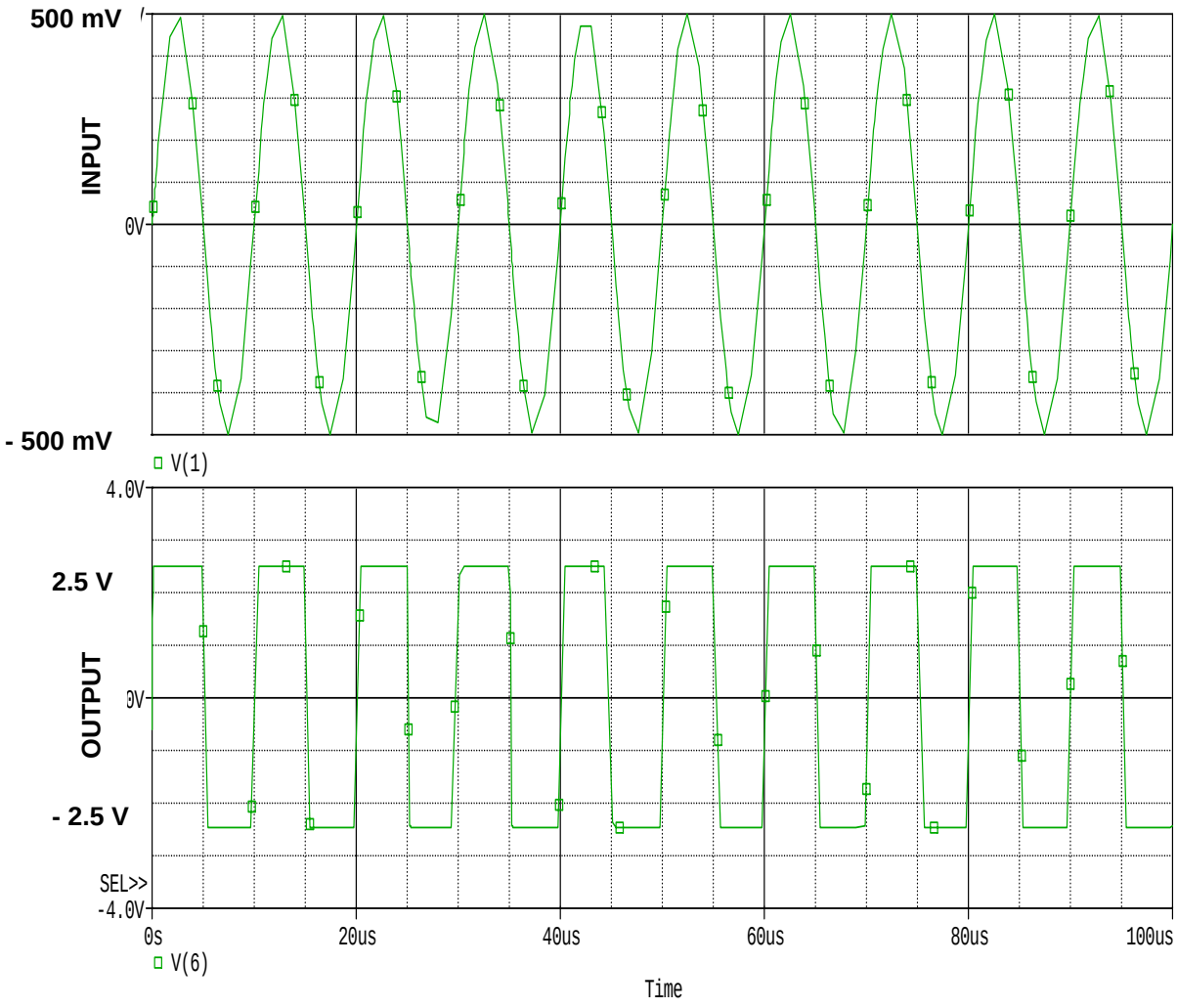



Figure 4.11: Post layout simulation output characteristics of the comparator of Fig. 4.10.

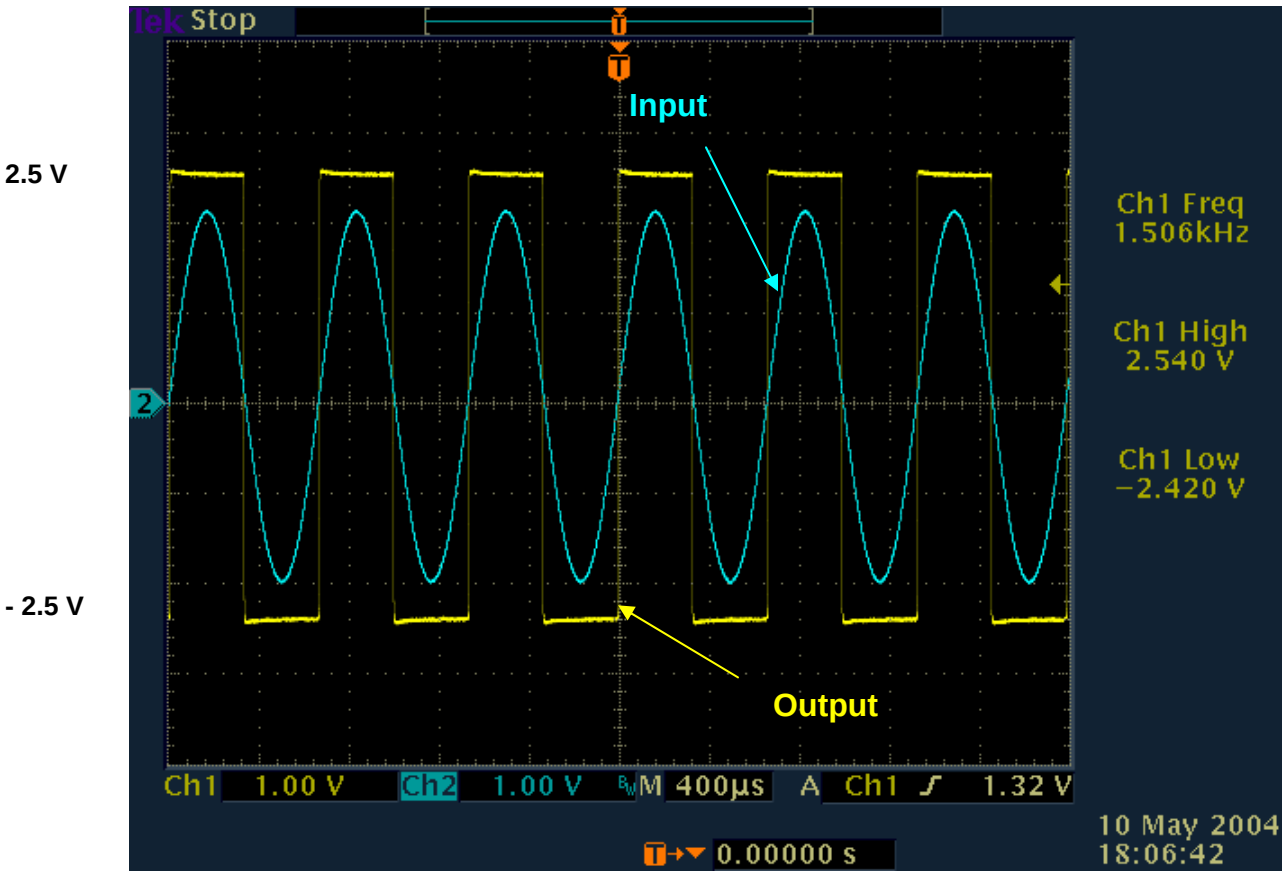



Figure 4.12: Measured output characteristics of comparator of Fig. 4.10.

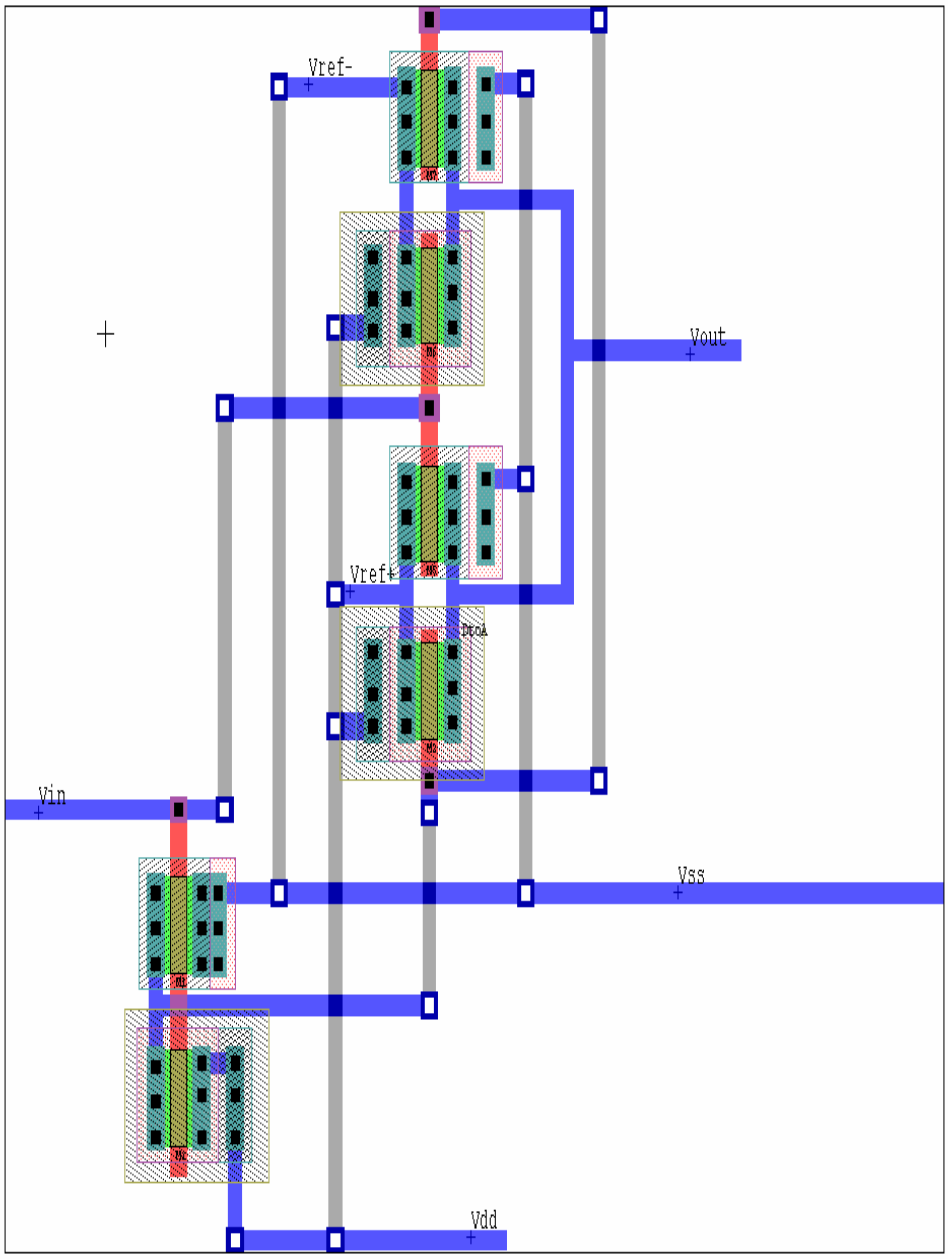



Figure 4.13: Layout of DAC.

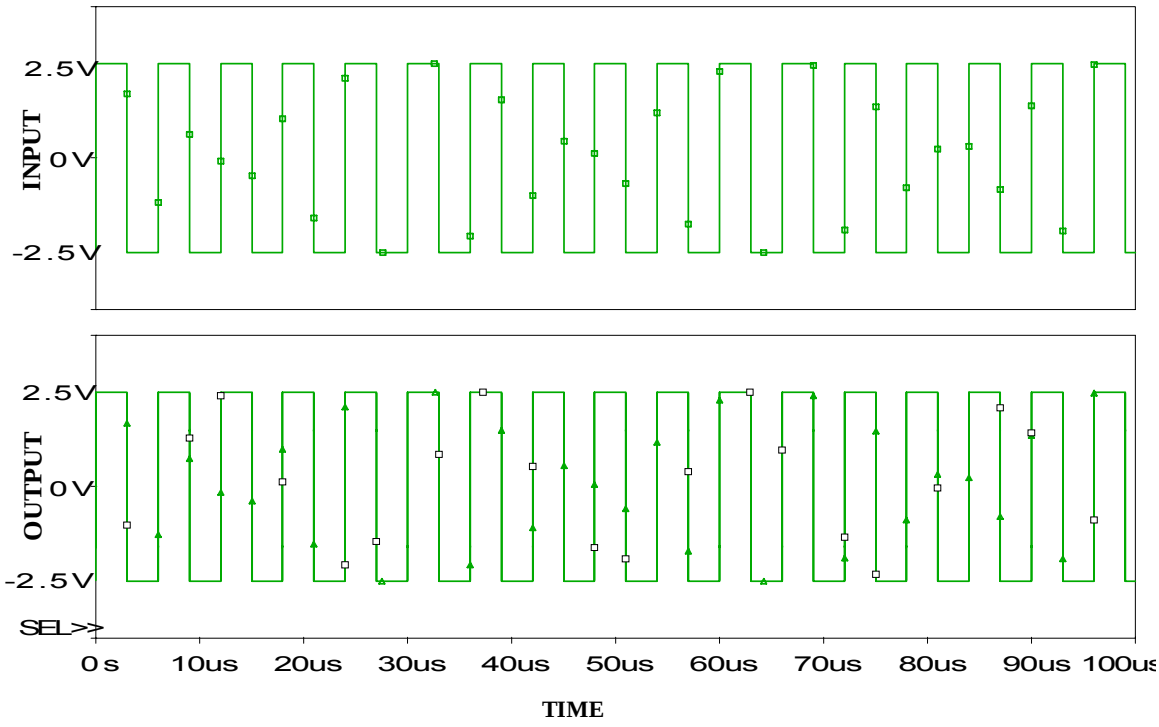



Figure 4.14: The post layout simulated output characteristics of DAC of Fig. 4.13.

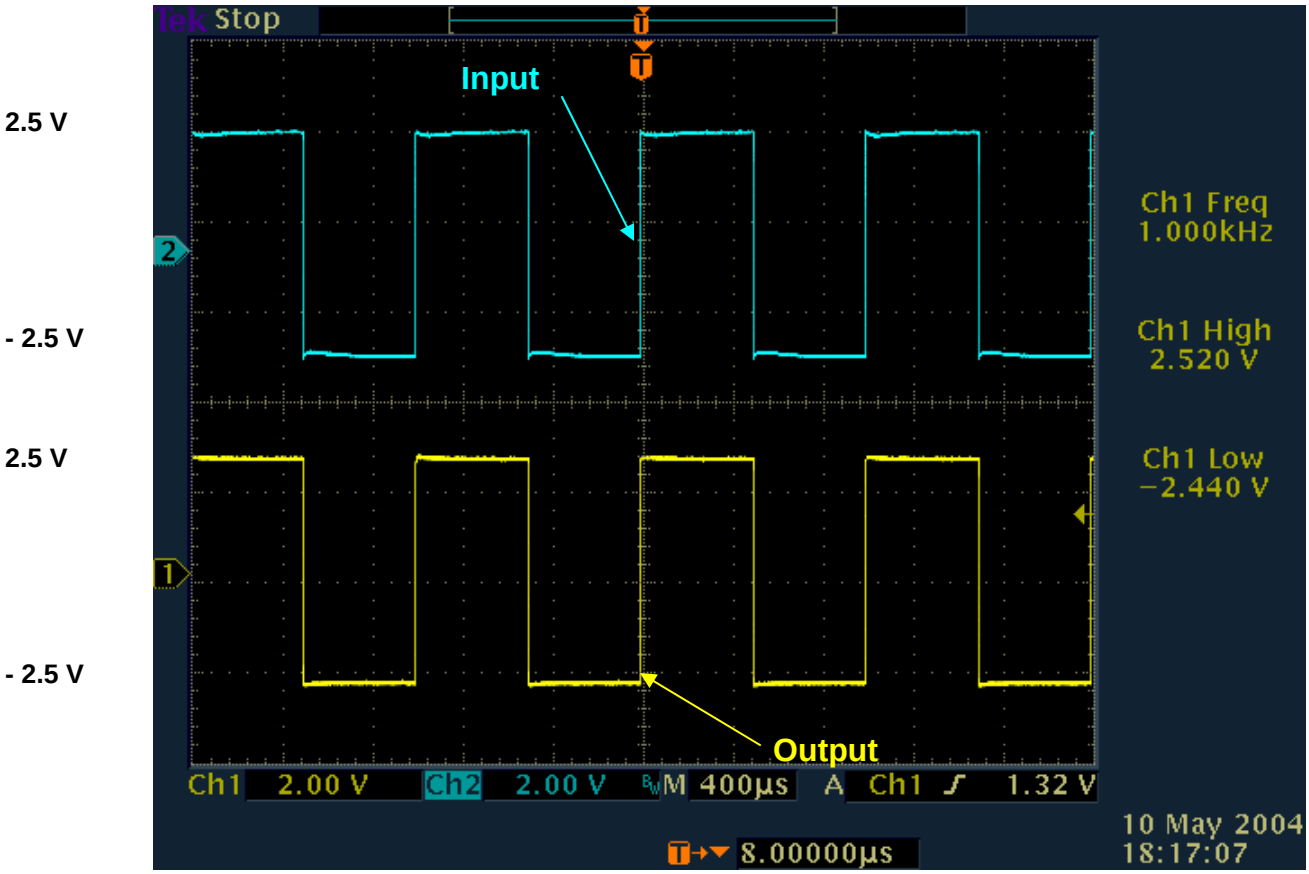



Figure 4.15: Measured output characteristics of DAC of Fig. 4.13.

# Chapter 5
# Conclusion

An 8-bit sigma-delta analog-to digital converter system has been designed and tested which uses first order modulator design in floating gate MOSFETs in standard 1.5 μm n-well CMOS process and an off-chip filter. The principle of MIFG transistor, calculating weighted sum of all inputs at gate level and switching transistor ON or OFF depending upon calculated voltage greater than or less than switching threshold voltage is utilized. A simple equivalent electrical simulation circuit is employed to avoid the convergence problems while using floating gate devices.

In present work, the circuits are simulated in SPICE with MOSIS Level-3 MOS model parameters. The physical layout for the circuits is drawn using L- EDIT V 8.3. The post layout simulations included interlayer and parasitic nodal capacitance to make the simulation more realistic. The modulator uses floating gate MOSFETs for low-voltage signal processing, which are compatible with a standard CMOS process. The ADC operates at a sampling clock frequency of 8 MHz. The ADC gives an 8-bit resolution with a 65 kHz bandwidth. It can be used with increased bandwidth up to 1 MHz for applications, such as for speech and audio signal processing. At present, ADC is demonstrated at five different data sample points for the corresponding analog inputs.

Decimator could be designed using MIFG transistors in CMOS process for low-power and integrated on-chip with the modulator for improved performance.

# References


[1] T. Shibata and T. Ohmi, "A Functional MOS transistor featuring gate-level weighted sum and threshold operations," *IEEE Trans. on Electron Devices*, Vol. 39, no. 6, pp. 1444-1455, June 1992.

[2] S. Rusu, "Trends and challenges in VLSI technology scaling towards 100 nm," *Proc. of 27th Euro. Solid-State Circuits Conf*., Sep. 2001.

[3] T. Shibata and T. Ohmi, "An intelligent MOS transistor featuring gate-level weighted sum and threshold operations," *IEDM Tech. Dig*, pp. 919-922, 1991.

[4] P. Hasler, B. A. Minch and C. Diorio, "Floating gate devices: they are not just for digital memories anymore," *Proc. IEEE International Symposium on Circuits and Systems,* Vol. 2, pp. 388-391, 1999.

[5] A. N. Mohieldin, A. Emira and E. Sanchez-Sinencio, "A 2V 11-bit incremental A/D converter using floating gate technique," *Proc. IEEE International Symposium on Circuits and Systems*, Vol. 4, pp. 667-670, May 2002.

[6] D. U. Thompson and B. A. Wooley, "A 15-b pipelined CMOS floating point A/D converter," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 2, pp. 299-303, February 2001.

[7] L. Yin, S.H.K. Embabi, E. Sanchez-Sinencio, "A floating gate MOSFET D/A converter," *Proc. IEEE International Symposium on Circuits and Systems,* pp. 409-412, June 1997.

[8] J. Ramirez-Angulo, R.G. Carvajal, J. Tombs and A. Torralba, "A low-voltage CMOS op-amp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple input floating gate transistors," *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 48, No. 1, pp. 111-116, Jan. 2001.

[9] J.J. Chen, S. Iuan and Y.S. Hwang, "Low-voltage single power supply four quadrant multiplier using floating gate MOSFETs," *Proc.* of *IEEE International Symposium on Circuits and Systems*, pp. 237-240, June 9-12, 1997.

[10] R.J. Baker, H.W. Li, D.E. Boyce, *CMOS Circuit Design Layout and Simulation*, Chapter 29, IEEE Press, 1998.

[11] K. M. Daugherty, *Analog-to-Digital Conversion: A Practical Approach*, Mc Graw-Hill, 1995.

[12] D.F. Hoeschele, *Analog-to-Digital and Digital-to-Analog Conversion Techniques*, John Wiley & Sons, 1994.

[13] J. C. Candy, "Decimation for sigma delta modulation," *IEEE Transactions on Communications*, Vol. COM-34, No.1, January 1986.

[14] E. R. Ruotsalainen, K. Lasanen and J. Kostamovaara, "A 1.2 V micropower CMOS op-amp with floating-gate input transistors," *Proc. of 43rd Midwest Symp. on Circuits and Systems*, Vol. 2, pp. 794-797, Aug. 2000.

[15] K. Nandhasri and J. Ngarmnil, "Hysteresis tunable voltage comparator using floating gate MOSFET," *IEEE International Conference on Semiconductor Electronics*, pp-709-712, Nov. 2000.

[16] J. R. Angulo, S.C. Choi and G.G. Altamirano, "Low-voltage circuits building blocks using multiple-input floating gate transistors," *IEEE Transactions on Circuits and Systems*, Vol. 42, No. 11, pp. 971-974, Nov. 1995.

[17] P. M. Furth and H. A. Ommani, "A 500-nW floating-gate amplifier with programmable gain," *Proc. of the 41st IEEE 1998 Midwest Symposium on Circuits and Systems*, August 1998.

[18] M. Keskin, Un-Ku Moon and G. C. Temes, "A 1-V, 10-MHz clock rate, 13-bit CMOS $\Delta\sum$ modulator using unity gain reset op-amps," *Proc. of 27th Euro. Solid-State Circuits Conf*., pp. 532-535, Sep. 2001.

[19] K. Bacrania, "A 12-bit successive-approximation-type ADC with digital error correction," *IEEE J. of Solid State Circuits*, Vol. SC-21, pp. 1016-1025, Dec. 1986.

[20] M. J. M Pelgrom, A.C.J.V. Rens, M.Vertregt, M.B. Dijkstra, "A 25-Ms/s 8-bit CMOS A/D converter for embedded application," *IEEE J. of Solid State Circuits*, Vol. 29, pp. 879-886, Aug. 1994.

[21] D. Choi, R. Pierson, F. Trafton, B. Sheahan, V. Gopinathan, G. Mayfield, I. Ranmuthu, S. Venkatraman, V. Pawar, O. Lee, W. Giolma, W. Krenik, W. Abbott, K. Johnson, " An analog front-end signal processor for a 64 Mbits/s PRML hard-disk drive channel," *IEEE J. of Solid State Circuits*, Vol. 29, pp. 1596-1605, Dec. 1994.

[22] T. Shibata and T. Ohmi, "Neuron MOS binary-logic integrated circuits-part I: design of fundamentals and soft hardware logic circuit implementation," *IEEE Trans. on Electron Devices*, Vol. 40, No. 3, pp. 570-576, March 1993.

[23] W. Weber, S. J. Prange, R. Thewes, K. Goser, A. Luck, "On the design robustness of threshold logic gates using multi-input floating gate MOS transistors," *IEEE Trans. on Electron Devices*, Vol. 47, pp. 1231-1239, June 2000.

[24] H. N. Venkata, *Ternary and Quaternary Logic to Binary Bit Conversion CMOS Integrated Circuit Design Using Multiple Input Floating Gate MOSFETs*, M.S. (EE) thesis, ECE Department, Louisiana State University, Baton Rouge, Dec. 2002.

[25] http://www.mosis.org

[26] J. Ramirez-Angulo, G. Gonzalez-Altamirano and S.C. Choi, "Modeling multiple input floating gate transistors for analog signal processing," *Proc.* of *IEEE International Symposium on Circuits and Systems*, pp. 2020-2023, June 9-12, 1997.

[27] E. Rodriguez-Villegas, G. Huertas, M. J. Avedillo, J. M. Quintana and A. Rueda, "A practical floating-gate Muller-C element using vMOS threshold gates," *IEEE Trans. on Circuits and Sytems-II: Analog and Digital Signal Processing*, Vol. 48, pp. 102-106, Jan. 2001.

[28] S. Hein and A. Zakhor, *Sigma Delta Modulators: Nonlinear Decoding Algorithms and stability analysis*, Kluwer Academic Publishers, 1993.

[29] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd edition, Oxford University Press, 2002.

[30] B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.

[31] F. Wang and R. Harjani, *Design of Modulators for Oversampling Converters*, Kluwer Academic Publishers, 1998.

[32] M. S. Roden, Analog and Digital Communication Systems, Prentice-Hall, 1979.

[33] K. S. Shanmugam, Digital and Analog Communication Systems, John Wiley and Sons, 1998.

[34] http://www.analog.com/library/analogDialogue/archives/33-08/adc

[35] R. J. Baker, *CMOS Mixed-Signal Circuit Design*, Volume 2, IEEE Press, 2003.

[36] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th edition, John Wiley & Sons, 2001.

[37] P. R. Gray and R.G. Meyer, "MOS operational amplifier design - a tutorial overview," *IEEE J. of Solid State Circuits*, vol. SC-17, pp. 969-982, Dec. 1982.

[38] Bradley A. Minch, "A folded floating gate differential pair for low voltage applications," *Proc. IEEE International Symposium on Circuits and Systems*, pp. 253-256, May 28-31, 2000.

# Appendix A
# Spice Parameters from [25]

```
* LOT: T37C                WAF: 3102
* DIE: N_Area_Fring        DEV: N3740/10
* Temp= 27
.MODEL CMOSN NMOS (LEVEL = 3
+ TOX    = 3.08E-8        NSUB   = 1.303524E15     GAMMA = 0.6890085
+ PHI    = 0.7            VTO    = 0.5766549           DELTA = 0.52441805
+ UO     = 605.3654969    ETA    = 1.523702E-3     THETA = 0.071321
+ KP     = 7.248459E-5    VMAX   = 2.270476E5      KAPPA = 0.5
+ RSH    = 0.1212666      NFS    = 5.41104E11      TPG    = 1
+ XJ     = 3E-7           LD     = 0               WD     = 6.807121E-7
+ CGDO   = 1.8E-10        CGSO   = 1.8E-10         CGBO   = 1E-10
+ CJ     = 2.674036E-4    PB     = 0.8             MJ     = 0.5
+ CJSW   = 1.411187E-10    MJSW   = 0.099261)
*
*

* LOT: T37C                WAF: 3102
* DIE: P_Area_Fring        DEV: P3740/10
* Temp= 27
.MODEL CMOSP PMOS (LEVEL = 3
+ TOX    = 3.08E-8        NSUB   = 1E17            GAMMA = 0.4813547
+ PHI    = 0.7            VTO    = -0.8943843      DELTA = 0.3978203
+ UO     = 100            ETA    = 1.283013E-5     THETA = 0.1291997
+ KP     = 2.430938E-5    VMAX   = 3.416068E5      KAPPA = 150
+ RSH    = 37.9153971     NFS    = 4.463283E11     TPG    = -1
+ XJ     = 2E-7           LD     = 1E-14           WD     = 9.9685E-7
+ CGDO   = 2.22E-10       CGSO   = 2.22E-10        CGBO   = 1E-10
+ CJ     = 3.008377E-4    PB     = 0.8             MJ     = 0.4380042
+ CJSW   = 1.489724E-10    MJSW   = 0.0849831)
*
```

# Appendix B
# Simulating Floating Gate MOS Transistor

Besides the theoretical background for the realization of transmission gates with floating gate MOSFETs, one practical design to be considered is electrical simulation. In the design phase of devices using floating-gate transistors, electrical simulations for validation must be performed. Other difficulty in simulating floating gate devices is the inability of the simulator to converge when floating nodes exists. Since manufactures do not provide models for floating gate devices, techniques to simulate floating gate devices using standard MOS models must be devised. Few approaches for this problem are given in references [7, 6, 15 and 20]. They use an additional network formed by resistors and voltage controlled voltage sources (VCVSs) to establish the initial floating-gate voltage value. But the main problem of these approaches is that an operation point is previously determined to fix the value of the voltages at the VCVS control terminals.

Villegas et. al., [27], suggests initializing all the input voltage sources to zero, before running the simulation, which would allow setting an appropriate operating point when using floating gate devices. The equivalent circuit of a MIFG inverter when used for electrical simulation is given in Fig. B.1. When the circuit is simulated in SPICE it fails to converge at floating gate. Hence a large resistance in the range of $10^{12}$ Ω was placed from floating gate to ground as shown in Fig. B.2. The resistor gives an initial voltage on floating gate as well as an effect of open circuit from floating gate to ground.

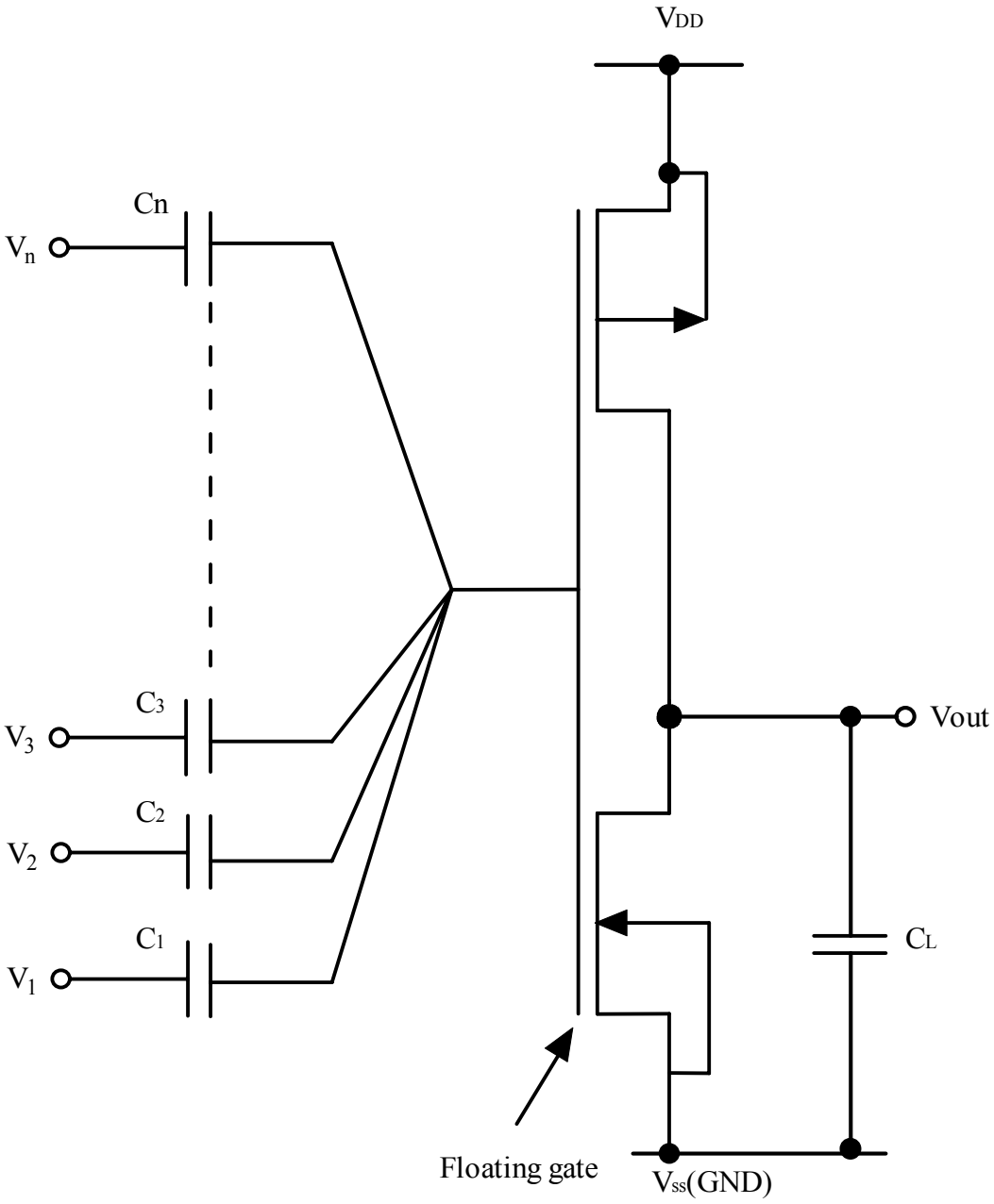



Figure B.1: Equivalent circuit of a multi-input floating-gate inverter for electrical simulations.

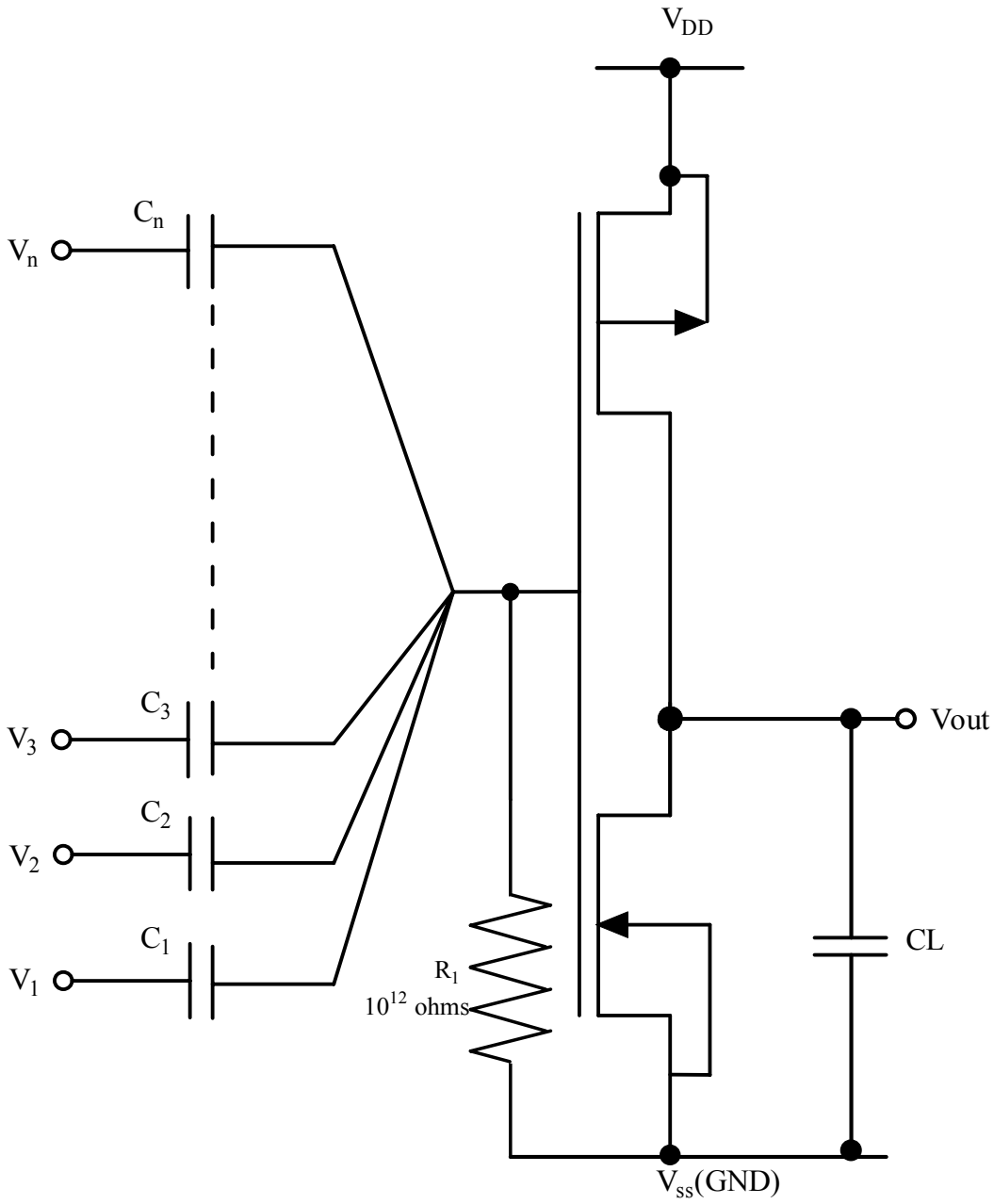



Figure B.2: Resistor added to equivalent circuit for simulation purposes.

When capacitor $C_1$ is used with DC voltage source as input to the capacitance, the simulator recognizes it as a DC storage capacitor, instead of a AC coupling capacitance and blocks the voltage. The DC voltage source is replaced with a piece-wise-linear voltage source by using which the simulator simulates the capacitor as a coupling capacitance. Taken the above considerations for simulating circuits having floating gate devices, the experimental results of circuits failed when MIFG inverters were cascaded. The circuits are simulated in SPICE with MOSIS level-3 MOS model parameters.

# Appendix C
# Decimator Implementation

The decimator is implemented in Verilog and was downloaded on to an Altera Max FPGA board (FLEXE20k FPGA). While interfacing the modulator with the decimator, we need to shift the logic levels of the modulator to the logic levels corresponding to Altera's board. This is due to the reason that Altera board has the logic low as 0V and the logic high as 5V. The modulator has logic high of +2.5V and a logic low of -2.5V. Therefore, is used in between the modulator and the decimator as shown in Fig. C.1. A simple buffer made-up of nand gate was used.

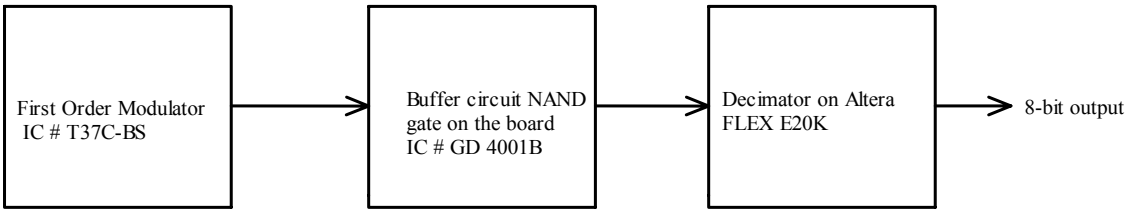



Figure C.1: Experimental set-up for the first-order sigma-delta modulator.

# Appendix D
# Testing the Chip (IC # T37C-BS)

The design of first order sigma-delta modulator includes individual sub-modules for testing the device. Figure D.1 shows the pin assignment for the chip layout and Figure D.2 shows the chip layout with naming each sub-module.

## D.1 Inverter circuit Testing

| PIN No. | Description |
|---|---|
| 34 | Input |
| 36 | Output |

Fabrication problems are verified by testing the inverter module. Logic '0' is applied at the input pin #34 and output (logic '1') is observed on pin #36. Logic '1' is applied at the input pin #34 and output (logic '0') is observed on pin #36.

## D.2 Integrator Module and Testing

| PIN No. | Description |
|---|---|
| 12 | Integrator Output |
| 17 | Integrator Input |
| 21 | Clock for Integrator |
| 18 | Ground for Integrator |
| 13 | Bias for Integrator |

The Analog Integrator is tested by using 4V p-p square wave. The clock of the Integrator is a pulse of ±2.5V. When the pulse is HIGH, the input is sampled and when the pulse is LOW, the circuit is in the hold mode. The output is observed at pin #12.

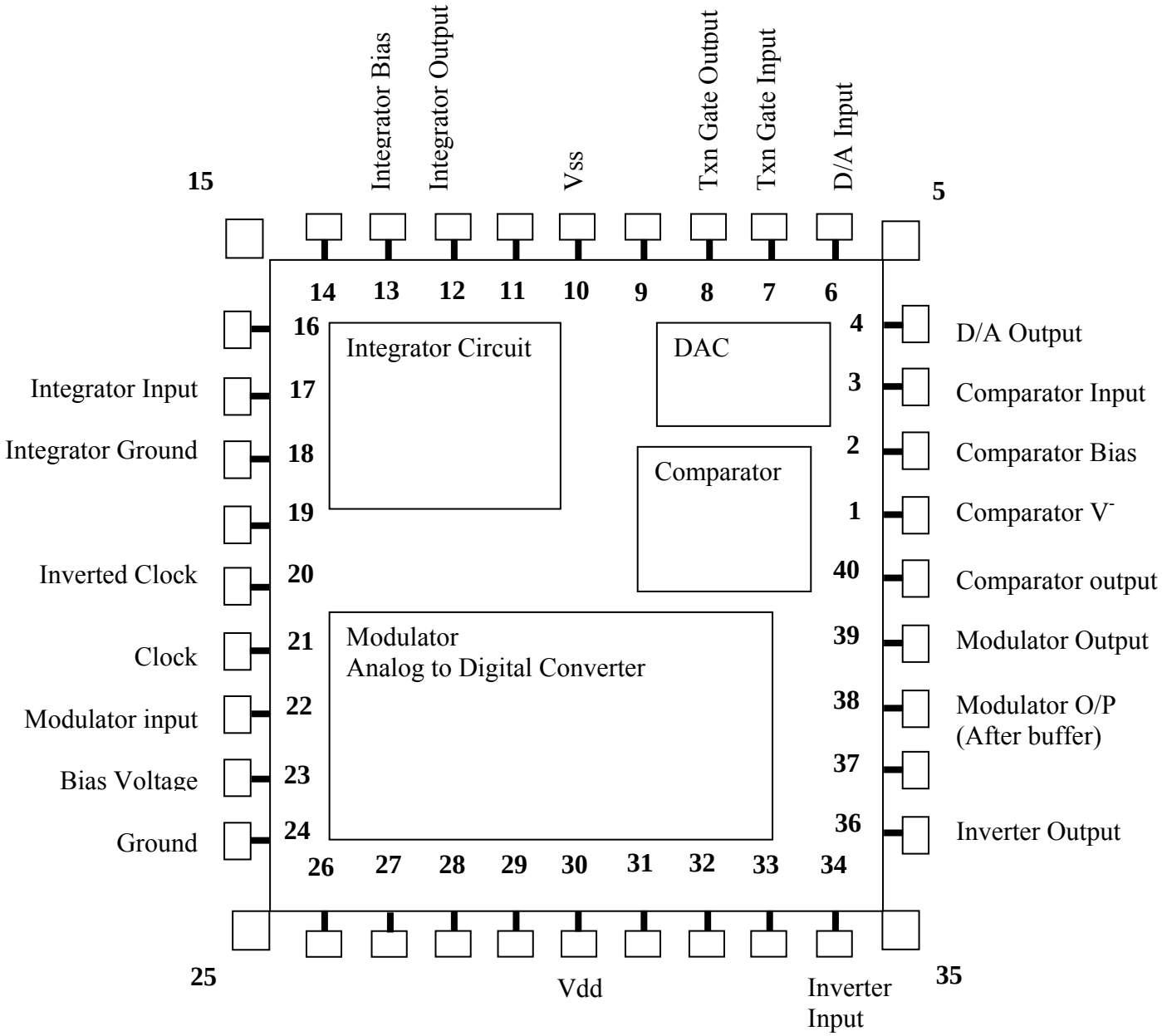



Figure D.1: Pin assignment for the chip layout.

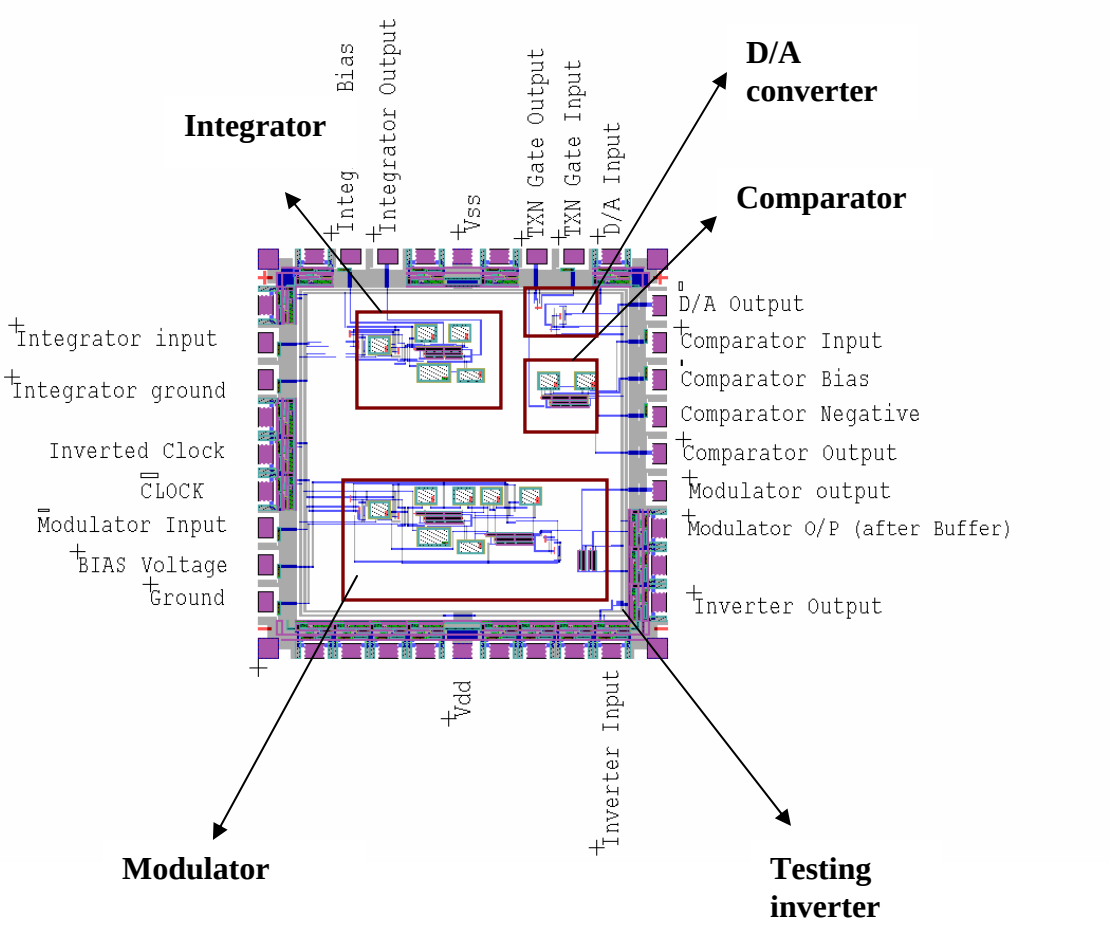



Figure D.2: Chip layout .

## D.3 1-Bit Comparator (ADC) and Testing

| PIN No. | Description |
|---|---|
| 40 | Comparator Output |
| 3 | Comparator Input |
| 2 | Comparator Bias |

The 1-Bit A/D is tested by giving 4V p-p square wave to the comparator positive. The comparator negative is grounded. The output is observed at pin # 40.

## D.4 First Order Sigma-Delta Modulator Testing

Table D.1 gives the pin numbers and their description to test 1st order modulator.

| Pin No. | Description of PIN |
|---|---|
| 10 | $V_{SS}$ |
| 21 | Clock |
| 22 | Modulator Input |
| 23 | Bias Voltage |
| 24 | Ground For Test Integrator |
| 38 | Modulator Output (after Buffer) |
| 39 | Modulator Output |
| 30 | $V_{DD}$ |

## D.5 First Order Modulator Testing in Normal Mode

1. Supply voltages of ±2.5V is given to the power supply pin numbers of the chip ($V_{DD}$ = +2.5V and $V_{SS}$ = -2.5V).

2. The 1st order modulator is tested with giving sinusoidal input to the analog input pin # 19.

3. The output of the Modulator is observed at pin # 39 on the oscilloscope.

## D.6 Testing of First Order Modulator using Logic Analyzer HP 1660CS

A sine wave with 1.5 KHz and amplitude as 2V p-p is given to the modulator. The clock input is a square wave with 700 KHz frequency and -2.5V to -2.5V amplitude. The output is observed at pin # 39 on the analyzer.

## D. 7 Decimator Details.

Table D.2 gives the pin numbers and description of the Decimator implemented on an FPGA board.

| PIN No. | Description |
|---|---|
| 17 | Digital Output BIT 1 |
| 19 | Digital Output BIT 2 |
| 21 | Digital Output BIT 3 |
| 23 | Digital Output BIT 4 |
| 25 | Digital Output BIT 5 |
| 27 | Digital Output BIT 6 |
| 29 | Digital Output BIT 7 |
| 31 | Digital Output BIT 8 |
| 41 | Input to Decimator |

## D. 8 Analog-to-Digital Converter Testing

1. The output from the first order modulator pin #39 is shifted from ±2.5V to ±5V since the logic HIGH of the Altera board is 5V and the logic LOW is 0V. This is done using an off-chip IC.

2. The shifted modulator output from the first order modulator is connected to the input of the decimator pin # 41.

3. Logic analyzer is used to observe the 8-bit digital output on the pin numbers given in Table D.2.

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# Vita

Syam Prasad Kommana was born on August 10, 1979, in Vijayawada, India. He received his Bachelor of Technology in Electronics and Communications Engineering from Nagarjuna University, Guntur, India, in May 2001. He is enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, since August 2001 to attend graduate school. His research interests include mixed-signal circuits and digital signal processing.