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Development of an algorithm for switching compensator control based on the Currents' Physical Components theory

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DEVELOPMENT OF AN ALGORITHM OF SWITCHING COMPENSATOR CONTROL BASED ON THE CURRENTS' PHYSICAL COMPONENTS THEORY

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ABSTRACT

Development of a three-phase switching compensator algorithm, based on the Currents' Physical Components (CPC) power theory and capable of performing in real time, is the subject of this thesis. The compensator algorithm could be implemented to control a PWM Inverter, which would perform as a shunt switching compensator of harmonic, reactive and unbalanced currents or a customizable combination of the three.

The hardware used to demonstrate the ability of the algorithm to perform within the restraints or real time operation is a Motorola DSP56F807 evaluation mode DSP board and a set of voltage and current sensors. The Evaluation Board was programmed, using Metrowerks Code Warrior 7.0©, to provide the compensator control algorithm according to the CPC power theory. The software written to control the compensator is primarily C based, but includes Java beans to control specific setting on the DSP board.

After data acquisition and digital signal processing, a CPC based algorithm, developed within this thesis, is the tool used to generate the reference signal. Once the reference signal is attained, the space vector PWM technique is applied to generate PWM outputs, which could be used to control an inverter. The inverter could then inject current into the power system such that the supply current is symmetrical, sinusoidal and in phase with the supply voltage.

CHAPTER 1: INTRODUCTION

1.1 Supply Quality and Loading Quality

Approximately two thirds of the electrical loads in the United States are rotating motors. The quality of the supply voltage is vital in the performance of these rotating machines as well as many other less common loads. Before discussing quality and how it pertains to the supply, an ideal supply must first be defined. An ideal supply voltage is a three phase voltage which is symmetrical, sinusoidal and has a constant RMS value. Sags, swells and transients will affects the RMS value, while harmonics and noise will cause the supply voltage to be nonsinusoidal. Quality, as it relates to the supply voltage, is a relative term used to compare two supplies, of which one is the ideal supply. The term "supply quality" as used in ref. [2] will be used in place of "quality of the supply" throughout this thesis.

Any deviation from the ideal supply will contribute to reducing the supply quality. The supply quality is important in determining how well a customer will utilize energy. Energy efficiency and cost effectiveness are tied together and both will become worse with the degradation of the supply quality. Efficiency will go down because of energy losses, primarily as heat, in rotating motors. An additional negative side effect of poor supply quality is the reduced life expectancy or electrical equipment because of the extra heat induced by the power losses.

The other side of this discussion is the quality of the load, which will be referred to as "loading quality"[2]. The term *ideal load*, will be used in this paper to refer to a load that is seen by the supply as balanced and purely resistive with parameters that do not change in time. Any deviation from the ideal load, including reactance, imbalance, a nonlinear characteristic or time dependent variations will reduce or degrade the loading quality. Loading quality is an important aspect of how energy efficient or cost effective it is for a utility to deliver energy. A reduction in

loading quality will lead to a reduction in power factor. As loading quality becomes lower, the power losses and costs associated with energy delivery become higher.

The phenomena associated with loading quality and supply quality are more commonly referred to by the term "power quality". The term, however, is vague because one cannot decipher if a degradation in power quality is due to a degradation in the quality of the supply, the quality of the load, or the quality of both the supply and the load. An increase in voltage and current harmonics can be characterized as a degradation in power quality even though this can be the effect of two different causes.

The appearance of harmonics in the voltage can be the response of current harmonics injected into the system by a harmonic generating load, which would be a loading quality issue. The appearance of voltage harmonics can also be a result of low supply quality, in which case the current harmonics may be only a response to the distribution voltage harmonics. When observing the supply voltage and load current in a cross-section it is important to know the source of the degradation in power quality, which is why the terms "loading quality" and "supply quality" will be used instead of "power quality"

The knowledge which is available when the supply quality and loading quality are known is crucial when developing and implementing a compensator. A compensator must possess the ability to make adequate decisions regarding compensation of asymmetry, imbalance, harmonics, noise and time dependent variations.

1.2 Compensator Topologies

There are various types of compensators which can be used to improve loading quality, supply quality or both. The type will greatly affect the capabilities of the compensator as well as the cost of the compensator. Although each group can be broken down further, most compensators fit into one of three categories.

The most common category is parallel or shunt compensators, sometime referred to as "active power filters" [12]. Shunt compensators have essentially no affect on supply quality and are used only to improve loading quality. These compensators determine the detrimental current and inject this current into the system so the load can draw its typical current while the supply will see a near ideal load. The power ratings of the electrical components in a shunt compensator are lower than those in a series compensator because the active current, which usually makes up a majority of the current, does not flow through shunt compensators.

Another category is series compensators. These compensators are placed in series with a load in between the supply and the load. A series compensator injects a voltage into the power system to make the supply seen by the load closer to the ideal supply. They can only affect the supply quality and they must be sized according to the total load rating. Because the entire load current flows through series compensators, they are typically more expensive than shunt compensators. Some industrial customers are also reluctant to place a filter or compensator in series with a load because of the extra impedance and voltage drop.

A third category of compensators includes combining series and shunt compensators. This category is commonly referred to as hybrid compensators, although hybrid can imply other completely different meanings. A hybrid compensator is capable of improving both supply quality and loading quality because it injects voltages and currents into the system. This approach can be the most effective structure, but it is also typically the most complex and expensive.

1.3 Thesis Subject

With the information presented in sections 1.1 and 1.2, the subject and objectives of the thesis can now be described with far less confusion. This section will provide a general overview of the subject, most of which is common to many compensators.

The most commonly used compensator is a pulse width modulation or PWM inverter-based shunt switching compensator. This compensator is composed of a PWM inverter, built of six power transistors and an energy storage device, typically a capacitor as shown in figure 1.1, as well as a Data Acquisition (DAQ) and Digital Signal Processing (DSP) System for the compensator control.

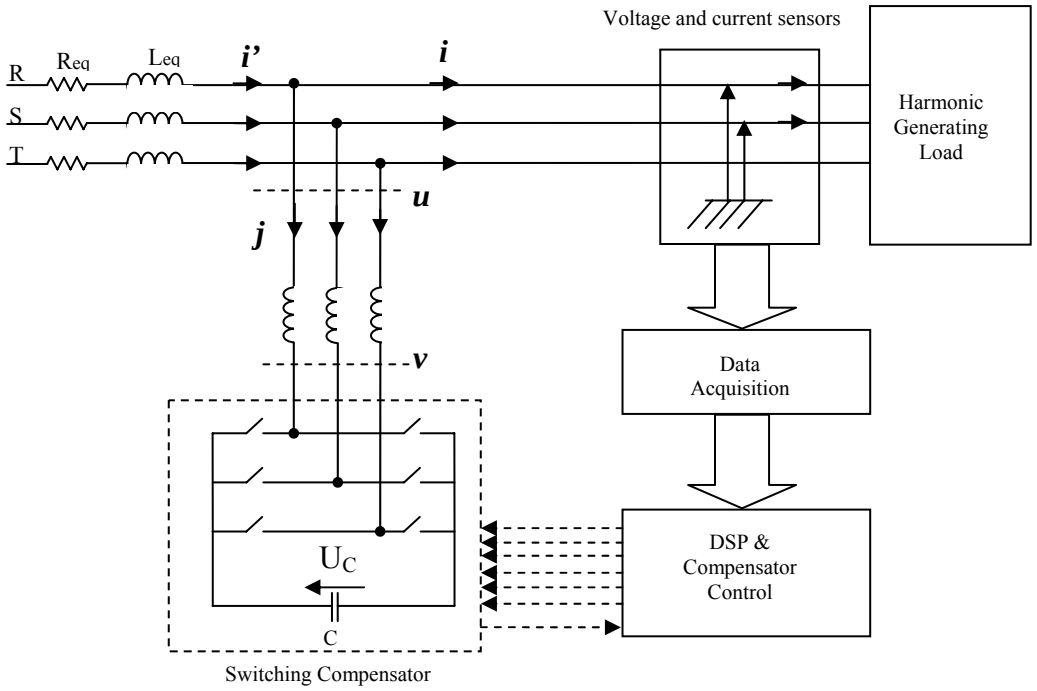

Figure 1.1 PWM Inverter-Based Shunt Switching Compensator

A shunt compensator will have approximately no affect on the supply voltage, therefore it cannot affect the load current, ***i***. The load current contains a number of components that do not contribute to energy transfer to the load, but these components increase the rms value of the load current. Each non-active component of the current should be compensated for various reasons. All non-active current increases energy losses, decreases power factor and reduces the life of transmission and distribution equipment. Harmonic current can lead to the miss operation of protective equipment causing false trips, or electronic equipment many not function properly. Harmonic current also increases voltage distortion, which will cause further problems for

electronic equipment, and increases the possibility of damaging power factor correcting capacitors if a resonance occurs near a voltage harmonic. Another non-active component of the current that is compensated is the unbalanced current. This current component increases energy losses and increases voltage asymmetry. Voltage asymmetry can cause three phase loads to function improperly, especially rotating machines, which will experience increased heating and reduced power.

If all components of the current, which do not deliver energy, are supplied by the compensator, then they can be removed from the distribution system. Reducing supply current while keeping energy and voltage rms values constant will improve loading quality, power factor and the effectiveness of energy delivery.

A compensator must sample the currents and voltages and decide which current components should be injected. The compensator must separate the active and non-active current components and inject the current into the system which yields the best possible energy delivery. After compensation, the supply current should contain only active current while the rest of the current is supplied to the load by the compensator. When a load is fully compensated it will appear to the supply as an ideal load, meaning the loading quality is ideal.

The most commonly used compensators to improve loading quality are the PWM inverter-based shunt switching compensators. Unfortunately, there are situations when algorithms used to control these compensators produce inadequate or sometimes detrimental results. The most commonly used algorithms, based on well known power theories, may yield erroneous results in the presence of non-ideal supply voltage. Sags, swells, distortion and asymmetry in the supply voltage are often misinterpreted by these compensators due to their inability to distinguish between loading quality and supply quality.

1.4 Thesis Objectives

The objective of this thesis is the development of a compensation algorithm based on the Currents' Physical Components (CPC) power theory used for compensator control. Using CPC, an algorithm can separate all currents and voltages into their physical components, an ability which will allow compensators to overcome many of the shortcomings of compensators currently in use. In the presence of low supply quality, where other algorithms lose effectiveness, this CPC based algorithm will allow loads to be fully compensated.

Although actual compensation will not be performed within this thesis, the commonly used PWM inverter-based shunt switching compensator is the structure which this algorithm is designed to control. The data acquisition and digital signal processing will be performed with a Motorola DSP56F807 Evaluation Board. Because the algorithm is designed to control a shunt compensator, there will be little or no affect on supply quality, only on the loading quality.

CHAPTER 2: THE CONTROL ALGORITHM

2.1 The Reference Signal

In order to improve the loading quality, a compensator has to inject a compensating current of specific contents and waveform into the distribution system. Information on this current, referred to as a *reference signal*, usually in a digital form, has to be provided by the DSP system based on the data acquired by the data acquisition (DAQ) system. One of the biggest challenges facing the development of a compensator is the generation of the reference signal.

There are different approaches for determining the reference signal. If the compensator is working in a closed loop, it will typically measure the current on the supply side of the compensator and compensate deviations from the desirable current. If the compensator is operating in an open loop, it will measure the current on the load side of the compensator. In this case it should reproduce the reference signal as its input current.

Before a reference signal can be generated at least two voltages and two currents are sampled using a sample and hold circuit and converted to digital form with analog to digital converters. After these quantities are measured, one of several power theories, to be described later, is applied to generate the reference signal. Since making the load appear to the supply as an ideal load requires a specific current to be injected, it can be expected that the application of any power theory should yield approximately the same reference signal. There are conditions however, where the application of different power theories will yield different results. If the goal of compensation is for the supply to see an ideal load, there can only be one correct solution, therefore it can be concluded that only one and possibly none of the results are correct when the results differ from one another.

2.2 Generating PWM Output

Once the reference signal in known, a power electronics technique must be implemented in order to inject the desired current waveform into the power system. Mathematical operations which utilize Space Vector Pulse Width Modulation (SV-PWM) will be used to accomplish this task. The first step is to find the reference voltage, which is the voltage necessary to inject the reference current into the power system. The next step is to convert the voltage reference signals into the αβ plane using the Clarke transform. The αβ plane is divided into six equally spaced sectors separated by state vectors, where each vector represents an inverter switching state. The compensator output voltage, $\boldsymbol{v}$, is controlled using fast switching transistors. The compensator can supply a reference voltage anywhere on the αβ plane with a magnitude less than or equal to the state vectors.

The detailed calculations for finding $\boldsymbol{v}$, identifying the necessary state vectors and determining the switching time intervals will be presented in chapter five.

2.3 Capacitor DC Voltage Control

It is very important to keep the capacitor voltage, U_C in figure 1.1, nearly constant because the algorithm is implemented with the assumption that this voltage always remains the same. The compensator output voltage is merely the capacitor voltage applied across some combination of the three phases, therefore the magnitude of this voltage is crucial because it will influence the magnitude of the compensation current.

There are two reasons why the capacitor voltage will decay if it is not controlled. First, there are energy losses within the compensator, primarily in the inductors and power switches. If the compensator algorithm were to neglect these losses, this energy would be delivered from the capacitor and consequently the voltage would decline. The losses must be accounted for within the algorithm to prevent a voltage decay on the capacitor.

The second reason why a voltage decline may be seen on the capacitor is when the compensator delivers active power to the load. An example of when the compensator would supply active power is when a load draws harmonic current in the presence of same harmonic voltage. If the compensator is supplying active power, the energy is supplied by the capacitor, therefore the voltage will decline.

To eliminate the problem of capacitor voltage decay, energy must be sent to the capacitor from the supply. This should be done in a way which will not reduce loading quality, therefore balanced and sinusoidal active current is supplied to the compensator. To accomplish this, the reference signal should be altered to include a small positive active current proportional to the difference in the magnitude of the capacitor voltage and the predetermined desired voltage.

CHAPTER 3: METHODS OF REFERENCE SIGNAL GENERATION

In order to generate a reference signal for control of a switching compensator, an algorithm must be developed based on a power theory which can interpret the measured data. This chapter will discuss some of the most commonly used power theories in the development of the reference signal generating algorithms.

3.1 Instantaneous Reactive Power *p-q* Power Theory

The Instantaneous Reactive Power (IRP) *p-q* Power Theory [3, 13] is the most prevalent power theory used to develop reference signal generating algorithms [4]. The IRP *p-q* based algorithms require that the alternating component of the instantaneous power be compensated. This theory is based on the assumption that instantaneous active power of ideally compensated loads should always be constant.

The power properties of electric loads are described in terms of voltages and currents on the αβ plane, meaning a Clarke Transform must be performed. Since $i_T = -i_R - i_S$ in a three wire system, it is possible to perform the transform with only two of the voltages and two of the currents.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \sqrt{3/2}, & 0 \\ 1/\sqrt{2}, & \sqrt{2} \end{bmatrix} \begin{bmatrix} i_R \\ i_S \end{bmatrix} \qquad \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} \sqrt{3/2}, & 0 \\ 1/\sqrt{2}, & \sqrt{2} \end{bmatrix} \begin{bmatrix} u_R \\ u_S \end{bmatrix} \tag{3.1}$$

According to the IRP *p-q* theory, the load properties can now be described in terms of two instantaneous quantities, active power *p*, and reactive power *q*, defined as follows [3].

$$p = u_\alpha i_\alpha + u_\beta i_\beta \tag{3.2}$$

$$q = u_\alpha i_\beta - u_\beta i_\alpha \tag{3.3}$$

The instantaneous quantity *q* should be compensated as well as the alternating component of active power *p*, which will be referred to as $\tilde{p}$. After the instantaneous powers to be compensated are know, the compensation current should be determined with the given formula.

$$\begin{bmatrix} j_\alpha \\ j_\beta \end{bmatrix} = \frac{1}{u_\alpha^2 + u_\beta^2} \begin{bmatrix} u_\alpha, & -u_\beta \\ u_\beta, & u_\alpha \end{bmatrix} \begin{bmatrix} \tilde{p} \\ -q \end{bmatrix} \tag{3.4}$$

Now that the compensation current has been solved for, it should be converted into phase currents using an inverse Clarke Transform.

$$\begin{bmatrix} j_R \\ j_S \end{bmatrix} = \begin{bmatrix} \sqrt{2/3}, & 0 \\ -1/\sqrt{6}, & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} j_\alpha \\ j_\beta \end{bmatrix} \tag{3.5}$$

If $j_T = -j_R - j_S$ is applied, the current to be injected into each phase is known and the reference signal has been solved for.

Unfortunately, the assumption that instantaneous active power of ideally compensated loads should always be constant is not always true, as questioned in ref [5] and ref [6]. Degradation in the supply voltage will often lead to an alternating component in the instantaneous active power p, even when applied to an ideal load. Attempts to compensate the alternating component in the presence of a non-ideal supply voltage will rarely if ever lead to total compensation and can even cause detrimental results.

If the example [6] of an asymmetrical supply voltage is considered where

$$\begin{bmatrix} u_R \\ u_S \end{bmatrix} = \sqrt{2} \begin{bmatrix} U^p + \cos\omega_1 t + U^n \cos\omega_1 t \\ U^p \cos(\omega_1 t - 120^0) + U^n \cos(\omega_1 t + 120^0) \end{bmatrix} = \sqrt{3} \begin{bmatrix} (U^p + U^n)\cos\omega_1 t \\ (U^p - U^n)\sin\omega_1 t \end{bmatrix} \tag{3.6}$$

then in αβ coordinates

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \boldsymbol{C} \begin{bmatrix} u_R \\ u_S \end{bmatrix} = \sqrt{3} \begin{bmatrix} (U^p + U^n)\cos\omega_1 t \\ (U^p - U^n)\sin\omega_1 t \end{bmatrix}. \tag{3.7}$$

If this voltage is then applied to a balanced three phase resistive load where the conductance of each branch is equal to G, then the current would be

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \boldsymbol{C} \begin{bmatrix} i_R \\ i_S \end{bmatrix} = \sqrt{3}G \begin{bmatrix} (U^p + U^n)\cos\omega_1 t \\ (U^p - U^n)\sin\omega_1 t \end{bmatrix}. \tag{3.8}$$

The instantaneous active power of the balanced resistive load with the given supply is

$$p = u_\alpha i_\alpha + u_\beta i_\beta = 3G[U^{p2} + U^{n2} + 2U^p U^n \cos 2\omega_1 t]. \tag{3.9}$$

There is obviously an alternating component of the active power which is equal to

$$\tilde{p} = 6GU^p U^n \cos 2\omega_1 t. \tag{3.10}$$

The IRP *p-q* theory based algorithms will compensate this alternating active power, which will generate a disturbing component in the reference signal. A more detailed analysis of IRP *p-q* compensation in the presence of non-ideal supply voltage is performed in reference [1], including voltage distortion and imbalance.

The IRP *p-q* Power Theory provides a straight forward approach to compensation, however, the inability to distinguish between supply quality and loading quality create potential problems. Compensation should always provide beneficial results, regardless of if the supply voltage is ideal or non-ideal. This approach will be avoided because it requires favorable conditions that may not always be available.

There are other methods of reference signal generation based on the IRP *p-q* Power Theory [7, 8 and 17]; but they have the same problems as described above.

3.2 Currents' Physical Components Power Theory

The Currents' Physical Components (CPC) power theory [11] is a frequency domain approach for describing power properties of electrical systems, while the previously discussed power theory is strictly a time domain approach. Although compensation applications have utilized aspects of this theory, as in ref [18], it has been avoided due to the perception of all frequency domain applications being too computationally complex for real time calculations. CPC is founded on physical phenomena in electrical systems, therefore it provides insight into

power properties of electrical systems. The compensation algorithm will utilize both the frequency domain and the time domain. The fundamental currents and voltages are calculated and the active current is subtracted from the total current. The remaining current is only viewed as a current with a magnitude that varies in time. The frequency domain allows the algorithm to calculate the any component of the current, while the time domain allows for faster computations. Because reactive, unbalanced and harmonic current are all should all be compensated, they do not have to be calculated, instead they can be consider the remainder of the total current minus the active current.

This section will briefly cover the steps necessary to generate a CPC based reference signal. A more detailed description of the operations performed will be discussed in chapter four.

The goal of compensation is to make the load appear ideal as seen by the supply. An ideal load, as defined in chapter one, is a load that is seen by the supply as balanced and purely resistive with parameters that do not change in time. The current drawn by an ideal load will contain only active, positive sequence, sinusoidal components, therefore all energy delivered to an ideal load will be useful energy. To make a load appear ideal, the current which delivers useful energy must be found. This current is the active current of the positive sequence component of the fundamental harmonic, which can be found by the following steps:

1. Load voltages and currents are acquired
2. Fundamental harmonic of the load voltages and currents is calculated
3. The fundamental harmonic is separated into symmetrical components
4. The active component of the positive sequence current is found.

Once the active current of the positive sequence component of the fundamental harmonic is known, it can be used to generate a reference signal. If this useful current is subtracted from

the load current, the remaining current can be considered as non-useful or detrimental current. The compensator can then inject the negative of this non-useful current into the power system and the supply will only deliver the useful current, meaning it will see the load as ideal.

3.3 Selection of Reference Signal Generation Method

The IRP *p-q* based compensators were discussed with details because of the large number of compensators which are based on the theory. It should also be noted that there is another little used compensator algorithm referred to as the FDB [14] method. This method is based on Fryze's power theory [15], which has already been disproven in ref [16].

After reviewing the methods mentioned above, the decision was made to use the Currents' Physical Components power theory to generate the reference signal. The decision was arrived at based on both the negative aspects of PQ and the advantages of a frequency domain approach to compensation. A more detailed comparison of the CPC and IRP *p-q* power theories can be found in ref [10].

A major advantage of a frequency domain approach is the ability to separate the current into components, such as positive sequence, negative sequence, reactive current and harmonic current. With this knowledge comes additional flexibility. Compensators can be programmable, meaning a user can select specific components to compensate or to exclude from compensation. A CPC based compensator could easily be set to work in conjunction with an existing compensator, or multiple compensators can be installed when there are advantages in doing so.

A common advantage is when multiple compensators provide similar results but the total is cheaper than a single compensator. Some current components require fast switching but not necessarily high power, while other components typically require high power but not fast switching. For a single compensator to have fast enough switching to compensate the fast varying component and high enough power to compensate the slow varying component, the cost

would likely be higher than two separate compensators to compensate each component. The additional flexibility allows compensators to be built more effectively and sometimes at a lower cost.

CHAPTER 4: CPC BASED REFERENCE SIGNAL GENERATION

This chapter explains the steps listed in Chapter 3 concerning CPC and additional considerations will also be discussed. CPC is the theory in which the compensation algorithm is based off of. The discussion will require several numerical definitions, as well as the use of terms recently coined in [2]. The following chapter will discuss utilizing the reference signal to generate the gating signals to control the power switches.

4.1 Working Current and Detrimental Current

Approximately 2/3 of electrical loads in the U.S. are rotating machines, and an even higher portion in industrial environments. Because the active power associated with the supply voltage of the negative sequence and with voltage harmonics do not contribute to the motor torque, but to harmfully overheat the motor, this power, although active, is note useful power. The only useful power is the active power associated with the positive sequence of the fundamental. It can be called “working power”. Similarly, the positive sequence component of the supply voltage and current fundamental can be called working voltage and current respectively.

When a load current contains additional components besides the working current, those components can be considered detrimental because they will generate power losses as well as reduce the mechanical power and life of electric machines. For this reason all current, which is not working current, will be considered detrimental current. Figure 4.1 is a model of the compensator which includes labels for the working current, the detrimental current and the compensator current. As can be seen on the figure, the detrimental current is not in the compensated supply current, therefore it will not be supplied to the load by the distribution system.

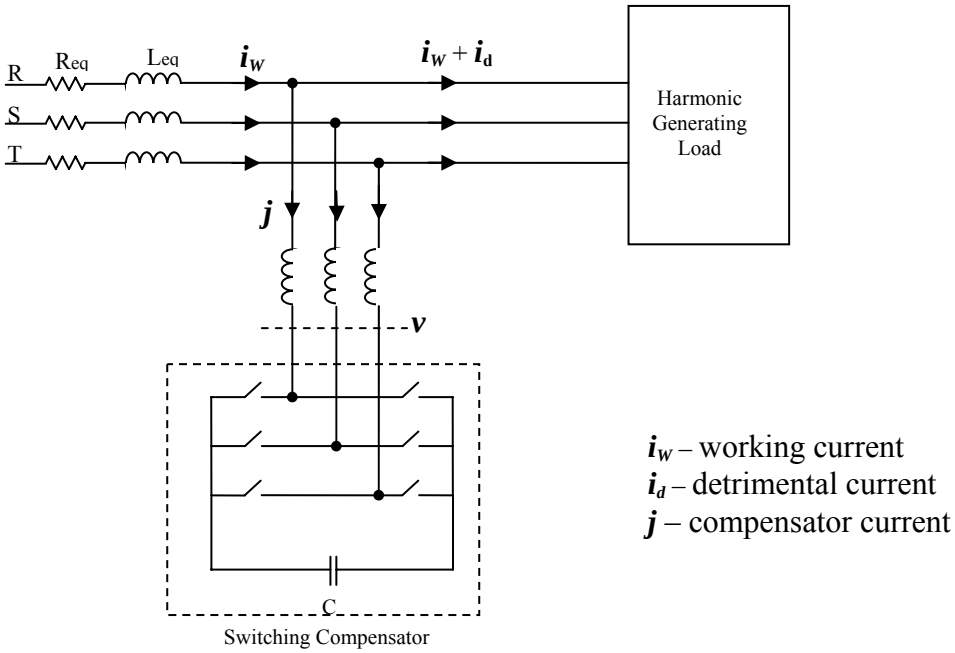

Figure 4.1 Compensator Showing Working and Detrimental Current

4.2 Generating the Reference Signal

As listed in Chapter 3, the first step in generating the reference signal is to acquire the load voltages and currents. The line currents i_R, i_S, i_T and the supply voltages u_R, u_S, u_T can be used to analyze the load, however it is simple to take advantage of the fact that each current is dependent on the other two. In a three wire power system $i_R + i_S + i_T = 0$ therefore $i_R + i_S = -i_T$, this equation is also true for voltages measured line to artificial ground, where the artificial ground is the common node of three equal resistors where the other end of the resistors are connected to the phases. It is only necessary to sample two currents and two voltages. The quantities used in this thesis are the line currents i_R and i_S and the line voltages u_R and u_S.

The next step is to calculate the fundamental harmonic of each quantity. In the past, this step has been the primary argument against using a frequency domain approach for reference signal generation due to the computational complexity of Fourier transforms. The complex rms

(crms) value of the fundamental harmonic of $\mathbf{X}_1$ of quantity $x(t)$, calculated with the Discrete Fourier Transform (DFT) is

$$\boldsymbol{X}_1 = X_1 e^{j\alpha_1} = \frac{\sqrt{2}}{N}\sum_{k=0}^{N-1} x_k e^{-j\frac{2\pi}{N}k} \tag{4.1}$$

The crms of the fundamental harmonic, however, can be calculated in a recursive way [9] where

$$\boldsymbol{X}_{1k} = \boldsymbol{X}_{1k-1} + (x_k - x_{k-N})\boldsymbol{W}^k, \qquad \boldsymbol{W}^k = \frac{\sqrt{2}}{N} e^{-j\frac{2\pi}{N}k} \tag{4.2}$$

and

$$\boldsymbol{W}^k = \frac{\sqrt{2}}{N} e^{-j\frac{2\pi}{N}k} = \frac{\sqrt{2}}{N}\cos(\frac{2\pi}{N}k) - j\frac{\sqrt{2}}{N}\sin(\frac{2\pi}{N}k)\,. \tag{4.3}$$

$\boldsymbol{W}^k$ has a real part and an imaginary part, if both are stored in a lookup table for every value of k, then $\mathbf{X}_{1k}$ can be updated with only two multiplications for each crms value, meaning eight total multiplications for the two currents and the two voltages after each set of samples is obtained.

There is a rounding error that could potentially accumulate when $(x_k - x_{k-N})\boldsymbol{W}^k$ does not equal $x_k\boldsymbol{W}^k - x_{k-N}\boldsymbol{W}^k$. One possible solution to the potential rounding error problem is to use $x_k\boldsymbol{W}^k - x_{k-N}\boldsymbol{W}^k$ in the calculations, but that would double the number of multiplications necessary to calculate the crms values. Fortunately, a rounding error in the crms calculation, even one that accumulates, becomes a non-issue after the capacitor DC voltage control code is executed. After the crms current is calculated, the DC voltage control adjusts the magnitude as needed to maintain a near constant DC voltage on the capacitor.

The next step is to find the symmetrical components, which are equal to

$$\begin{bmatrix} \boldsymbol{I}_1^{\mathrm{p}} \\ \boldsymbol{I}_1^{\mathrm{n}} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1, & \alpha, & \alpha^* \\ 1, & \alpha^*, & \alpha \end{bmatrix}\begin{bmatrix} \boldsymbol{I}_{\mathrm{R1}} \\ \boldsymbol{I}_{\mathrm{S1}} \\ \boldsymbol{I}_{\mathrm{T1}} \end{bmatrix} = \frac{1}{\sqrt{3}}\begin{bmatrix} e^{j30^0}, & e^{j90^0} \\ e^{-j30^0}, & e^{-j90^0} \end{bmatrix}\begin{bmatrix} \boldsymbol{I}_{\mathrm{R1}} \\ \boldsymbol{I}_{\mathrm{S1}} \end{bmatrix} \tag{4.4}$$

The crms value of the positive sequence is what is needed to continue, therefore

$$\boldsymbol{I}_1^{\mathrm{p}} = \frac{1}{\sqrt{3}}(\boldsymbol{I}_{\mathrm{R1}} e^{j30^0} + \boldsymbol{I}_{\mathrm{S1}} e^{j90^0}) \tag{4.5}$$

is used and the negative sequence is not calculated. Multiplication by $e^{j\alpha}$ means only argument summation, so this operation can be performed with only a single multiplication. To reduce the number of multiplications, the tables used to calculate $\boldsymbol{I}_{\mathrm{R1}}$ and $\boldsymbol{I}_{\mathrm{S1}}$ can include the $1/\sqrt{3}$ and the phase shifts e^{j30} and e^{j90}. $\boldsymbol{I}_{\mathrm{R1}}$ and $\boldsymbol{I}_{\mathrm{S1}}$ do not have to be calculated because $\boldsymbol{I}_{\mathrm{R1}} e^{j30} / \sqrt{3}$ and $\boldsymbol{I}_{\mathrm{S1}} e^{j90} / \sqrt{3}$ can be calculated directly. With this information, $\boldsymbol{I}_1^{\mathrm{P}}$ can be calculated using only addition. The formula to calculate $\boldsymbol{U}_1^{\mathrm{P}}$ is

$$\boldsymbol{U}_1^{\mathrm{p}} = \frac{1}{3}(\boldsymbol{U}_{\mathrm{R1}} + \alpha \boldsymbol{U}_{\mathrm{S1}} + \alpha^* \boldsymbol{U}_{\mathrm{T1}}) = \frac{1}{3}(\boldsymbol{U}_{\mathrm{RT1}} + \boldsymbol{U}_{\mathrm{ST1}} e^{j120^0}) \tag{4.6}$$

which can also be calculated using only addition with proper tables and previous multiplications in the same was as $\boldsymbol{I}_1^{\mathrm{P}}$.

After the positive sequence component of the fundamental harmonic quantities are known, the final step, which is to find the working current, can be completed. The working current can be expressed as

$$\boldsymbol{i}_{\mathrm{w}} = \frac{P_1^{\mathrm{p}}}{\|\boldsymbol{u}_1^{\mathrm{p}}\|^2} \boldsymbol{u}_1^{\mathrm{p}} = \frac{3U_1^{\mathrm{p}} I_1^{\mathrm{p}} \cos\varphi_1^{\mathrm{p}}}{(\sqrt{3}\,U_1^{\mathrm{p}})^2} \boldsymbol{u}_1^{\mathrm{p}} = I_1^{\mathrm{p}} \cos\varphi_1^{\mathrm{p}} \frac{1}{U_1^{\mathrm{p}}} \boldsymbol{u}_1^{\mathrm{p}} \tag{4.7}$$

where

$$\boldsymbol{U}_1^{\mathrm{p}} = U_1^{\mathrm{p}} e^{j\alpha_1^{\mathrm{p}}}, \qquad \boldsymbol{I}_1^{\mathrm{p}} = I_1^{\mathrm{p}} e^{j\beta_1^{\mathrm{p}}}, \qquad \varphi_1^{\mathrm{p}} = \alpha_1^{\mathrm{p}} - \beta_1^{\mathrm{p}} \tag{4.8}$$

Because the rms value of the working current is

$$I_{\mathrm{w}} = I_1^{\mathrm{p}} \cos\varphi_1^{\mathrm{p}} \tag{4.9}$$

The working current can also be expressed as

$$\boldsymbol{i}_{\mathrm{w}} = I_{\mathrm{w}} \frac{1}{U_{\mathrm{l}}^{\mathrm{p}}} \boldsymbol{u}_{\mathrm{l}}^{\mathrm{p}} = \sqrt{2}\, I_{\mathrm{w}} \begin{bmatrix} \cos(\omega_{\mathrm{l}} t + \alpha_{\mathrm{l}}^{\mathrm{p}}) \\ \cos(\omega_{\mathrm{l}} t + \alpha_{\mathrm{l}}^{\mathrm{p}} - 120^{0}) \\ \cos(\omega_{\mathrm{l}} t + \alpha_{\mathrm{l}}^{\mathrm{p}} + 120^{0}) \end{bmatrix}. \tag{4.10}$$

It is obvious from equation x.x that the working current is balanced and sinusoidal because it is a magnitude multiplied by a balanced sinusoidal vector.

4.3 Additional Considerations

The working current will only deliver the useful energy consumed by the load. There is additional energy that must be supplied because there will be power losses in the compensator, therefore a small amount of active power must be supplied to the compensator to keep the energy stored in the capacitor from declining. Another consideration is the non-useful energy consumed by the load. Active negative sequence power and active harmonic power will not contribute to useful work, but the compensator cannot keep the load from drawing such active power. Because all negative sequence current and harmonic current will be supplied by the compensator, the compensator will lose energy when either of these currents has an active component. In order to maintain the energy level stored in the compensator, active current must be sent to the compensator from the supply.

The additional active current sent to cover the extra power losses will be referred to as complimentary current, $\boldsymbol{i}_{\boldsymbol{c}}$ and it will deliver the complimentary power, $\mathrm{P_c}$. To calculate $\boldsymbol{i}_{\boldsymbol{c}}$, the power losses must first be defined where $\Delta \mathrm{P_{sc}}$ is the power losses in the compensator, $\mathrm{P_l^n}$ is the negative sequence power and $\mathrm{P_h}$ is the harmonic power. The complimentary current can be found as follows.

$$\boldsymbol{i}_{\mathrm{c}} = \frac{P_{\mathrm{c}}}{\|\boldsymbol{u}_{\mathrm{w}}\|^{2}} \boldsymbol{u}_{\mathrm{w}} = \frac{\Delta P_{\mathrm{sc}} + P_{\mathrm{l}}^{\mathrm{n}} + P_{\mathrm{h}}}{\|\boldsymbol{u}_{\mathrm{w}}\|^{2}} \boldsymbol{u}_{\mathrm{w}} \tag{4.11}$$

where $\boldsymbol{u}_W$ is the working voltage. P_1^n and P_h can be calculated, however ΔP_{sc} is unknown and can only be approximated. Fortunately, none of powers have by accounted for directly. A voltage control system will monitor the capacitor voltage U_c and will detect drops in voltage, which are caused when the compensator supplier active current or because of internal power losses.

Diagram 4.2 is similar to 4.1 but updated to include all currents which should be considered for compensation.

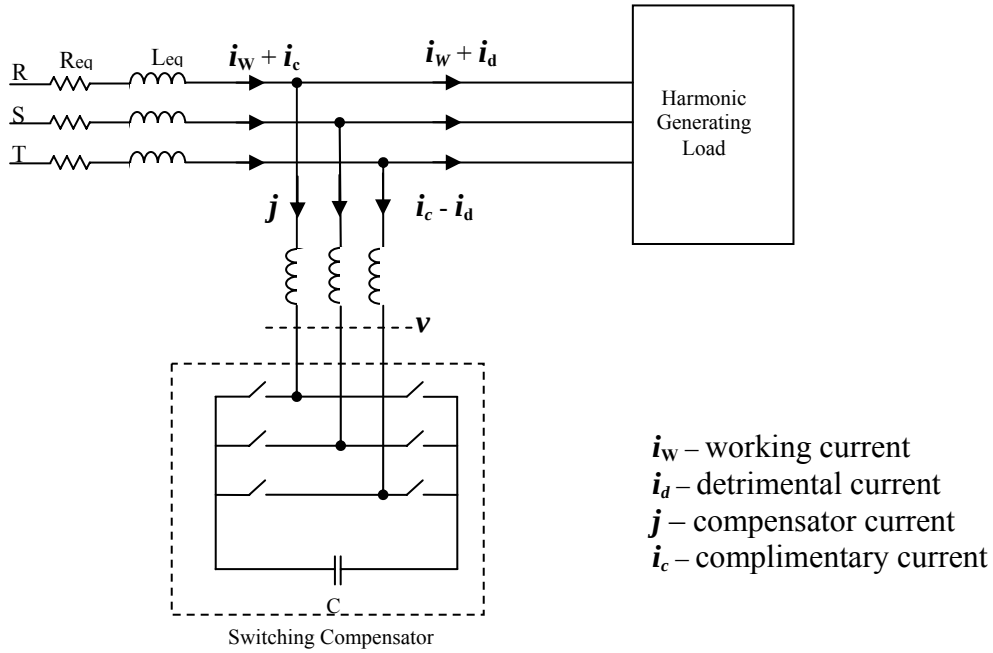

Figure 4.2 Compensator Diagram Including Complimentary Current

All useful energy will flow directly to the load without flowing through the compensator, while all non-useful energy will flow to the load through the compensator. This allows the compensator to reshape the active current sent by the supply so that the supply continues to see an ideal load.

CHAPTER 5. PWM-INVERTER VECTOR CONTROL

In order to inject a current that reproduces the digital reference signal, a method which utilizes the Space Vector Pulse Width Modulation (SV-PWM) approach will be implemented.

5.1 The αβ Representation

Converting both the distribution system voltage and the inverter output voltage to αβ coordinates allow for a visual and mathematical analysis much simpler than analyzing the operation using a three phase representation. Using a transform known as the Clarke transform, a three phase system can be represented by a single rotating vector. This vector is defined with rectangular coordinates where the horizontal axis is the α-axis and the vertical axis is the β-axis. v_α and v_β can be calculated using the following formula and reduced because one phase voltage is dependent on the other two phase voltages.

$$\boldsymbol{v}^C(t) = \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_R(t) \\ v_S(t) \\ v_T(t) \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} & 0 \\ \frac{1}{\sqrt{2}} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_R(t) \\ v_S(t) \end{bmatrix} \tag{5.1}$$

As the distribution voltages change in time, the Clarke vector rotates on the αβ plane. An example is provided in figure 5.1 for the Clarke vector at a specific time.

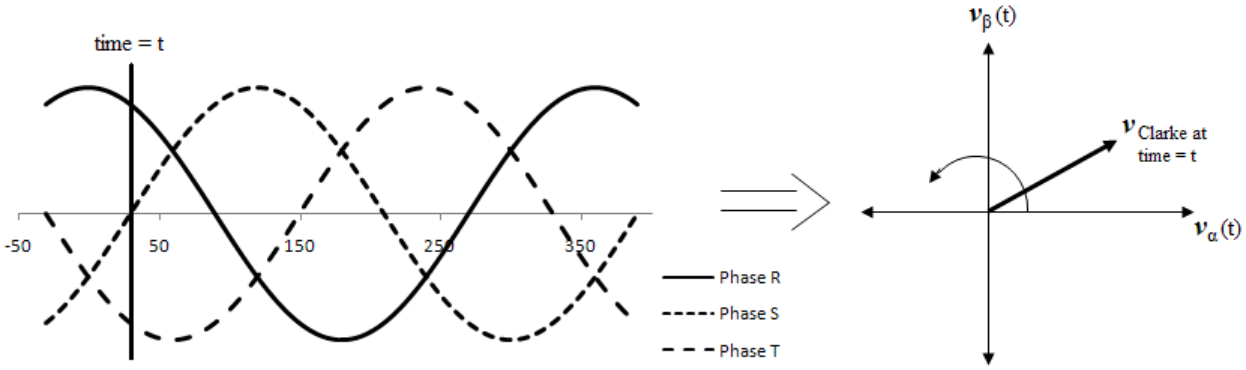

Figure 5.1 Example of How the Clarke Vector Relates to Phase Quantities

$$\boldsymbol{v}^C(t) = v_\alpha(t) + jv_\beta(t) = V^C e^{j\theta} \tag{5.2}$$

If both the distribution system voltage and the inverter output voltage are represented as vectors and the αβ plane, then the difference between them is the voltage applied across the linkage inductors as seen in figure 5.2.

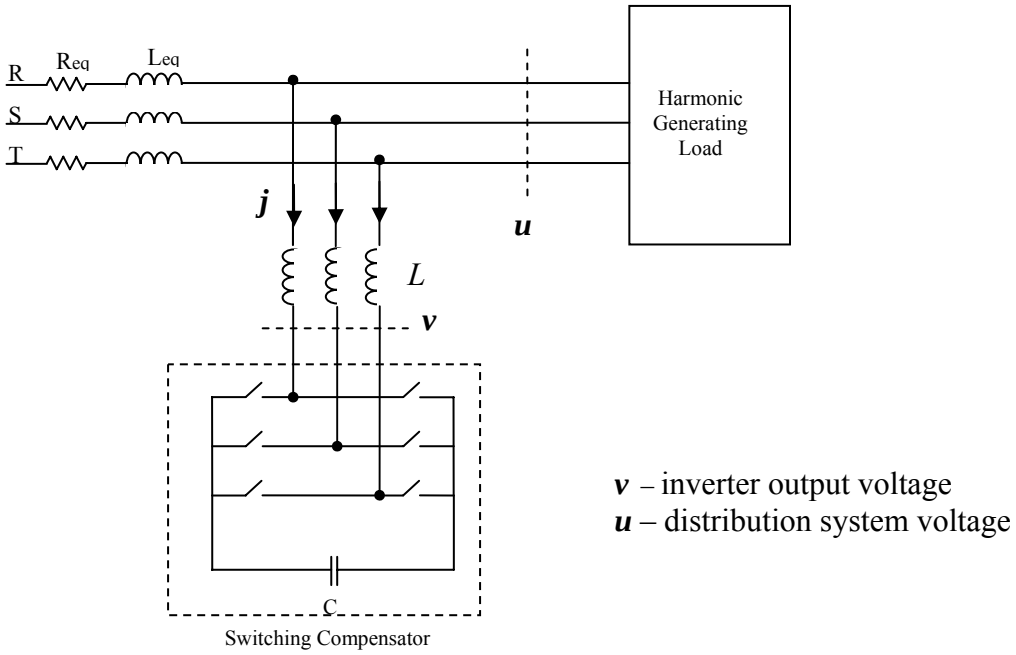

Figure 5.2 Compensator Showing the Output Voltage and Distribution Voltage Vectors

The difference in voltage vector ***u*** and voltage vector ***v*** is the voltage across the linkage inductors, which will determine the current ***j***. The compensator has no control over the distribution system voltage, the compensator can only control the compensator output voltage.

The compensator output voltage is controlled by switching the switches in the inverter. The power switches are composed of transistors where there are two transistors connected to each phase. Each transistor is always in the opposite state of the other transistor connected to the same phase. There are three transistor pairs and the combination of on transistors will determine the compensator output voltage. Using a binary representation where 1 is ON and 0 is OFF, there are eight possible combinations with three transistor pairs. Two states, 000 and 111, are

zero states and are only used to turn off the inverter. This means there are six possible combinations which will induce a voltage on the output terminals of the inverter.

If all possible inverter output voltages are viewed as vectors on the αβ plane, then there will be six state vectors, which will divide the αβ plane into six equally spaced sectors represented by roman numerals in figure 5.3. The development of this figure can be found in appendix X section X.

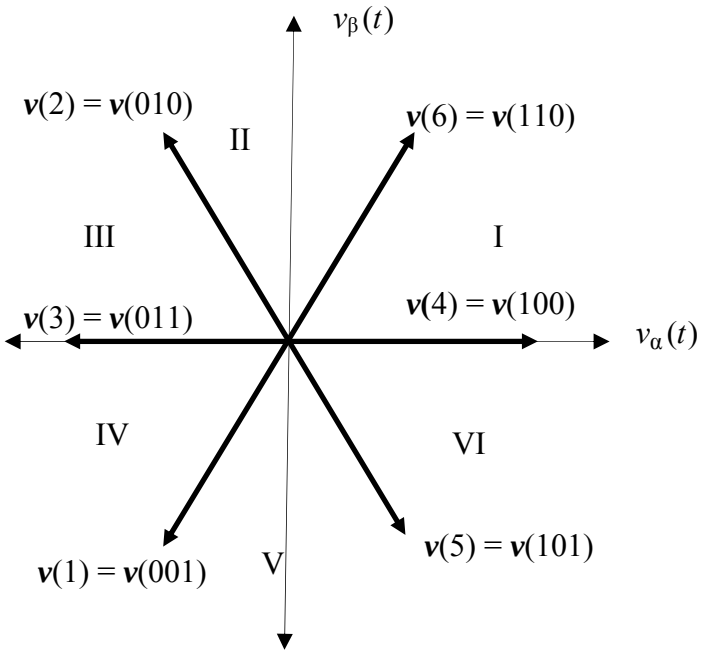

Figure 5.3 State Vectors On the αβ Plane

The compensator output voltage necessary to inject the desired current into the distribution system will fall in one of the six sectors seperated by the state vectors. The equivalent voltage can then be obtained as a combination of the state vectors which border the section the desired compensator output voltage falls in. If the desired voltage $\boldsymbol{v}$ is inbetween voltage vectors $\boldsymbol{v}_A$ and $\boldsymbol{v}_B$ as in figure 5.4, then it can be composed as a sum of $k_A\boldsymbol{v}_A$ and $k_B\boldsymbol{v}_B$ where k_A and k_B represent the duty ratio, or the ratio of the time in each switching state to the sampling time.

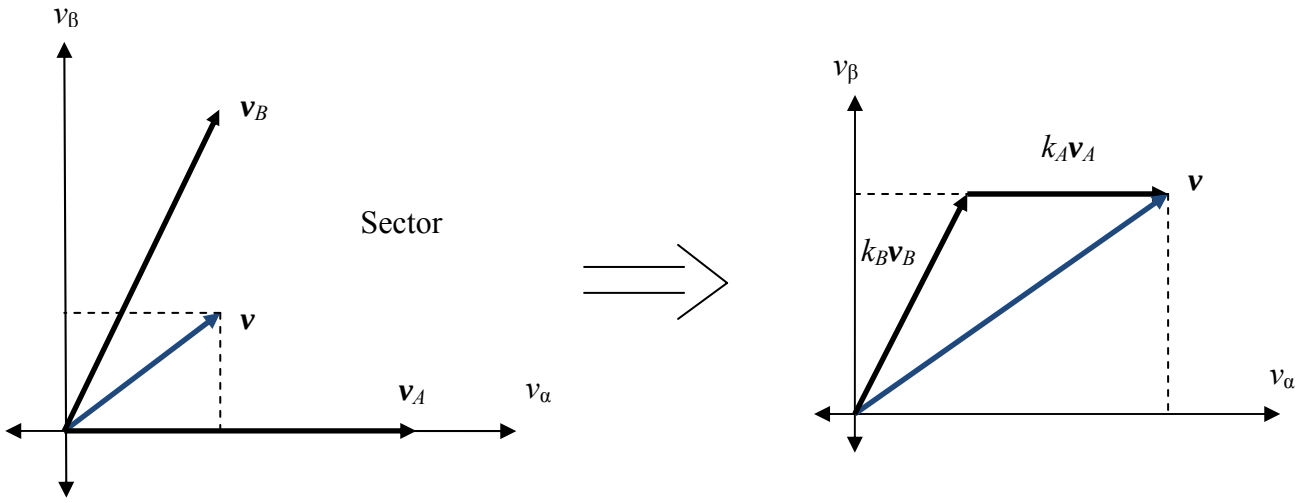

Figure 5.4 Example Vector Composed as a Linear Combination of State Vectors

The compensator must be able to supply the necessary current in an interval of time less than or equal to the sampling time T_a. If T_A and T_B are the times that the bordering state vectors are active, then the sum of T_A and T_B must be less than or equal to T_a.

$$\boldsymbol{v} = k_A\boldsymbol{v}_A + k_B\boldsymbol{v}_B$$
$$T_A = k_A T_a$$
$$T_B = k_B T_a$$
$$T_0 = T_a - T_A - T_B$$

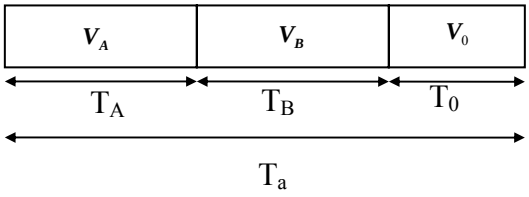

Figure 5.5 Sampling Time Broken Down Into State Vector Intervals

5.2 Calculating the Reference Voltage

Once the reference signal is know, the compensator output voltage, $\boldsymbol{v}$, must be calculated. $\boldsymbol{v}$ is the voltage necessary to inject the current, $\boldsymbol{j}$, into the distribution system, and it is calculated using the following formulas.

$$v_R(t) = u_R(t) - Rj_R - L\,\Delta j_R(t)/T_a \tag{5.3}$$

$$v_S(t) = u_S(t) - Rj_S - L\,\Delta j_S(t)/T_a \tag{5.4}$$

$$v_T(t) = u_T(t) - Rj_T - L\,\Delta j_T(t)/T_a \tag{5.5}$$

These three equations can be rewritten in the matrix form, assuming R and L are the same for all three phases as follows.

$$\boldsymbol{v}(t) = \boldsymbol{u}(t) - R\boldsymbol{j}(t) - L\,\Delta\boldsymbol{j}(t)/T_a \tag{5.6}$$

The analog to digital converters do not provide continuous values of the distribution system voltages and the reference signal, but discrete values at the instants of time $t_k = kT_a$. The equations could then be rewritten as follows.

$$\boldsymbol{u}_k = \boldsymbol{u}(kT_a) \tag{5.7}$$

$$\boldsymbol{j}_k = \boldsymbol{j}(kT_a) \tag{5.8}$$

$$\boldsymbol{v}_k = \boldsymbol{u}_k - R\boldsymbol{j}_k - L\,\Delta\boldsymbol{j}_k/T_a \tag{5.9}$$

The voltage distribution voltage, $\boldsymbol{u}_k$, is measured and the current $\Delta\boldsymbol{j}_k$ is the calculated change in inductor current based on the reference signal. The voltage could then be converted into the αβ plane using the Clarke transform and the switching intervals for each transistor pair could be calculated. Fortunately the extra computations can be avoided and the switching intervals can be computed directly from the three phase voltages with far less computations. Even though the Clarke transform was not actually used and αβ coordinates were not calculated in programming the DSP board, they were critical in developing the algorithm which was used and are an important aspect for understanding the problem.

Any desired compensator output voltage can be found on figure 5.6, where the vertical lines labeled *V(1)* through *V(6)* are the possible compensator output voltages. If the voltage necessary to inject the required current is in sector II, for example, than the inverter must spend some time in state 6 and some time in state 2. The inverter will also spend some time in a zero state depending on the magnitude of the output voltage.

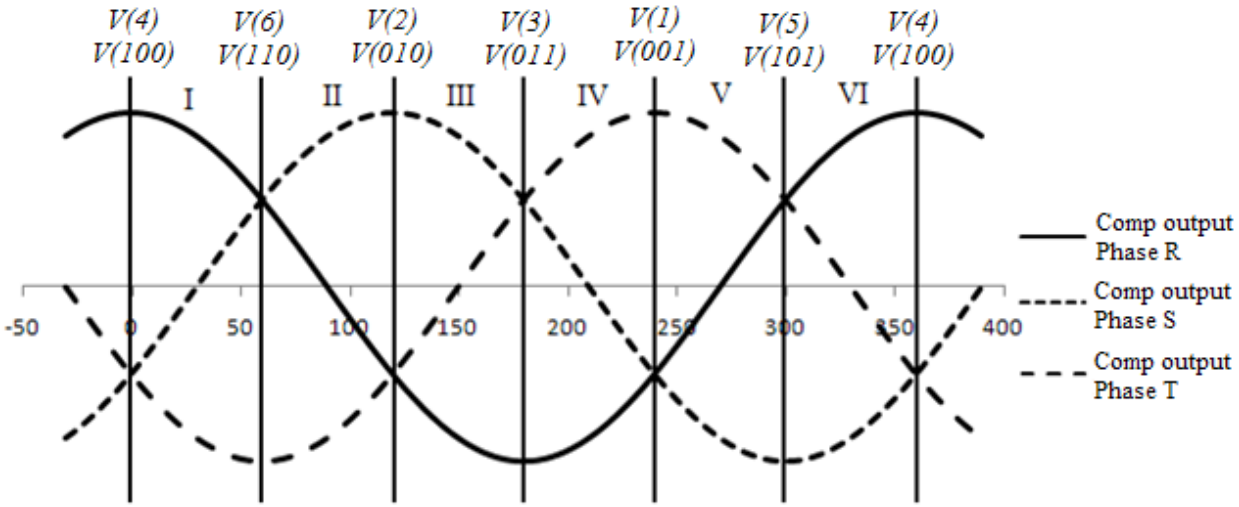

Figure 5.6 The State Vectors as They Relate to the Phase Quantities

5.3 Calculating Switching Intervals

Finding the angle and magnitude of the voltage vector, $\boldsymbol{v}_k$, as a Clarke vector and how to generate it as a sum of the two bordering state vectors can be performed using several trigonometric functions. In order to avoid that computationally demanding approach, we must first find the sector that the Clarke vector would fall in if calculated according to the Clarke Transform.

It is obvious when observing figure 5.6 that if the compensator output voltages were arranged in order of their magnitudes, that each sector would yield a different order. For example in sector I, $v_R > v_S > v_T$ and in sector II $v_S > v_R > v_T$. This information makes is very simple to determine the sector with only a few conditional checks. The flowchart in figure 5.7 represents the algorithm used to determine the sector that the Clarke vector would be in if it was calculated.

To determine the sector on the voltage vector falls in on the αβ plane, three comparisons are performed using the three phase voltages. If a voltage vector lies on the border between two sectors, then assigning it to either of the bordering sectors will produce the same results.

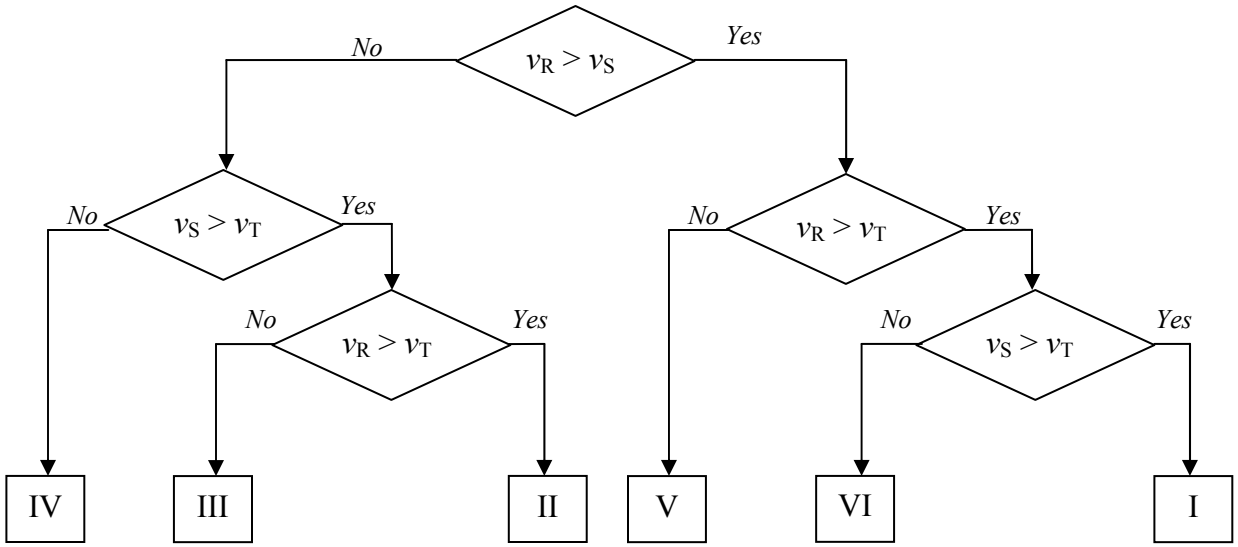

Figure 5.7 Flowchart for Finding Sectors

Once the sector is known, a switching sequence can be developed to ensure the inverter spends the correct amount of time in the states corresponding to the bordering state vectors. The state of the switches will determine the switching state, S_R, S_S and S_T, as seen in figure 5.8, are the power switches connecting phases R, S and T respectively to the positive capacitor voltage. T_R, T_S and T_T are the times that S_R, S_S and S_T are turned on. T_1 is the time that the inverter spends in the bordering state whose state vector requires closing only one of the S_R, S_S and S_T power switches and T_2 is the time that the inverter is in the other bordering state which requires closing two of the S_R, S_S and S_T power switches.

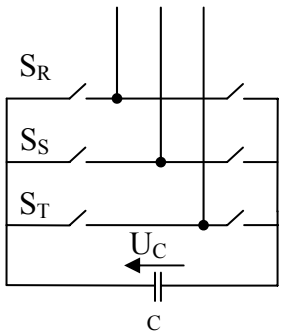

Figure 5.8 Names of the Power Switches

The calculation of the previously listed switching intervals will be discussed later in this section, first the switching sequence will be presented.

For a Clarke vector in sector I, S_R will be on for both states used to approximate the Clarke vector while S_S is on only during one of the state. T_R in this sector will be equal to the sum of T_1 and T_2, while T_S will be equal to T_2. To create a better approximation of the desired output voltage, changing from state 1 to state 2 can be performed twice by center aligning the gating signals. To form an even better approximation, the zero state, T_0, can also be split into two interval with one placed in the middle of the gating signal outputs. When using this approximation, if sector I is considered T_T will equal $T_0/2$ and this time will also be added to T_R and T_S. The proposed switching sequence can be seen in figure 5.9.

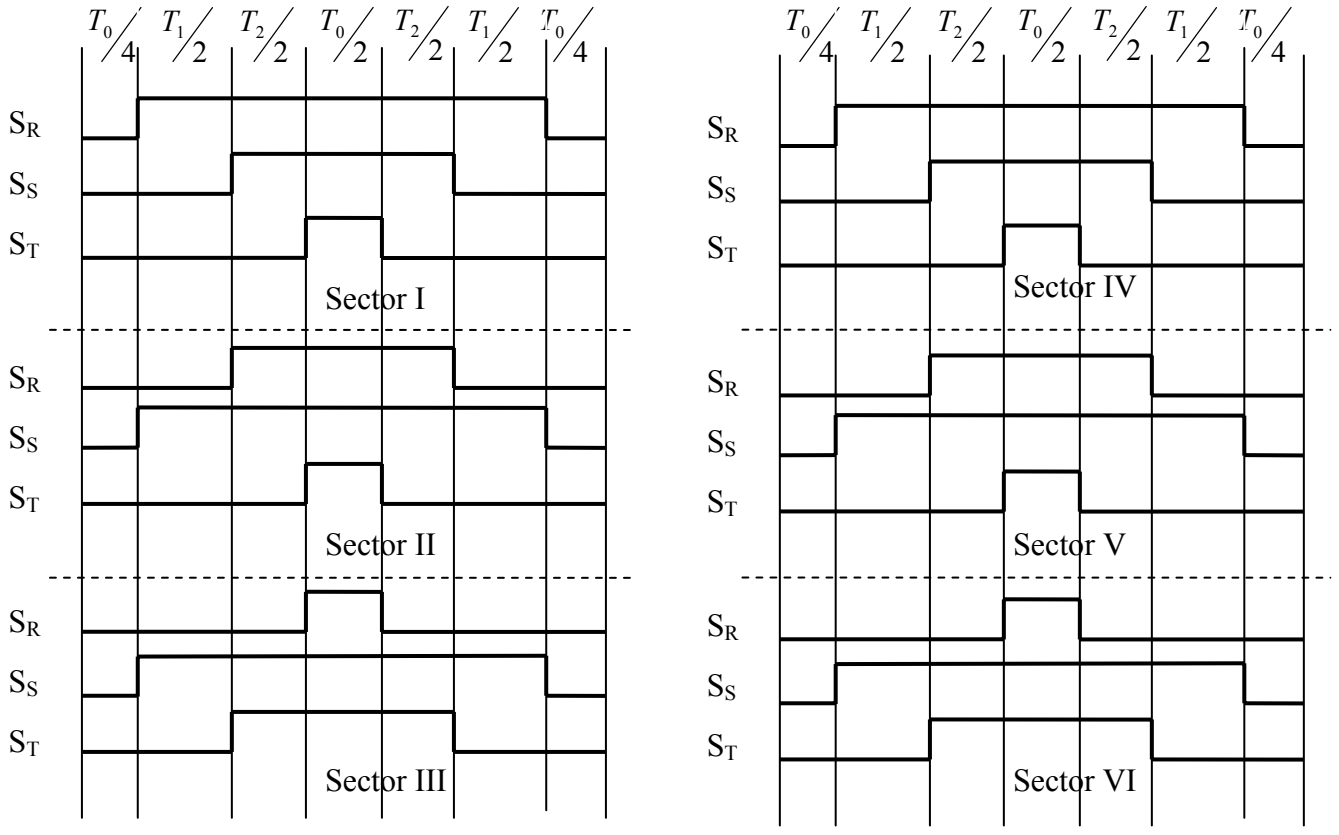

Figure 5.9 The State of the Individual Switches Verses the State of the Compensator

The switching sequence can be viewed in a binary form where the left bit represents the state of T_R the middle bit represents the state of T_S and the right bit represents the state of T_T. The binary representation can be found in table 5.1.

Table 5.1 The Switching Sequence for Each Sector

SECTOR	$T_0/4$	$T_1/2$	$T_2/2$	$T_0/2$	$T_2/2$	$T_1/2$	$T_0/2$
I	000	100	110	111	110	100	000
II	000	010	110	111	110	010	000
III	000	010	011	111	011	010	000
IV	000	001	011	111	011	001	000
V	000	001	101	111	101	001	000
VI	000	100	101	111	101	100	000

Now that the sector and switching sequence is known, the switching intervals can be calculated. If $\boldsymbol{v}$ is viewed as a vector on the αβ plane, then it can be solved as a sum of $k_A v_A$ and $k_B v_B$ with simple trigonometry as in equation 5.10 and 5.11. v_A is the state vector on the clockwise side of the Clarke vector and v_B is the state vector on the counter-cloclwise side.

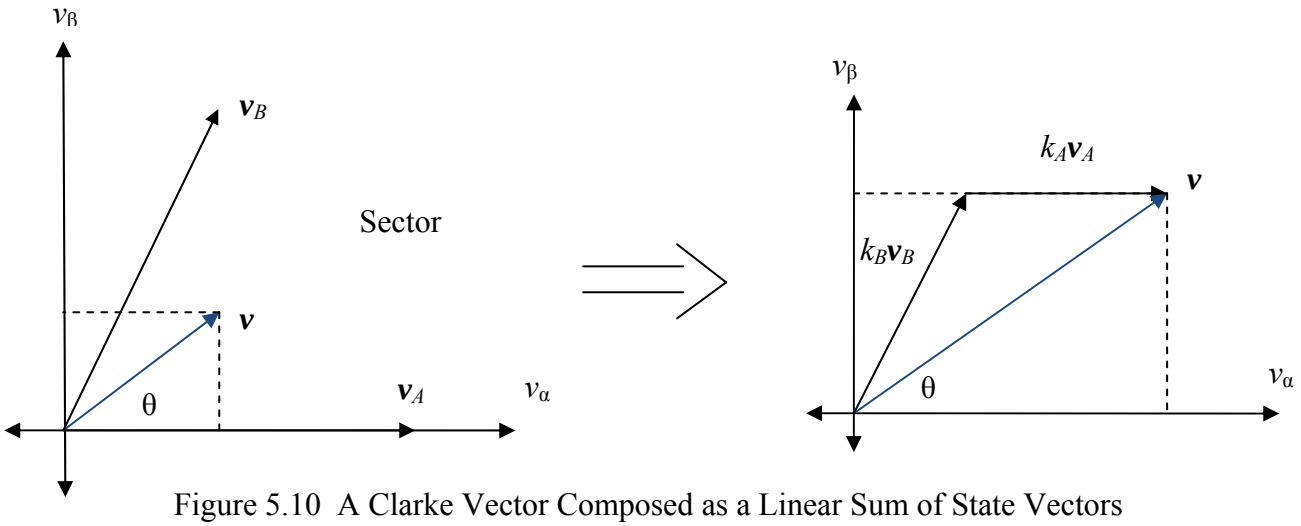

Figure 5.10 A Clarke Vector Composed as a Linear Sum of State Vectors

k_A and k_B are the duty factor or the ratio of time T_A and T_B to the sampling time T_a which are calculated according to the following formulas.

$$v\sin(\theta) = k_B v_B \sin(60) \qquad \text{rearranged} \qquad k_B v_B = \frac{v\sin(\theta)}{\sin(60)} \tag{5.10}$$

$$v\cos(\theta) = k_B v_B \cos(60) + k_A v_A \qquad \text{rearranged} \qquad k_A v_A = v\cos(\theta) - \frac{v\sin(\theta)}{\tan(60)} \tag{5.11}$$

Unfortunately trigonometric functions are very computationally intense, so another method is required if k_A and k_B are to be calculated in an acceptable amount of time on the DSP board. In order to convincingly describe the method actually used, the calculations based on the trigonometric functions will be carried out and the results compared to the method used.

Because k_A and k_B are always considered the ratio of time that the state vector to clockwise side of the Clarke vector and the state vector to the counter-clockwise side of the Clarke vector respectively are on, then figure 5.11 is a plot of k_A and k_B as a function of θ. The figure was plotted based on the magnitude of $\boldsymbol{v}$ being equal to half of the magnitude of $\boldsymbol{v}_A$ and $\boldsymbol{v}_B$.

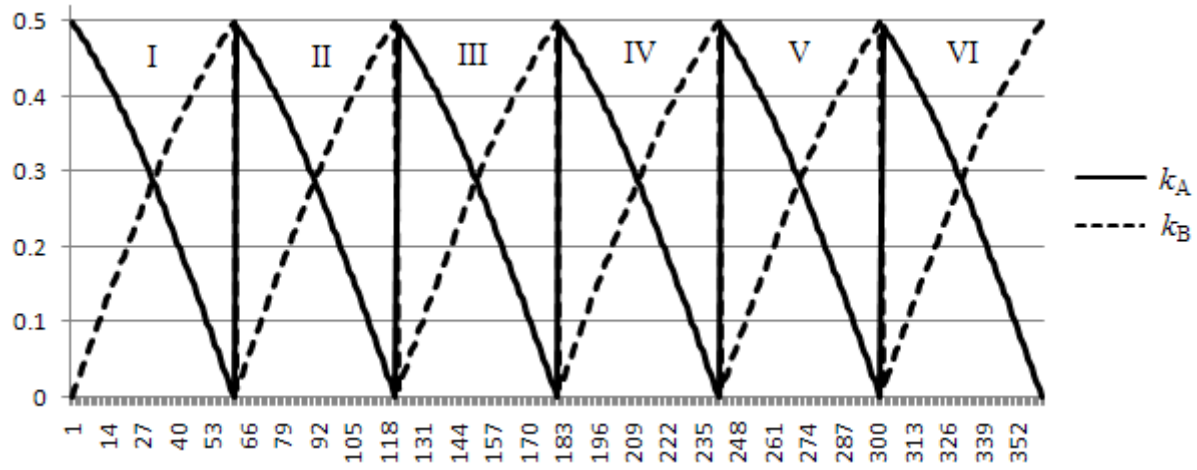

Figure 5.11 The Duty Factors k_A and k_B as a Function of θ

From this point, the time that the transistors are turned on can be calculated. Given the information in table 5.2, the duty ratio for the PWM gating signals of the power switches can be plotted as a function of θ.

Table 5.2 Timing Intervals for Individual Switches for Each Sector Using Clarke Vector

Sector	T_R	T_S	T_T
I	$T_1 + T_2 + T_0/2$	$T_2 + T_0/2$	$T_0/2$
II	$T_2 + T_0/2$	$T_1 + T_2 + T_0/2$	$T_0/2$
III	$T_0/2$	$T_1 + T_2 + T_0/2$	$T_2 + T_0/2$
IV	$T_0/2$	$T_2 + T_0/2$	$T_1 + T_2 + T_0/2$
V	$T_2 + T_0/2$	$T_0/2$	$T_1 + T_2 + T_0/2$
VI	$T_1 + T_2 + T_0/2$	$T_0/2$	$T_2 + T_0/2$

Figure 5.12 is the plot of k_R, k_S and k_T as the Clarke vector rotates on the αβ plane and it is separated by state vectors into sectors. k_R, k_S and k_T are the duty ratio of T_R, T_S and T_T to the sampling time T_a.

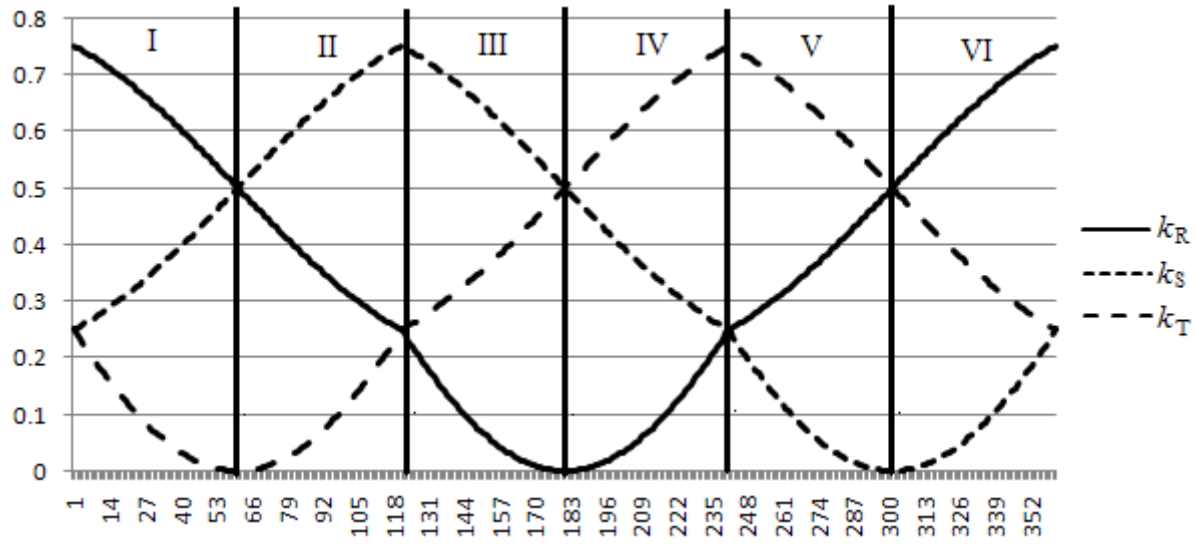

Figure 5.12 The Duty Factors k_R, k_S and k_T as a Function of θ

Using a Clarke transform to convert the compensator output voltage to a rotating vector, finding the angle θ, and finding the vector as a sum of the bordering state vectors requires many complex calculations. Fortunately, the values plotted in figure 5.12 can be obtained through

much less computationally complex means. T_R, T_S and T_T can be calculated directly from the compensator output voltages. When the voltages are converted using the Clarke transform, no information is gained or lost, therefore it stands to reason that the timing intervals can be calculated directly from the phase voltages. If the timing intervals are calculated according to table 5.3, identical duty ratio values as those in figure 5.12 are found. These formulas do not provide the same visual aid as performing similar calculations using a Clarke transform, but yield identical results.

Table 5.3 Timing Intervals for Individual Switches for Each Sector Using Phase Values

	k_R	k_S	k_T
I	$k_T + (v_R - v_T)/U_C$	$k_T + (v_S - v_T)/U_C$	$(1-(v_R + v_S - 2v_T)/U_C)/2$
II	$k_T + (v_R - v_T)/U_C$	$k_T + (v_S - v_T)/U_C$	$(1-(v_R + v_S - 2v_T)/U_C)/2$
III	$(1-(v_S + v_T - 2v_R)/U_C)/2$	$k_R + (v_S - v_R)/U_C$	$k_R + (v_T - v_R)/U_C$
IV	$(1-(v_S + v_T - 2v_R)/U_C)/2$	$k_R + (v_S - v_R)/U_C$	$k_R + (v_T - v_R)/U_C$
V	$k_T + (v_R - v_S)/U_C$	$(1-(v_R + v_T - 2v_S)/U_C)/2$	$k_R + (v_T - v_S)/U_C$
VI	$k_T + (v_R - v_S)/U_C$	$(1-(v_R + v_T - 2v_S)/U_C)/2$	$k_R + (v_T - v_S)/U_C$

Using the formulas presented in table 5.3, k_R, k_S and k_T are calculated in a more efficient manner. The results are identical to those in figure 5.12. The value of the capacitor voltage, U_C, is a controllable value which will affect the magnitudes of k_R, k_S and k_T. In most cases, the timing intervals will have to be multiplied by an additional constant to adjust for the capacitor voltage and voltage drops on the transistors and internal resistance of the inductors.

With the method for determining the switching sequence and the timing presented in this chapter, the final topic in the fundamentals of the algorithm is the method to maintain a near constant capacitor voltage on the energy storage capacitor.

CHAPER 6. INVERTER DC BUS VOLTAGE CONTROL

6.1 Controlling the Inverter DC Bus Voltage

The capacitor voltage, U_C, is the voltage applied across the compensator output terminals depending on the states of the power switches. The compensation algorithm is based on the assumption that the capacitor voltage is always very close to the desired DC reference voltage. The algorithm performs capacitor voltage control by altering active current to insure that the capacitor voltage remains near the DC reference voltage.

When this compensation algorithm is applied the supply current, ***i'***, will be reduce to the working current, $\boldsymbol{i}_w$, therefore the compensator current will be equal to the difference in the load current and the working current. If one phase of a load were to draw the current as seen in the top of figure 6.1, then the compensator current for that phase, i_R would be as shown on the bottom of the same figure.

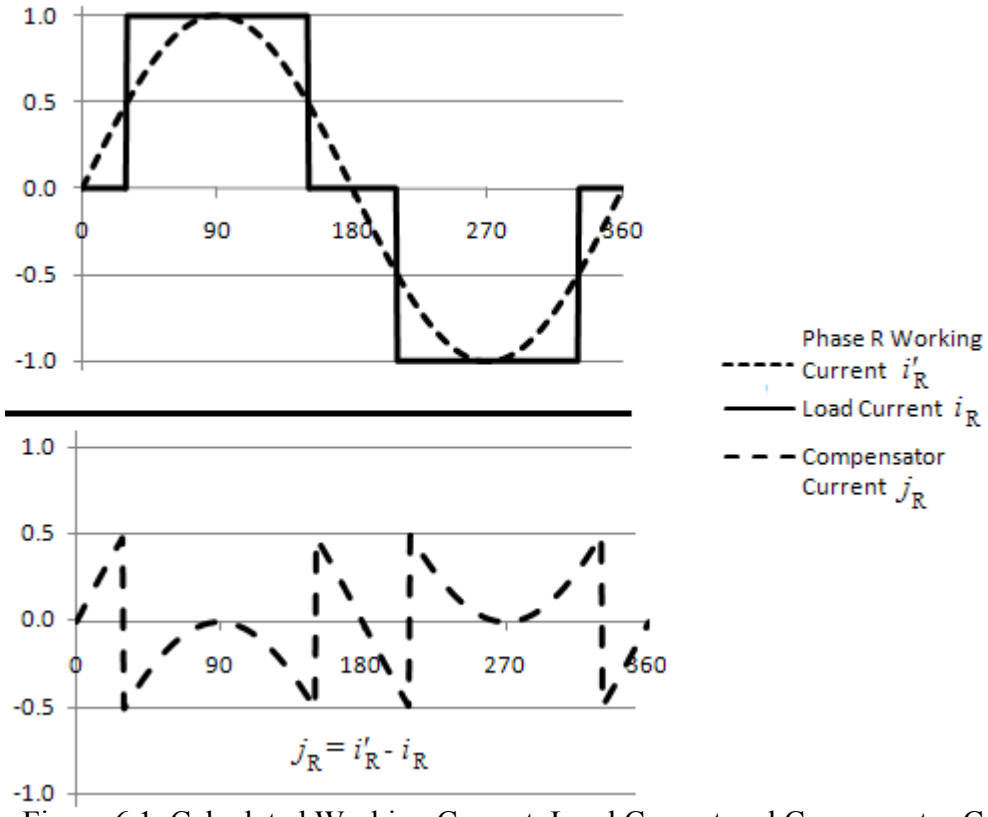

Figure 6.1 Calculated Working Current, Load Current and Compensator Current

In order to correct fluctuations in the capacitor voltage, the magnitude of the working current can be adjusted. If the magnitude of the working current, I_W, is increased, then the active current sent to the compensator will increase and the capacitor voltage will increase. Conversely, a decrease in the magnitude of the working current will reduce the active current sent to the compensator and the capacitor voltage will decrease as well. Figure 6.2 has the same load current as in figure 6.1, but the magnitude of the working current is increased. It can be seen looking at the bottom of figure 6.2 that the compensator current is similar to that in figure 6.1 but it now includes a positive active component, which will increase the capacitor voltage.

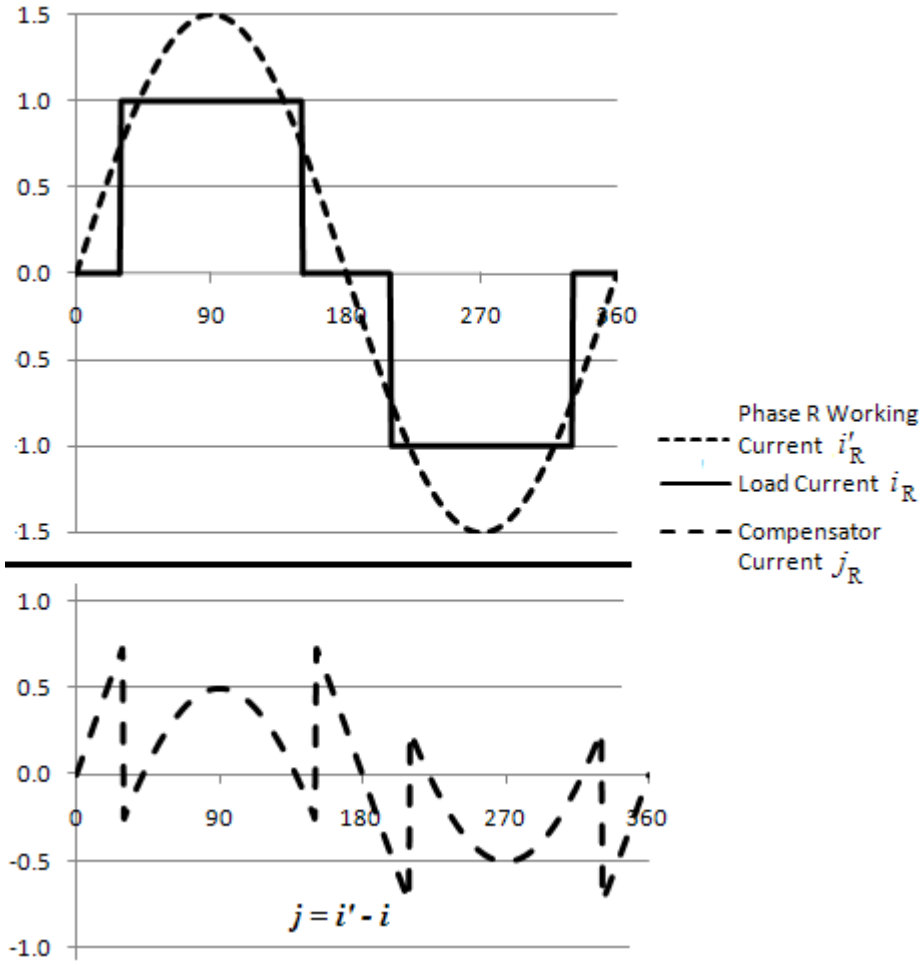

Figure 6.2 Adjusted Working Current, Load Current and Compensator Current

Once the magnitude of the working current, I_W, is calculated, it should be adjusted to include a component to correct the capacitor voltage. The adjusted magnitude, I_W', will include the difference in the capacitor voltage, U_C, and the DC reference voltage ,*Ur*, multiplied by a proportional gain as seen in the following formula.

$$I_W' = I_W + (Ur - U_C)g \tag{6.1}$$

The adjusted working current magnitude is used in calculating the reference signal in place of the working current magnitude calculated directly from the measured voltages and currents.

6.2 Reducing the Effects of a Cumulative Error

As discussed in section 4.2, there is running summation which can possibly accumulate an error when calculating the complex RMS values of the voltages and currents. The complex RMS values are used to calculate the working current. An error in these values will affect the value of the working current which will in turn affect the amount of active current the compensator draws from the supply. If the active current is affected, the capacitor voltage will change. The control for the capacitor voltage will measure a change and will adjust the magnitude of the working current accordingly.

The adjustment allows to compensator to operate normally even in the case of a large cumulative error, unless overflow occurs. To prevent overflow, the complex RMS values of the current are increased by the smallest possible amount when the capacitor voltage is too low and decreased by the smallest possible amount when the capacitor voltage is too high. To prevent overflow on the voltage complex RMS values, bounds must be set. The data acquisition elements are designed to operate within a certain range. The upper bound is the maximum value that can be measured, while the lower bound is a small margin below the lowest value at which the distribution voltage should operate.

CHAPTER 7. IMPLEMENTATION OF HARDWARE

7.1 The DSP Board

The algorithm for control of the switching compensator was implemented on a Motorola DSP56F807 evaluation mode DSP board. This is a 16 bit microcontroller capable of performing at 80MHz. There is 120KB of onboard program flash memory and can be expanded with 128 KB of external program and data memory. Because the board is an evaluation mode board, it can be programmed through a serial or parallel port and it is capable of sending information directly to a printer. The evaluation mode boards are more convenient for developing applications.

The structure of the DSP board, taken from reference [20] can be seen in figure 7.1.

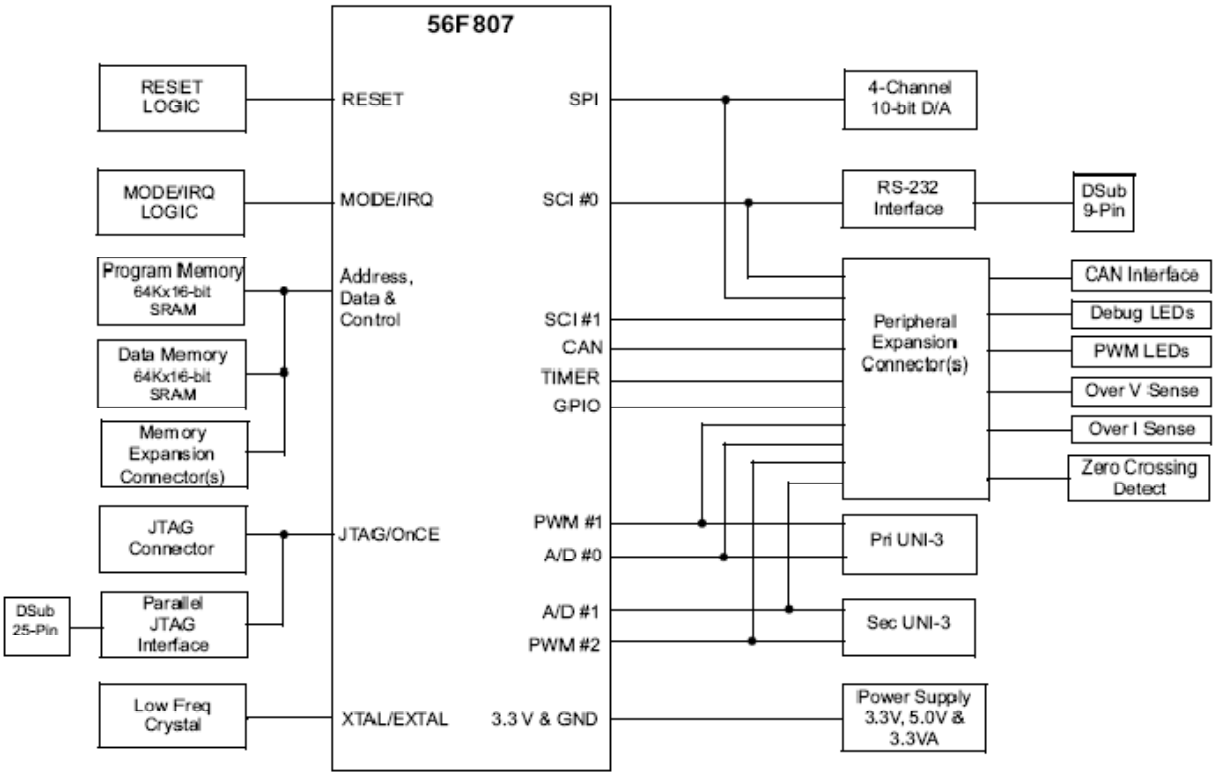

Figure 7.1 Basic Structure of the 56F807 DSP Board [20]

Although many peripherals are available, the only ones used for the algorithm are a multichannel analog to digital converter (ADC) and a multichannel Pulse Width Modulator (PWM) module. There were specific jumpers that pertained to the operation of each of these peripherals.

The ADCs have twelve bits of resolution and a minimum conversion time of 1.7μs. There are four ADCs and each one has eight single ended channels or four differential channels. There are five signals to measure and they were all measured using the single ended operation in order to avoid executing repetitious commands for two different ADCs. A conversion time of 3.4μs was selected based on trial and error. The higher the conversion time, the higher the accuracy, but a smaller conversion time leaves more time for other computations. Experiments suggested that accuracy began to plateau with the selected conversion time.

The required operation for the PWM module was to have three center-aligned complementary outputs with a period the same as the sampling time. To prevent a possible short circuit, a dead time must be inserted between the time a PWM signal turns off and the complimentary PWM signal turns on.

Part of the task to use the DSP board includes arranging the jumpers on the actual DSP board. There are over one hundred pairs of pins that would require a jumper for specific operations. For the given application, twenty-eight jumpers were used for various reasons. The combination of jumper locations falls within a commonly used arrangement. A diagram of the jumper locations, from [20], is provided in figure 7.2. Although many of the jumpers had no affect on the performance of the board, relative to the intended use of this thesis, the function of each jumper had to be checked to verify the functionality and prevent conflicts amongst the peripherals.

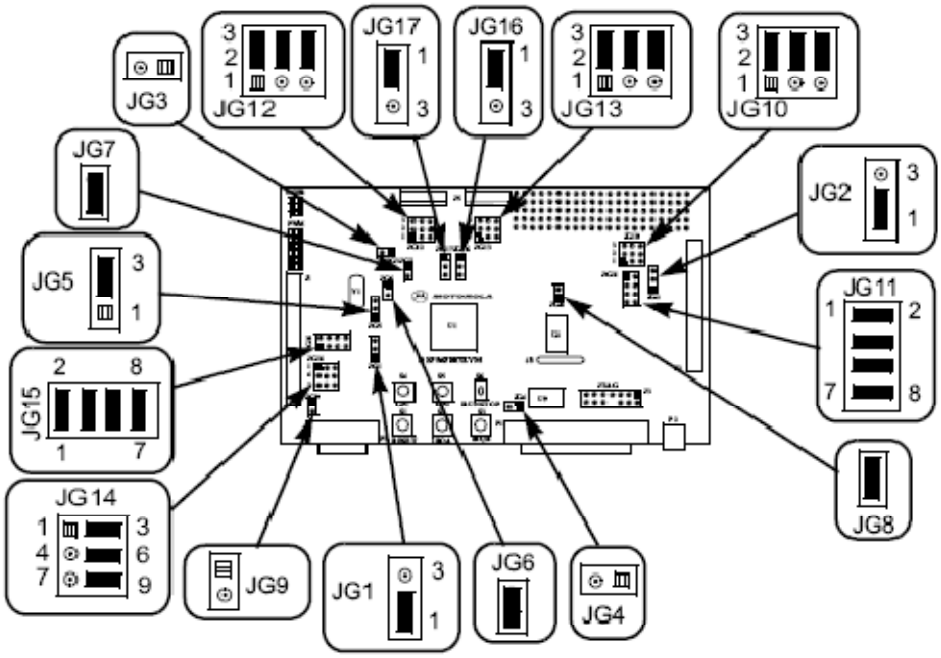

Figure 7.2 DSP Board Jumper Reference [20]

7.2 Additional Hardware

To perform the measurements, the voltage had to be stepped down to a level which could be safely read by the DSP board. The DSP board will read a maximum voltage of five volts peak, therefore the 120V RMS supply voltage was stepped down to ensure that the peak voltage did not exceed 4.8 volts. A resistive divider was used to step down the voltage to avoid a measurement error introduced by a potential transformer. Transformers will introduce a small phase shift between the voltage and current due to their inductive characteristics. Transformers will also attenuate voltage harmonics from the supply as well as inject harmonics due to nonlinearity of the core.

The current was measured using Hall effect based current sensors produced by Allegro Microsystems. The current sensors are rated for five amps of RMS current and output a voltage based on a supplied reference voltage proportional to the current. The current sensors have an

eight pin SOIC (Small Outline Integrated Circuit) package which had to be mounted to an adapter to fit the sensor onto an eight pin DIP (Dual In-line Package).

7.3 Hardware Adaptations

There were two issues that had to be resolved with hardware applications. The first one was to overcome the inability of the DSP board to measure negative voltages, therefore additional hardware was required to enable to board to measure bidirectional signals. The current sensors add a controllable DC component to their voltage output. The stepped down voltage signal however, has to include an op-amp circuit, as seen in figure 7.3, to add a DC component. A sufficiently positive DC component was selected to insure that the voltage signal always remains positive.

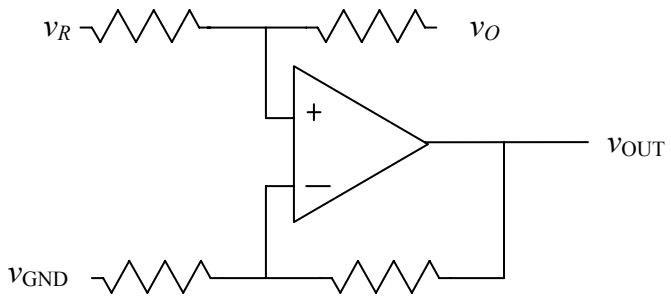

Figure 7.3 OP-AMP Circuit Used to Insert DC Offset

This circuit is used for each phase where v_O is the DC offset voltage and v_{GND} is the ground potential. Once the signals are sampled, the DC component is removed from the signal with a simple subtraction.

The second hardware adaptation was necessary to accurately measure the DC voltage on the storage capacitor. If resistive division is used and the stepped down value is supplied directly to the DSP board, then it will be referenced to ground. The voltage across the capacitor is very close to DC, but when measuring either the positive or negative terminal with respect to ground, there is an oscillating component. To correctly measure the capacitor voltage, a resistive divider

is used and an op-amp measures the voltage drop across the resistor as in figure 7.4. The output of the op-amp can then be supplied to the DSP board with respect to ground without oscillation.

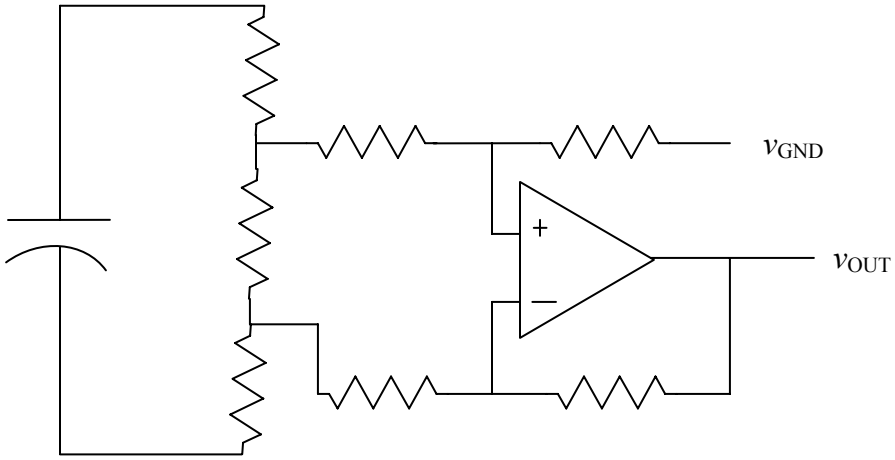

Figure 7.4 OP-AMP Circuit to Calculate Capacitor Voltage

CHAPTER 8. IMPLEMENTATION OF SOFTWARE

8.1 Overview of the Software

Figure 8.1 below is the flowchart for the compensation control algorithm.

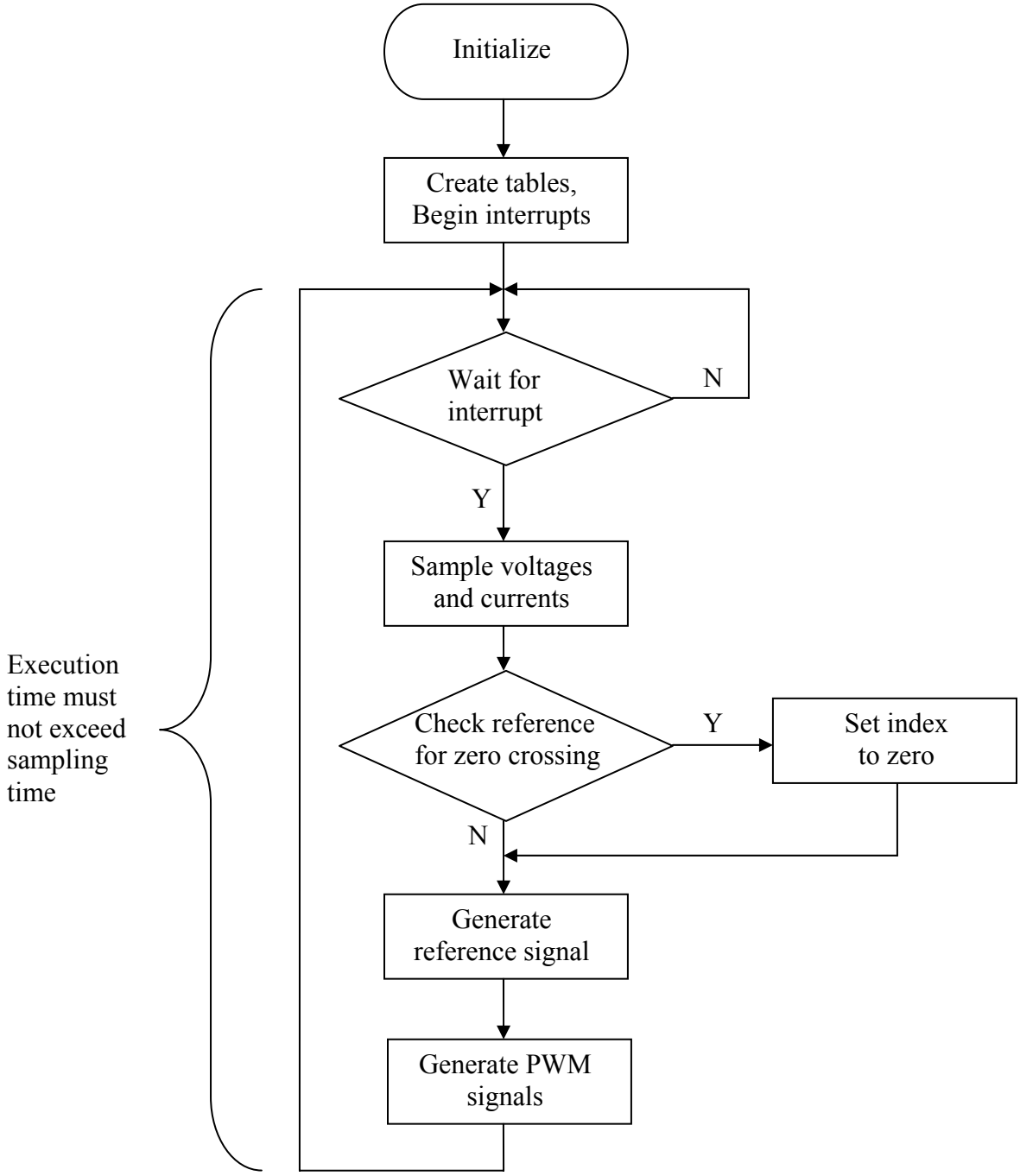

Figure 8.1 Flowchart for Compensation Algorithm

The flowchart briefly described the structure of the compensation control algorithm. The "Generate reference signal" block and the "Generate PWM signals" block are both complex blocks that require the majority of the time necessary to perform the compensator control. Both of these blocks could be expanded into long flowcharts, each of which would be more complicated than the flowchart in figure 8.1.

There were many challenges associated with developing the software while keeping the calculations computationally simple enough to maintain a sufficiently high sampling rate. All measurements and calculations must be performed in less time than what is available in between samples. In some cases, there are extra computations depending on the value of certain counters and flags. Some of the challenges and the steps to overcome them will be discussed in next section.

8.2 Developmental Software

The software used to program the DSP board is CodeWarrior 7.0©, which is developed by Metrowerks to enable users to write C based code with the aid of Java Beans. The C code is separated into two files. One file is the main code and the second file is the events file, certain conditions trigger an event which will execute the code associated with that event. The Java Beans are used to provide users with a graphical user interface with dropdown boxes instead of using text based code exclusively. Java Beans are used to define events, initialize peripherals and provide other conveniences to a user.

The first Java Bean used is the bean to control the processor. This bean allows a user to select the oscillator frequency, the clock speed, what memory to use and several other attributes. Figure 8.2 is a screenshot from Code Warrior 7.0©, which shows a list of beans on the left side. The right side of the figure is the properties which can be controlled using the bean. The dropdown boxes provide a list of selectable values and provide warnings when a conflict exists

between two or more selected values. The dropdown boxes and warnings greatly reduce the number of errors which frequently occur using text based programming.

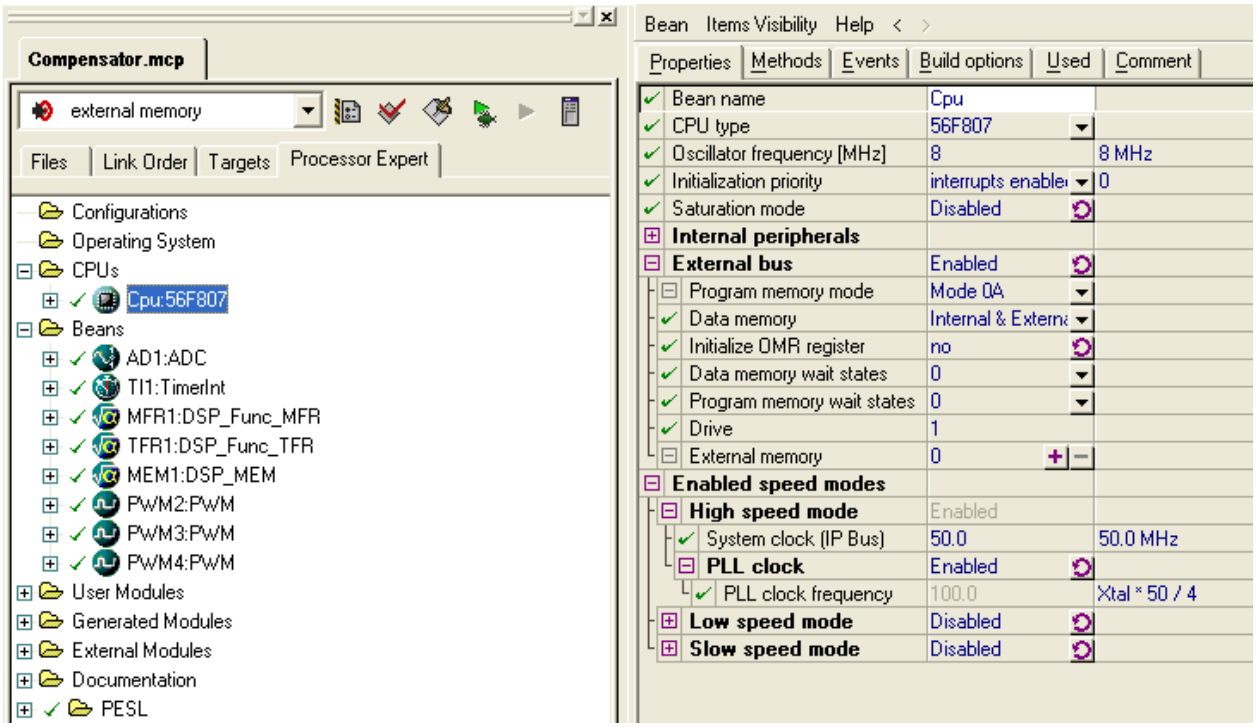

Figure 8.2 Code Warrior 7.0© Screenshot Showing Java Beans

The next Java Bean used was the periodic interrupt bean. The periodic interrupt was used to trigger events with a frequency of 10800Hz, which is 180 interrupts per period of the sixty hertz power signal. This event performed all periodic measurements and computations. The required parameters for this bean include a dedicated timer, a clock speed mode and an interrupt priority. All adjustable parameters for the periodic interrupt bean can be seen in figure 8.3. The bean also allows users to select which methods, code which is executed serially, and events, code which requires a specific event to execute, are available.

The other beans utilized for the development of the compensator control software are the ADC bean, the fractional math bean, three PWM beans and a trigonometric library bean. Three PWM beans were necessary to control each complimentary pair of PWM signals independently. The trigonometric library was necessary to initialize the lookup tables.

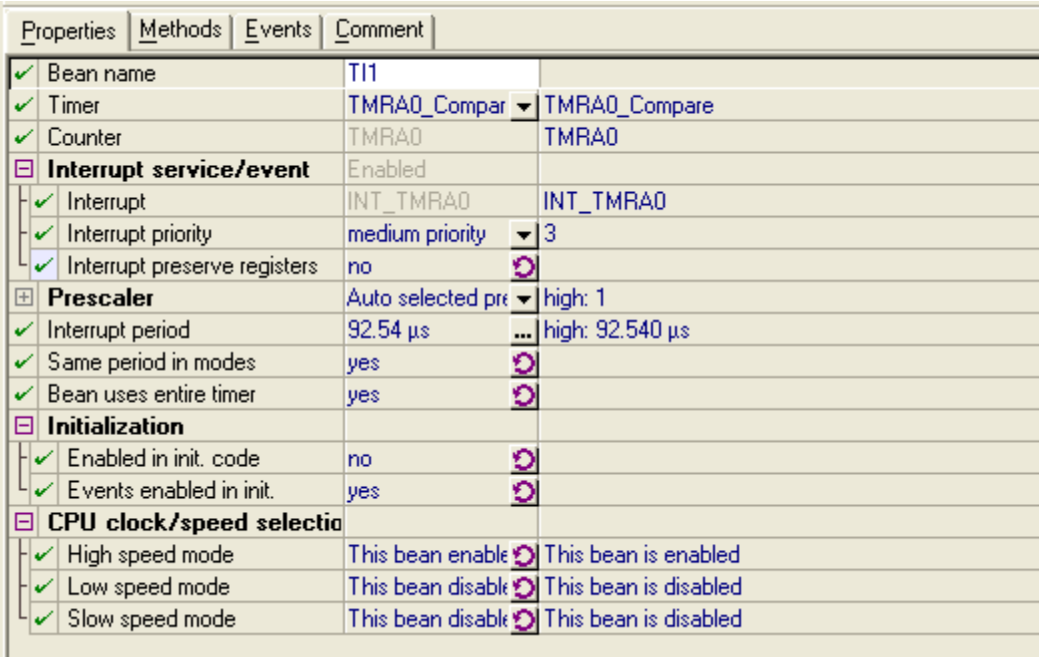

Figure 8.3 Code Warrior 7.0 Screenshot of Bean Settings

To have increased functionality, sometimes text based commands were necessary. There is a large library called the Processor Expert System Library or PESL, which includes C based commands to control every aspect of the DSP board. Some functions of the software were executed using PESL commands such as center aligning the PWM signals and inserting dead time into the complementary PWM signals.

8.3 Software Hurdles

The implementation of the theory and mathematics presented within this thesis brings forth many hurdles for real time compensation. The most common hurdle was to avoid floating point multiplications or divisions. Just two floating point multiplications are enough to exceed the time used by the entire algorithm. Because this is a very common problem when programming DSP boards, a fractional math library is made available to users. Instead of using decimal or base ten for representing fractions, the number one has a fractional value of 2^{15} or 32768 and any number between negative one and one is multiplied by 2^{15} to attain its fractional

value. This multiplication obviously cannot take place during the execution of the software, the decimal values must be converted to fractional numbers during development of the software. An additional consideration is decimal numbers greater than one have to be separated into two quantities. 2.5 for example must be considered an integer of 2 plus a fractional value of 16384.

Another hurdle in performing the necessary calculations is avoiding trigonometric functions. There are instances where the results of sine, cosine and tangent functions are needed but cannot be computed in the standard way. Lookup tables are used in place of the trigonometric functions to find all angles needed for calculations. To use a lookup table in place of a sine function, for example, requires dividing opposite by hypotenuse with a function from the fractional math library and expressing the result as a fractional number. The result is then compared to values stored in the table and when the closest value is found the corresponding angle is used. The tables have values for every two degrees, therefore the table produces a result with an accuracy of plus or minus one degree.

An additional problem arises when computing the angle of a tangent function using a lookup table. The fractional divide function will only produce results less than or equal to one, therefore when the opposite magnitude exceeds the adjacent magnitude it must be calculated separately. The tangent lookup table is split into two tables, one for opposite greater than adjacent and one for adjacent greater than opposite. When opposite is greater than adjacent it is divided by one hundred, then the fractional division is applied and the second tangent lookup table is used. If opposite is greater than adjacent after it is divided by one hundred, then the angle is set equal to eighty-nine degrees.

The final software hurdle to be discussed is overcoming the problem of noise creating a false negative to positive zero crossing during a positive to negative zero crossing. An example of this can be seen in figure 8.4, which is composed of actual measured values. In order to

prevent noise from creating a false negative to positive zero crossing on the DSP board, a counter is used to count the number of sampling interrupts since the last negative to positive zero crossing. The distributions system frequency can safely be assumed to be a near constant frequency and the interrupts are periodic, therefore a counter can count the number of periodic interrupts and not allow the DSP board to recognize a zero crossing until at least 270^{o} past the last negative to positive zero crossing.

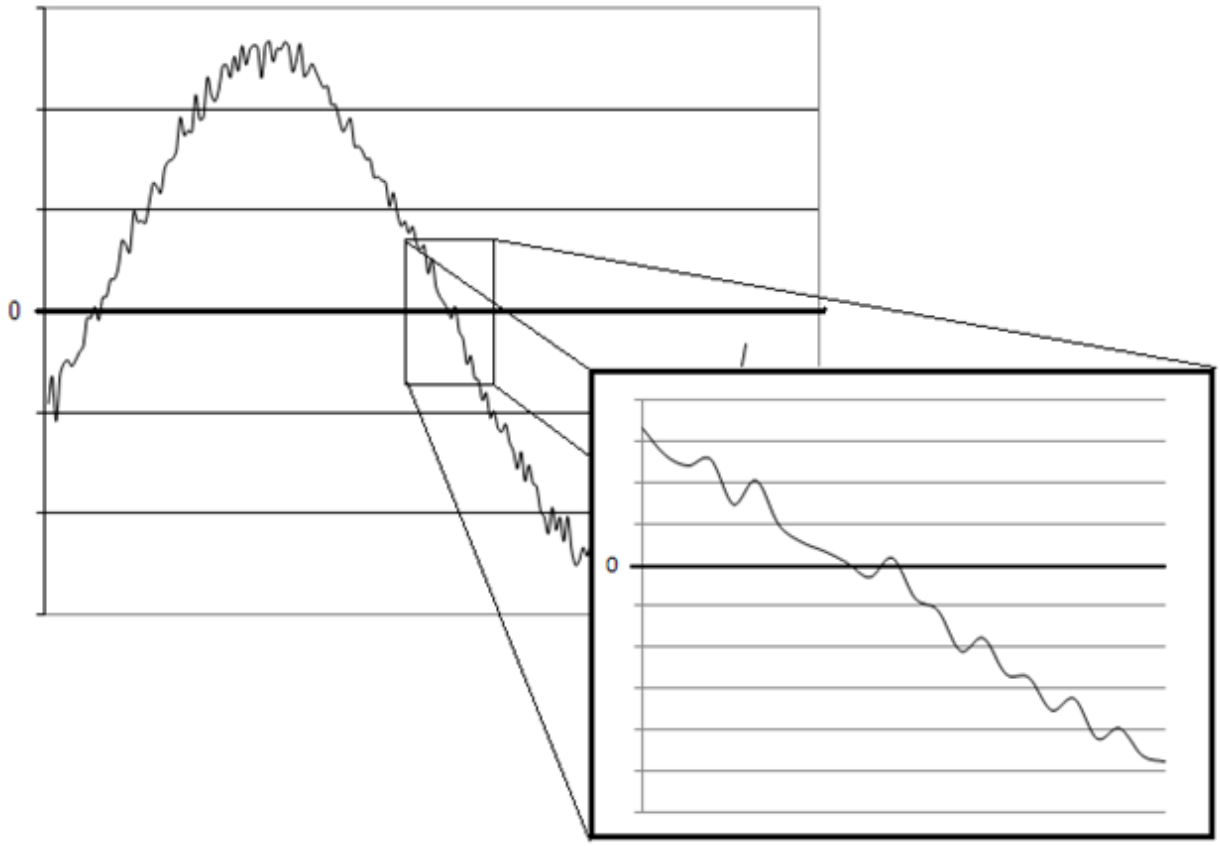

Figure 8.4 Noise Creating False Negative to Positive Zero Crossing

CHAPTER 9. CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

This thesis demonstrates that a CPC based compensation algorithm can be implemented to operate in real time with a sufficiently high sampling rate, a rate similar to what is possible using more popular Instantaneous Reactive Power *p-q* based compensators. This contradicts some opinions that CPC is too computationally demanding for real time compensation. Many details were provided to explain how the computational complexity was reduced enough to make a high sampling rate possible.

Using the proposed algorithm, a compensator will be able to compensate reactive current, harmonic current and unbalanced current. Unlike IRP *p-q* based compensators, the performance of this algorithm will not be reduced with supply voltage distortion and asymmetry.

9.2 Future Work

With the algorithm developed and the DSP board programmed accordingly, the next step is to interface the DSP board with a PWM inverter. Once the hardware and software are integrated, the software can be tested and the inputs and outputs can be scaled for the best possible accuracy. Once the hardware and software are complete, the performance can be analyzed with respect to loading quality, or how well the power factor is improved and how the efficiency of energy delivery changes.

The control algorithm works in an open loop because the load current is measured and the compensator injects current accordingly. A future consideration would be to implement a closed loop operation to insure that the injected current is measured and compared to the calculated value. The closed loop system could be expected to produce compensator current that more closely resembled the waveform of the reference signal.

Another future objective is compensator of active power variation. This would require observing the power in an interval much larger than one period and compensating variations from the median value. This type of compensator would require a much larger energy storage capacity than the compensator controlled by the algorithm developed in this thesis, a fly wheel for example could be used. A rock crusher is an example of a system that has large aperiodic active power variations. A compensator of active power variation could charge when load active power is below the average value and could discharge when the load active power is greater than the average value. If an active power compensator would release energy when a rock is being crushed and receive energy between large rocks, then the power and voltage fluctuations can be greatly reduced. One advantage of this type of compensation is reducing the annoying effects of voltage fluctuations, such as flickering lights. Another advantage when power is delivered without large fluctuations is reducing the energy losses in the transmission and distribution system.

The compensator proposed in this thesis, in conjunction with a compensator of active power variations could be very beneficial to a plant or factory. Industrial customers are billed based on power factor and peak demand, the combination of these two compensators could reduce the penalties for both of these quantities.

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APPENDIX

DEVELOPMENT OF STATE VECTORS

Development of state vectors, from unpublished literature by Dr. L.S. Czarnecki

Two-Level inverter is built of six power transistor switches, with a diode that provide a current path for the current of the opposite direction that can flow through transistor. A pair of such switches with symbols of components is shown in Fig. 17.6. Control of the inverter requires that there is a full control over ON-OFF switching. Transistors enable such full control, but only for one direction of the current, marked by the emitter arrow. Diodes are not controlled devices, however. One might have a doubt whether switches shown in Fig. 17.6 provide full ON-OFF control of a bidirec-tional current in the compensator output lines. Therefore, detailed analysis of such a switch would be desirable.

Symbols T^+ and T^- as well as D+ and D^- denote transistors and diodes connected to the positive (+) and negative (–) dc bars of the inverter. Symbols S^+ and S^- denote switching signals of transistors, with logical values 1 (transistor in ON state) and 0 (transistor in OFF state).

To avoid short circuit of the capacitor, the switches have to be controlled such that both of them cannot be in ON state at the same time, meaning the logic product of control signals has to be equal to zero

$$S^+ \cdot S^- \equiv 0 .$$

Figure 17.7. Combinations of switching signal values and the sign of output current

The change of the value of switching signals, S^+ and S^-, and the change of direc-tion of the output current *i*, creates six different combi-nations of the switch condi-tions, thus it operates in one of six different modes. These combinations are shown in Fig. 17.7. Observe, that to avoid situations that, due to transients, both switches are in the ON state, there have to be intervals of time, where both switching signals have zero value, thus Mode 2 and Mode 5 are needed.

Operation of the switch in particular modes is shown in Fig. 17.8. The purpose of the switch is connection, accor-ding to the value of the switching signal, the output line of the inverter to the positive or to the negative dc bus.

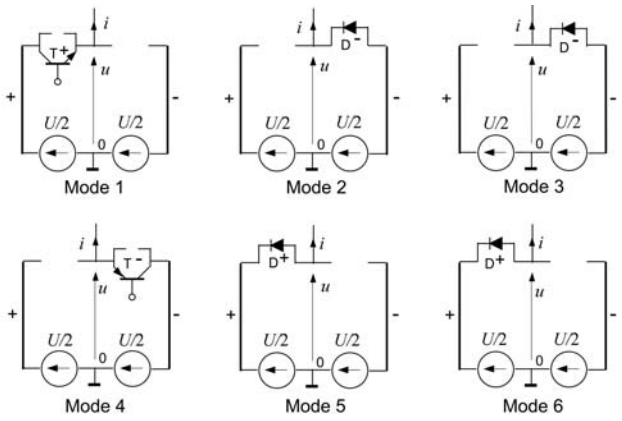

Figure 17.8. Modes of inverter switches operations

Current paths in Fig. 17.8 show that at positive output current *i*, the output line is connected to the negative bus before switching signal S^- is equal to 1, meaning in Mode 2. When this current is negative, the output line is connected to the positive dc bus before S^+ is equal to 1, meaning in Mode 5. Thus, in Modes 2 and 5 the output line is not connected to the dc buses according to the switching signal values. Therefore, these two modes, necessary for avoiding switching hazard, should be as short as possible.

Sequential switching of the inverter switches changes the state of the inverter as shown in Fig. 17.9

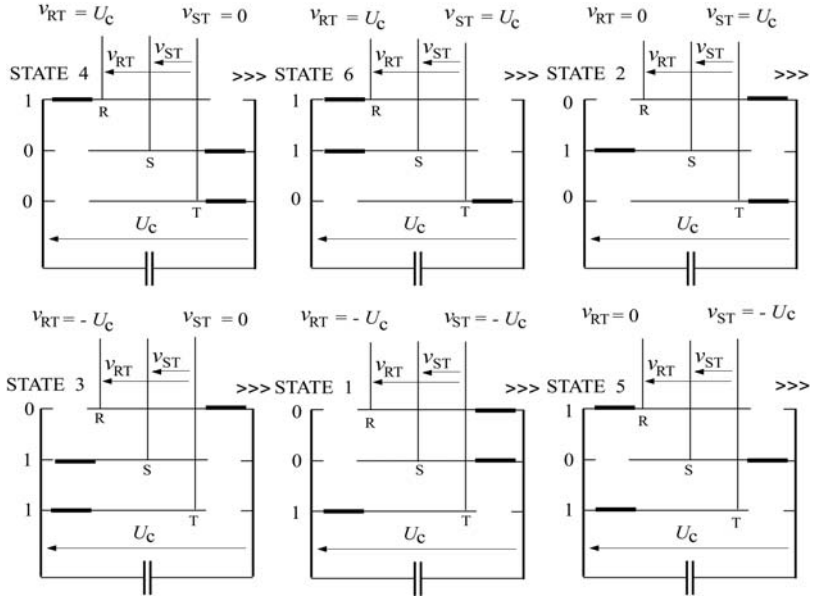

Figure 17.9. Inverter states

The logical state of transistors which connect terminals R, S and T to the positive dc voltage bus specifies the ***state of the inverter*** in a binary or in a decimal number. According to Fig. 17.9, with sequential switching of only one switch, the inverter proceed the state sequence

State 4 >> State 6 >> State 2 >> State 3 >> State 1 >> state 5 >> State 4 >>….. (..)

To produce zero voltage at the inverter output terminals, all swit-ches connected to the positive dc bus have to be in ON or in OFF states, as shown in Fig. 17.10. This creates two additional states of the inverter. Because the inverter output lines are short-circuit in that two state, these state can be referred to as ***short-circuit states***. One of these states can be reached with only one transistor switched ON at any instant of the switching sequence (..).

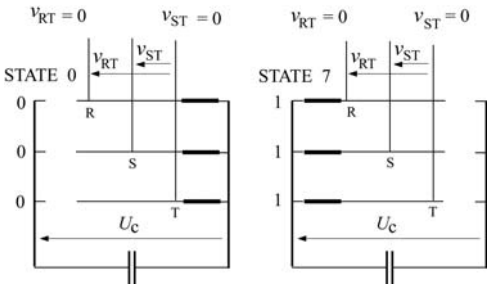

Figure 17.10. Short circuit states

The inverter output voltage $\boldsymbol{v}$ can have only seven values $\boldsymbol{v}_s$, where index s denotes the state decimal number, $\boldsymbol{v}_0$, $\boldsymbol{v}_1$, $\boldsymbol{v}_2$, $\boldsymbol{v}_3$, $\boldsymbol{v}_4$, $\boldsymbol{v}_5$, $\boldsymbol{v}_6$. The voltage in state 7, is equal to that in state 0, i.e., $\boldsymbol{v}_7 = \boldsymbol{v}_0 = \mathbf{0}$. The entries of vectors $\boldsymbol{v}_s$ in the line-to-line voltage form, meaning values of voltages v_{RT} and v_{ST}, are compiled in Figs. 17.9 and 17.10, respectively.

Since the output voltage of the inverter can have only seven discrete values, the Clarke Vector of this voltage, denoted generally by $\boldsymbol{V}^C(t)$, can have only seven values

$$\boldsymbol{V}_s^C = v_{s\alpha} + jv_{s\beta} = [1,\ j]\,\boldsymbol{v}_s^C = [1,\ j]\,\mathrm{D}\,\boldsymbol{v}_s = [1,\ j]\,\mathrm{D}\begin{bmatrix} v_{RT} \\ v_{ST} \end{bmatrix}_s$$

$$= [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} v_{RT} \\ v_{ST} \end{bmatrix}_s .$$

With this general expression, for sequential states of the inverter, we obtain

$$\boldsymbol{V}_1^C = [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} -U_c \\ -U_c \end{bmatrix} = \sqrt{\frac{2}{3}}U_c\, e^{-j120^0},$$

$$\boldsymbol{V}_2^C = [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} 0 \\ U_c \end{bmatrix} = \sqrt{\frac{2}{3}}U_c\, e^{-j60^0},$$

$$\boldsymbol{V}_3^C = [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} -U_c \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}}U_c\, e^{j180^0},$$

$$\boldsymbol{V}_4^C = [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} U_c \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}}U_c,$$

$$\boldsymbol{V}_5^C = [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} 0 \\ -U_c \end{bmatrix} = \sqrt{\frac{2}{3}}U_c\, e^{j60^0},$$

$$\boldsymbol{V}_6^C = [1,\ j]\begin{bmatrix} \sqrt{2/3}, & -1/\sqrt{6} \\ 0, & 1/\sqrt{2} \end{bmatrix}\begin{bmatrix} U_c \\ U_c \end{bmatrix} = \sqrt{\frac{2}{3}}U_c\, e^{j120^0}.$$

Thus, Clarke Vectors of the inverter output voltage $\boldsymbol{v}_s$ have the same magnitude

$$V^C = \sqrt{\frac{2}{3}} U_c ,$$

while different angles. The remaining two Clarke Vectors $\boldsymbol{V}_0^C = \boldsymbol{V}_7^C = \mathbf{0}$.

Clarke Vectors of the inverter output voltage $\boldsymbol{v}_s$ divide the complex plane into six polar sectors with the same angle of 60^0, as shown in Fig. 17.11.

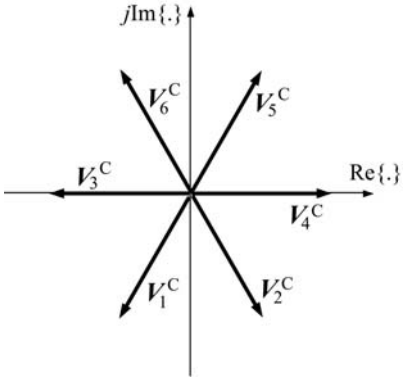

Figure 17.11. Clarke Vectors of the inverter output voltage $\boldsymbol{v}$

VITA

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