

2003

## Iddq testing of a CMOS 10-bit charge scaling digital-to-analog converter

Srinivas Rao Aluri

*Louisiana State University and Agricultural and Mechanical College*

Follow this and additional works at: [https://digitalcommons.lsu.edu/gradschool\\_theses](https://digitalcommons.lsu.edu/gradschool_theses)



Part of the [Electrical and Computer Engineering Commons](#)

---

### Recommended Citation

Aluri, Srinivas Rao, "Iddq testing of a CMOS 10-bit charge scaling digital-to-analog converter" (2003). *LSU Master's Theses*. 3314.

[https://digitalcommons.lsu.edu/gradschool\\_theses/3314](https://digitalcommons.lsu.edu/gradschool_theses/3314)

This Thesis is brought to you for free and open access by the Graduate School at LSU Digital Commons. It has been accepted for inclusion in LSU Master's Theses by an authorized graduate school editor of LSU Digital Commons. For more information, please contact [gradetd@lsu.edu](mailto:gradetd@lsu.edu).

# **$I_{DDQ}$ TESTING OF A CMOS 10-BIT CHARGE SCALING DIGITAL - TO - ANALOG CONVERTER**

A Thesis

Submitted to the Graduate Faculty of the  
Louisiana State University and  
Agricultural and Mechanical College  
in partial fulfillment of the  
requirements for the degree of  
Master of Science in Electrical Engineering

in

The Department of Electrical and Computer Engineering

by  
Srinivas Rao Aluri  
Bachelor of Engineering, Osmania University, Hyderabad, India, 2000  
December 2003

## **Acknowledgements**

I would like to dedicate my work to my parents, Mr. and Mrs. A.Sreedhar Rao and my brother Seshu, for their constant prayers and encouragement throughout my life.

I am very grateful to my advisor Dr. A. Srivastava for his guidance, patience and understanding throughout this work. His suggestions, discussions and constant encouragement have helped me to get a deep insight in the field of VLSI design.

I would like to thank Dr. P. K. Ajmera and Dr. Martin Feldman for being a part of my committee.

I am very thankful to Electrical Engineering Department, for supporting me financially during my stay at LSU.

I would like to thank my friend Miss. Chandra Srinivasan for her constant love and support for me through out my life.

I take this opportunity to thank my friends Anand, Uday, Vijay and Harish for their help and encouragement at times I needed them. I would also like to thank all my friends here who made my stay at LSU an enjoyable and a memorable one.

Last of all I thank GOD for keeping me in good health and spirits throughout my stay at LSU.

# Table of Contents

Acknowledgements .....	ii
List of Tables .....	v
List of Figures .....	vi
Abstract .....	x
Chapter 1: Introduction .....	1
1.1 Description of $I_{DDQ}$ .....	3
1.2 Reliability Benefits Derived from $I_{DDQ}$ .....	5
1.3 Literature Review.....	5
1.4 Chapter Organization.....	9
Chapter 2: The Digital-to-Analog Converter (DAC) Design .....	10
2.1 Performance Specifications of Digital-to-Analog Converter .....	12
2.2 Digital-to-Analog Converter Architectures .....	19
2.3 Digital-to-Analog Converter Operation.....	24
2.3.1 Capacitor Array Design .....	27
2.3.2 Operational Amplifier Design .....	30
2.3.3 A Two Stage CMOS Opamp Topology.....	33
2.3.4 Current Mirrors .....	33
2.3.5 Active Resistor.....	37
2.3.6 Unity Follower.....	45
2.3.7 Sample-and-hold circuit.....	47
2.3.8 The Transmission Gate Switch.....	50
2.3.9 The Storage Capacitor .....	51
2.4 10-bit Digital-to-Analog Converter .....	52
Chapter 3: Built-in Current Sensor Design .....	61
3.1 Current Testing in CMOS Integrated Circuits Using BICS.....	61
3.2 $I_{DDQ}$ Hardware.....	62
3.2.1 External $I_{DDQ}$ Testing .....	64
3.2.2 Internal $I_{DDQ}$ Testing .....	66
3.3 Physical Faults in CMOS Integrated Circuits .....	67
3.3.1 Open Faults .....	67
3.3.2 Bridging Faults.....	70
3.3.3 Gate-Oxide Short Defects .....	73
3.4 Definition and Description of $I_{DDQ}$ of a Faulty Circuit.....	73
3.4.1 Description of $I_{DDQ}$ of a Faulty Inverter .....	75
3.5 Design Considerations of BICS .....	77
3.5.1 Previously Proposed Schemes .....	77
3.5.2 The Design of the BICS .....	78
3.6 The Implementation of BICS.....	80

3.6.1	BICS in Normal Mode .....	80
3.6.2	BICS in Test Mode .....	82
3.6.3	Detailed Analysis of BICS .....	83
3.7	Layout, Simulation and Timing Diagrams for BICS .....	84
3.7.1	Current Mirror Circuit.....	84
3.7.2	Current Differential Amplifier .....	84
3.7.3	BICS.....	87
3.8	Fault Detection, Simulation and Testing .....	87
3.8.1	Fault-Injection Transistor.....	89
Chapter 4: Theoretical and Experimental Results .....		97
4.1	Simulation Results .....	97
Chapter 5: Conclusion and Scope of Future Work .....		121
Bibliography: .....		123
Appendix A: SPICE LEVEL 3 MOS Model Parameters for Standard n-well CMOS Technology .....		127
Appendix B: Chip Testability .....		129
Vita.....		136

## List of Tables

4.1	Theoretical and measured $I_{DDQ}$ for different fault types .....	119
4.2	Comparison of built-in-current .....	120

## List of Figures

1.1	Block diagram of $I_{DDQ}$ testing .....	4
1.2	Example of how $I_{DDQ}$ detects physical defects .....	6
2.1	Block diagram of a digital-to-analog converter .....	11
2.2	Basic Architecture of a DAC without the S/H circuit.....	13
2.3	DNL Characteristics of a 10-bit charge scaling DAC [19].....	14
2.4	INL characteristics of a 10-bit charge scaling DAC [19] .....	16
2.5	Offset in a DAC .....	17
2.6	Gain error in a DAC.....	18
2.7	A simple resistor string DAC.....	20
2.8	Current steering based DAC architecture .....	22
2.9a	Charge scaling DAC Architecture .....	23
2.9b	Equivalent circuit with MSB =1, and all other bits set to zero .....	23
2.10	Schematic block diagram of a 10-bit charge scaling DAC.....	25
2.11	Integrated Capacitance network, multiplexer switches and amplifier part of the circuit of Fig. 2.10 .....	26
2.12	Layout of a unit capacitance made of poly1 and poly2 used in the design .....	28
2.13	Layout of the capacitor array using unit capacitor configuration .....	29
2.14	Layout showing the use of dummy capacitors to match the capacitors present at the corner of the capacitor array .....	31
2.15	Block diagram for an integrated opamp.....	32
2.16	A CMOS operational amplifier.....	34
2.17	PMOS current mirror design.....	36
2.18	NMOS current mirror design .....	36

2.19	Layout of an operational amplifier design of Fig. 2.16 .....	40
2.20	Post-layout transfer characteristics of the circuit of Fig. 2.16 .....	41
2.21	Input and Output response of the amplifier circuit of Fig. 2.16 .....	42
2.22a	Frequency response characteristics of the circuit of Fig. 2.16 .....	43
2.22b	Phase response characteristic of the circuit of Fig. 2.16 .....	44
2.23	The non-inverting OPAMP configuration .....	46
2.24	The CMOS operational amplifier as a unity gain amplifier (follower) .....	48
2.25	Schematic diagram of a sample-and-hold amplifier .....	49
2.26	Sample and Hold CMOS circuit .....	54
2.27	Layout of a CMOS sample-and-hold circuit (S/H) circuit .....	55
2.28	Sample-and-hold circuit response .....	56
2.29	Schematic block diagram showing opamp, TG-switch, storage capacitor and unity gain buffer .....	57
2.30	Sample and hold response of circuit of Fig. 2.26 obtained from post layout SPICE simulations .....	58
2.31	Layout of a 10-bit charge-scaling DAC .....	59
2.32	DAC output response for all (0000000000 – 1111111111) combinations of the input digital word .....	60
3.1	Faulty ( $I_{DEF}$ ) and fault-free ( $I_{REF}$ ) $I_{DDQ}$ current .....	63
3.2a	Off-chip $I_{DDQ}$ current measurement using an automatic test equipment .....	65
3.2b	Off-chip $I_{DDQ}$ current measurement .....	65
3.3	Block diagram of $I_{DDQ}$ testing .....	68
3.4	Open circuit defect .....	69
3.5	Drain-source and inner-gate bridging faults in an inverter chain .....	71
3.6	Bridging defect .....	72



3.7a	Gate-oxide-short (GOS) in a MOSFET .....	74
3.7b	Equivalent circuit model. $R_S$ is the effective resistance of the short. B models the rectifying behavior of new current path introduced by the defect .....	74
3.8	Bridging fault causing $I_{DDQ}R_B$ drop and a path to the ground .....	76
3.9	CMOS built-in current sensor circuit.....	79
3.10	Built-in current sensor with CUT .....	81
3.11	n-MOS current mirror circuit.....	85
3.12	Schematic of a current differential amplifier .....	86
3.13	Layout of a built-in current sensor circuit.....	88
3.14a	Fault-injection transistor (FIT).....	91
3.14b	Fault-injection transistor between drain and source nodes of a CMOS inverter .....	91
3.15	Layout of a 10-bit DAC with BICS showing the defects induced in the CUT using fault-injection transistors .....	92
3.16	CMOS operational amplifier circuit with defect 1 introduced using a FIT .....	93
3.17	CMOS unity gain buffer circuit for S/H with defect 2 introduced using a FIT ....	94
3.18	CMOS MUX circuit with defect 3 introduced using a FIT .....	95
3.19	CMOS MUX circuit with defect 4 introduced using a FIT .....	96
4.1	CMOS chip layout of a 10-bit charge scaling DAC with four fault injection transistors distributed across the chip.....	98
4.2	MOS chip layout of a 10-bit charge scaling DAC including BICS within a padframe of $2.25\text{mm} \times 2.25\text{mm}$ size .....	99
4.3	Microchip photograph of 10-bit charge scaling DAC and BICS for $I_{DDQ}$ testing.....	101
4.4	Simulated and measured characteristics of a 10-bit charge scaling DAC .....	102
4.5	Measured DNL characteristics of a 10-bit charge scaling DAC.....	103
4.6	Measured INL characteristics of a 10-bit Charge Scaling DAC.....	104

4.7	Voltage gain response of op-amp with fault introduced .....	105
4.8	Transfer function of op-amp with fault ( $V_{E1}$ ) induced.....	106
4.9	Gain versus frequency response of the CMOS opamp circuit with fault introduced .....	107
4.10	Simulated output response of the multiplexer circuit of Fig 3.18 without defect.....	108
4.11	Simulated output response of the multiplexer circuit of Fig. 3.18 with fault activated.....	109
4.12	Simulated BICS output of the circuit of Fig 3.16 when Error-signal-1 for defect-1 is activated.....	110
4.13	Simulated BICS output of the circuit of Fig 3.17 when Error-signal-2 for defect-2 is activated .....	112
4.14	Simulated BICS output of the circuit of Fig. 3.18 when Error-signal-3 for defect-3 is activated.....	113
4.15	Simulated BICS output of the circuit of Fig.3.19 when Error-signal-4 for defect-4 is activated.....	114
4.16	CMOS circuit diagram of 10-bit charge scaling DAC with four fault injection transistors distributed across different parts of the circuit.....	115
4.17	Simulated BICS output with defects induced using fault injection transistors.....	116
4.18	HP 1660CS logic analyzer test results on a fabricated CMOS 10-bit charge scaling DAC showing the performance of BICS in normal and test modes.....	118
5.1	Block diagram of a sigma-delta ADC.....	122
B.1	Pin configuration of 10-bit DAC with BICS.....	134
B.2	Microchip photograph of 10-bit charge scaling DAC and BICS for $I_{DDQ}$ testing .....	135

## **Abstract**

This work presents an effective built-in current sensor (BICS), which has a very small impact on the performance of the circuit under test (CUT). The proposed BICS works in two-modes the normal mode and the test mode. In the normal mode the BICS is isolated from the CUT due to which there is no performance degradation of the CUT. In the testing mode, our BICS detects the abnormal current caused by permanent manufacturing defects. Further more our BICS can also distinguish the type of defect induced (Gate-source short, source-drain short and drain-gate short). Our BICS requires neither an external voltage source nor current source. Hence the BICS requires less area and is more efficient than the conventional current sensors. The circuit under test is a 10-bit digital to analog converter using charge-scaling architecture.

# Chapter 1

## Introduction

Conventional logic testing applied in digital circuits can detect faults, which can cause logic errors [1]. It, however, cannot detect several physical defects such as the gate-oxide shorts, floating gates and the bridging faults. These physical defects do not cause any logical error at the time of testing but can manifest into a fault at an early stage of the circuit life. Thus, circuits should also be tested for physical defects apart from logic errors. Though methods exist for testing digital circuits but testing of analog circuits is still a problem. Mixed signal circuits are even more difficult to test. A general and efficient solution for testing mixed-signal integrated circuits is still not available.

Functional test approach applied to test the functionality of analog and mixed-signal integrated circuits is based on empirical development of a test set [2, 3]. This approach needs a reasonably large number of sample circuits for collecting the test data. The approach also does not have any inherent test metric to measure the achievement of a test goal. Design for testability (DFT) is another widely used method [4]. Oscillation test strategy is based on the DFT technique [4, 5], which gives good fault coverage and does not require any test vectors. In this method, the complex analog circuit is partitioned into functional building blocks such as an amplifier, comparator, Schmitt trigger, filter, voltage reference, oscillator, phase-lock loop (PLL), etc., or a combination of these blocks. During the test mode, each building block is converted into a circuit that oscillates. The oscillation frequency,  $f_{osc}$  of each building block can be expressed as a function of its components or performances. The oscillation test method allows removing the analog test vector generator and output evaluators, and consequently reduces the test

complexity, area overhead, and test cost. However, the method suffers from performance degradation in complex integrated circuits since it is not usually possible to divide the circuit into the fundamental blocks. Built in self-test (BIST) method is based on measuring the output data and calculating the performance of the system using an on-chip circuitry [6,7]. This method reduces testing complexity of mixed-signal integrated circuits by incorporating all or some of the testing circuitry on the silicon. An important component of a mixed-signal BIST is a precision analog signal generator required for on-chip stimulation. While the area overhead is kept to a minimum, these generators should be capable of synthesizing high-precision single-and multitone signals with controllable frequency and amplitude. This method also suffers from performance degradation and does not cover physical defects.

The steady state or quiescent current ( $I_{DDQ}$ ) testing of CMOS integrated circuits is known to be very efficient for improving test quality [8, 9]. The test methodology based on the observation of the quiescent current on power supply lines allows a good coverage of physical defects such as gate-oxide shorts, floating gates and bridging faults. These defects are neither well modeled by the classical fault models, nor detectable by conventional logic tests. In addition,  $I_{DDQ}$  testing can be used as a reliability predictor due to its ability to detect defects that do not yet involve faulty circuit behavior, but could be transformed into functional failures at an early stage of circuit life. Thus,  $I_{DDQ}$  testing became a powerful complement to the conventional logic testing. In analog circuits, the quiescent current, termed as  $I_{PS}$  may be in the order of  $\mu A$ 's or  $mA$ 's [10]. Under the fault conditions, the normal values of  $I_{PS}$  may be increased, decreased or generally

distorted. Thus, fault detection can be accomplished by monitoring the  $I_{PS}$  current fluctuations using a current sensing circuit.

In this thesis, a simple built-in current sensor (BICS) is presented, which provides a digital output for supply current monitoring and testing in mixed-signal circuits. The proposed BICS is based on current differential amplifier architecture providing a digital output proportional to the  $I_{DDQ}$  ( $I_{PS}$ ) current of the circuit under test. BICS is inserted in series with the power supply or the ground of the CUT to detect abnormal  $I_{DDQ}$  current in the integrated circuit [5] as shown in Fig. 1. The new BICS requires less area and has less performance degradation than reported earlier [11-18]. Furthermore, BICS requires neither an external voltage reference nor a current reference since the reference is generated on chip. It only requires two extra control pins, which control the mode of operation of the BICS and one output pin. The proposed BICS has been designed to test a 10-bit charge scaling digital-to-analog converter (DAC) [19].

### **1.1 Description of $I_{DDQ}$**

$I_{DDQ}$ 's definition is the current that flows in the CMOS circuit under quiescent (steady state) operating condition. Any current above the quiescent current would indicate the presence of physical defects in the circuit. Figure. 2 shows how an  $I_{DDQ}$  test can identify physical defects.  $Q_4$  has a defect that causes a resistive path between its gate and source. When  $V_{IN}$  is logic '1' level, the gate and the source of  $Q_4$  are held at ground by  $Q_2$ , which prevents the flow of any  $I_{DD}$  current [20]. When  $V_{IN}$  switches to a logic '0' level,  $Q_4$ 's gate is pulled high by  $Q_1$ . This allows the current to flow from  $V_{DD}$  through the defective path to ground.

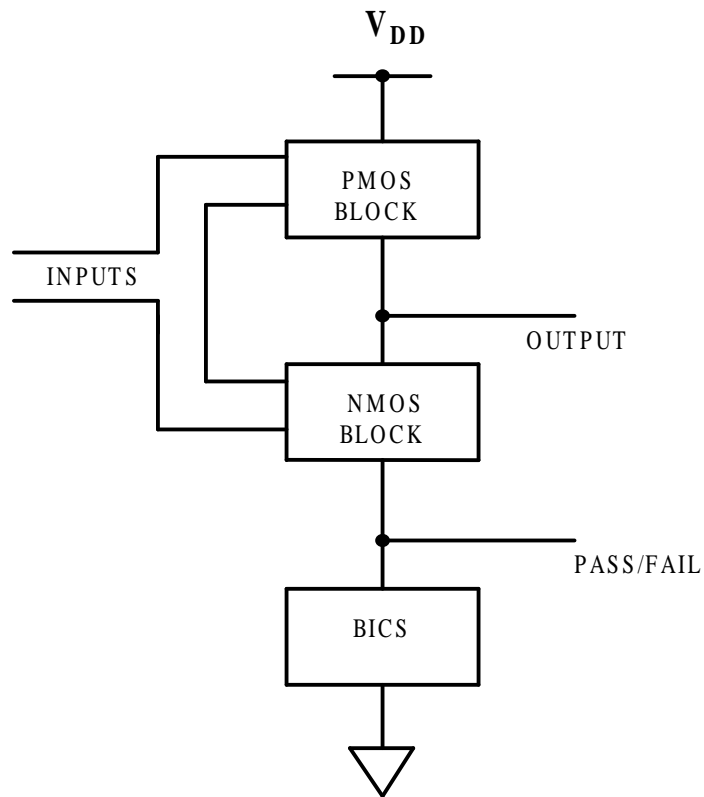


Figure 1.1: Block diagram of  $I_{DDQ}$  testing.

## 1.2 Reliability Benefits Derived from $I_{DDQ}$

$I_{DDQ}$  testing has been shown to identify gate oxide shorts (GOS). Many of these gate oxide shorts do not initially cause a functional failure but over the time they can deteriorate until functionality is affected. To quantify this effect, Ford Microelectronics Inc. (FMI) conducted a life test study on  $I_{DDQ}$  failures for ASIC's, recording leakage current instability [20]. It was theorized that any instability could be used as a leading indicator for predicting component reliability. After 48 hours of life testing, the ASIC components passed all burn-in, hot and cold functional testing, and parametric testing but failed for  $I_{DDQ}$ . The circuit under test (ASIC components) had  $I_{DDQ}$  values ranging from 0  $\mu A$  to greater than 100  $\mu A$  [20]. This experiment was repeated and verified on similar devices. Failing  $I_{DDQ}$  does not necessarily result in non-functional behavior. However, data is available, which confirms a significant number of  $I_{DDQ}$  failures will result in reliability problem [20]. Life test studies conducted at FMI have shown a statistically significant number of  $I_{DDQ}$  failures have become inoperative over time [20]. This life test experiment studied the effect of  $I_{DDQ}$  values versus product reliability.

## 1.3 Literature Review

In the following section a brief review of the selected works on  $I_{DDQ}$  testing are described which are used to compare with the present work

- Maly and Patyra's design [13]: The main idea is to make use of a differential amplifier with a reference voltage at the non-inverting node and the current-related voltage at the inverting node. Two clocks  $\phi_1$  and  $\phi_2$  are used to control when to sample the data. The importance of minimizing the impact of BICS on the performance of the CUT is taken into consideration. Hence a lateral NPN BJT



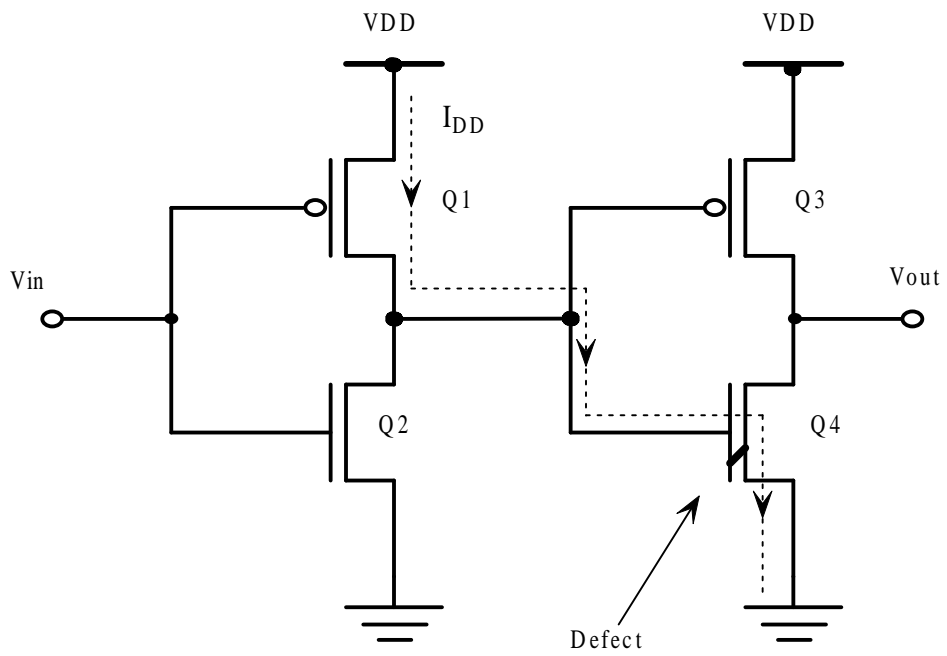


Figure 1.2: Example of how  $I_{DDQ}$  detects physical defects.

- is used to supply a large current with an allowable drop [13,18]. Due to the exponential characteristic of the BJT, this design [13] also enhances the  $I_{DDQ}$  detectability even when the abnormal current is little more than steady state current. However, the requirement of external voltage reference, double clocks, and lateral NPN BJT make this design difficult to implement.
- Favalli et al. design [14]: In this design, each gate requires two extra transistors and the whole circuit requires other transistor (see Fig. 3 of [14]). All these transistors are used to convert analog faults to stuck-at faults. A selection line is used to switch between normal mode and test mode. The design is easy to implement since it uses only digital circuits. However, the area overhead is quite high since each gate requires two additional transistors.
- Miura and Kinoshita's design [15]: The design consists of a V-I translator, a level translator and a integrator circuit. The V-I translator transforms the current of a given CUT to a corresponding voltage. The level translator transforms the output voltage of the V-I translator to an appropriate logic value. The integrator circuit produces a faulty signal when the faulty logic generated by the level translator lasts for certain time intervals. This BICS itself can be tested by applying an external current source to the special ground pin  $N_{GND}$  (Fig.1 of [15]).
- Shen et al. design [16]: The design is similar to the comparator circuitry (the differential amplifier) of Ref.15 and consists of a differential amplifier (comparator) circuit and an output circuit. A clock generator is used to generate a two-phase clock CLK1 and CLK2 so that the transient current can be bypassed. A diode is used to limit the voltage drop on the sensing device. The comparator

circuit compares the externally generated  $I_{REF}$  with  $I_{DDQ}$  from the CUT. Through proper sampling in the steady state, a PASS/FAIL flag is then detected from the output circuit. This scheme may still degrade the circuit since the cut-off voltage 0.6V of the diode may be too high when compared to the low level output voltage  $V_{OL} = 0.5V$ . The design also requires external current reference and a two-phase clock generator.

- Verhelst's design: By employing the “virtual short” property of an OP-AMP the voltage drop on BICS is further reduced. The current supplied by the CUT passes through the current sensing transistor  $T_s$ . This current is compared with the reference current. Since the transistor,  $T_s$  operates in the linear region, less current can be provided for a given device dimension. Thus, even if the voltage stability is increased, the current supply capability is limited. An external current reference is also needed. [See U.S. patent 5057774, Oct. 15, 1991 by S.C. Verhelsts, E. Seevinck and K. Baker, “ Apparatus for measuring the quiescent current of an integrated monolithic digital circuits” referred in J.J. Tang, K.J. Lee and B.D. Liu, “ A practical current Sensing Technique for  $I_{DDQ}$  Testing,” IEEE Trans. on Very large Scale Integration (VLSI) Systems, vol.3, No.2, June 1995, pp.302-310].

Methods have been developed to test integrated circuits based on dynamic supply current ( $I_{DD}$ ) measurement [21], on-line power dissipation measurement and  $I_{DDQ}$  testing [22] and on-chip transient current measurements [23-26]. Current sensors have been proposed for analogue applications [22]. In [22], the sensor design is based on a series voltage regulator, in which a series transistor is connected between the supply and the

(CUT). One drawback is the area required to realize this serial transistor since it has to sink all the current to the CUT.

## **1.4 Chapter Organization**

In the following chapters, the methodology, circuit design and technology considerations, transient simulations, post layout measurements and experimental results are discussed.

**Chapter 2** explains the basic structure and operation of a 10-bit charge scaling digital to analog converter (DAC).

**Chapter 3** explains concept of  $I_{DDQ}$  testing, design and implementation of a built-in current sensor. The mechanism of fault simulation and fault detection in a 10-bit charge scaling using the BICS is explained.

**Chapter 4** describes the simulation result and design considerations of each module of 10-bit charge scaling DAC. Simulations results of each module of the DAC are included. It also describes the simulation results for each module of the built-in current sensor. Finally, a description of the abnormal current behavior and fault detection in the DAC is explained and simulation results are included. Experimental results of the fabricated device are presented, compared with simulations. Results are also compared with the published work.

**Chapter 5** provides a summary of the work presented and scope for future work.

The MOS model parameters used for design is presented in Appendix A. The entire chip testing procedure is presented in Appendix B.

## Chapter 2

### The Digital –to- Analog Converter (DAC) Design

The ability to convert digital signals to analog and vice versa is very important in signal processing. The digital-to-analog conversion is a process in which digital words are applied to the input of the DAC to create from a reference voltage an analog output signal that represents the respective digital word. In this conversion process, an N-bit digital word is mapped into a single analog voltage. Typically, the output of the DAC is a voltage that is some fraction of a reference voltage, such that [27-29].

$$V_{OUT} = F V_{REF} \quad (2.1)$$

Where  $V_{OUT}$  is the analog voltage output.  $V_{REF}$  is the reference voltage. F is the fraction defined by the input word, D, that is N bits wide. The number of input combinations represented by the input word D is related to the number of bits in the word by

$$\text{Number of input combinations} = 2^N \quad (2.2)$$

The maximum analog output voltage for any DAC is limited by the value of some reference voltage  $V_{REF}$ . If the input is an N-bit word, then the value of the fraction, F, can be determined by,

$$F = \frac{D}{2^N} \quad (2.3)$$

Figure. 2.1 shows a conceptual block diagram of a DAC converter. The inputs are a digital word of N-bits ( $b_1, b_2, b_3 \dots b_N$ ) and a reference voltage,  $V_{REF}$ . The voltage output,  $V_{OUT}$ , can be expressed as

$$V_{OUT} = KV_{REF}D \quad (2.4)$$

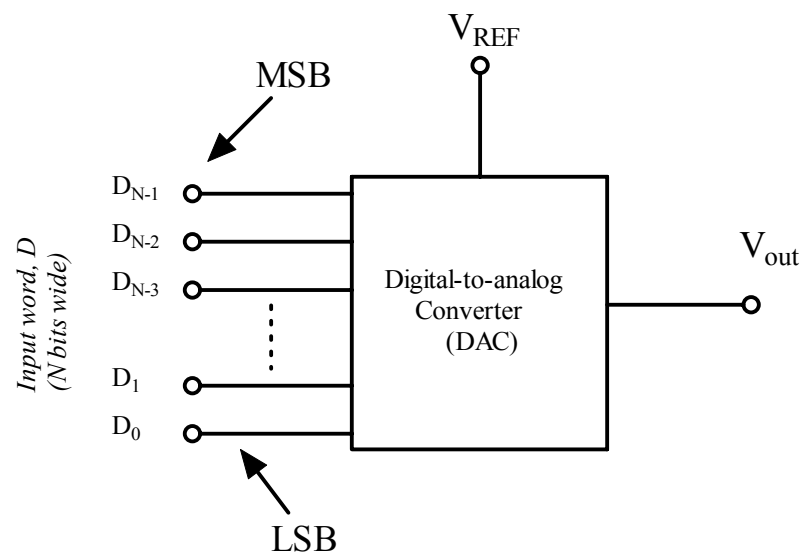


Figure 2.1: Block Diagram of a digital-to-analog converter

Where K is a scaling factor and the digital word D is given by

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \dots + \frac{b_N}{2^N} \quad (2.5)$$

N is the total number of bits of the digital word, and  $b_i$  is the  $i^{\text{th}}$  coefficient and is either 0 or 1. Thus, the output of a DAC can be expressed by combining Eqs. 2.4 and 2.5 to get

$$V_{\text{OUT}} = K V_{\text{REF}} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \dots + \frac{b_N}{2^N} \right) \quad (2.6)$$

The basic architecture of a DAC without a sample and hold circuit at the output is shown in Fig. 2.2. The various blocks are a voltage reference, which can be supplied externally, binary switches, a scaling network, and an output amplifier. The voltage reference, binary switches, and scaling network convert the digital word as either a voltage or current signal, and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of conversion.

## 2.1 Performance Specifications of Digital-to-Analog Converter

The following are some of the important static and dynamic performance parameters used to characterize a DAC [27-29].

- **Differential Nonlinearity (DNL)**

The DNL gives a measure of how well a DAC can generate uniform analog LSB multiples at its output. It is defined as follows

$$\text{DNL}_n = (\text{actual increment height of transition, } n) - (\text{ideal increment height}).$$

Where ‘n’ is the number corresponding to the digital input transition. DNL is illustrated in Fig. 2.3.

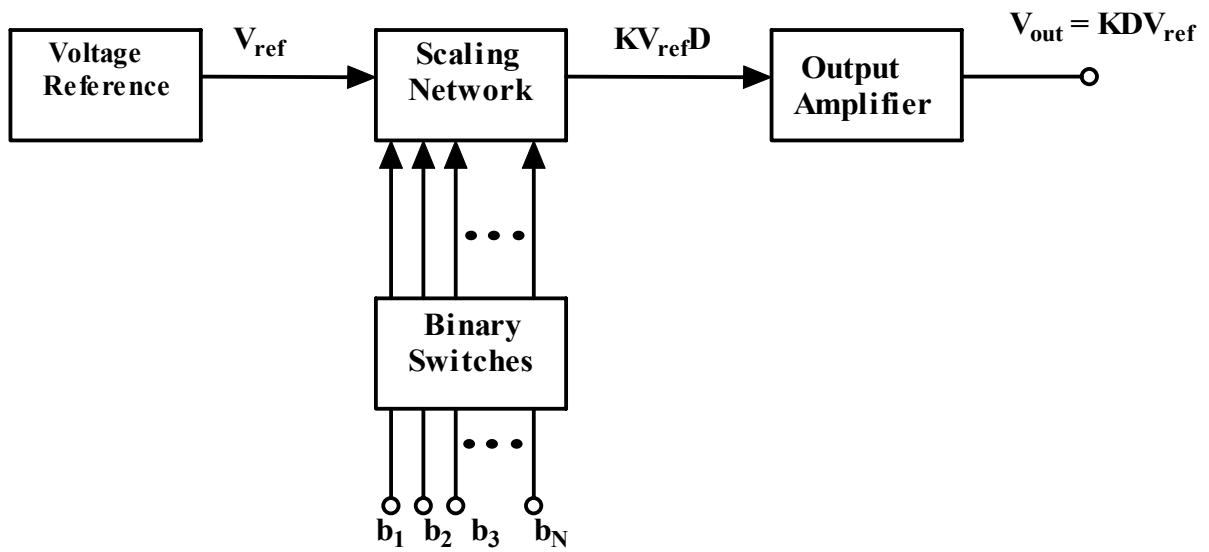


Figure 2.2: Basic Architecture of a DAC without the S/H circuit.



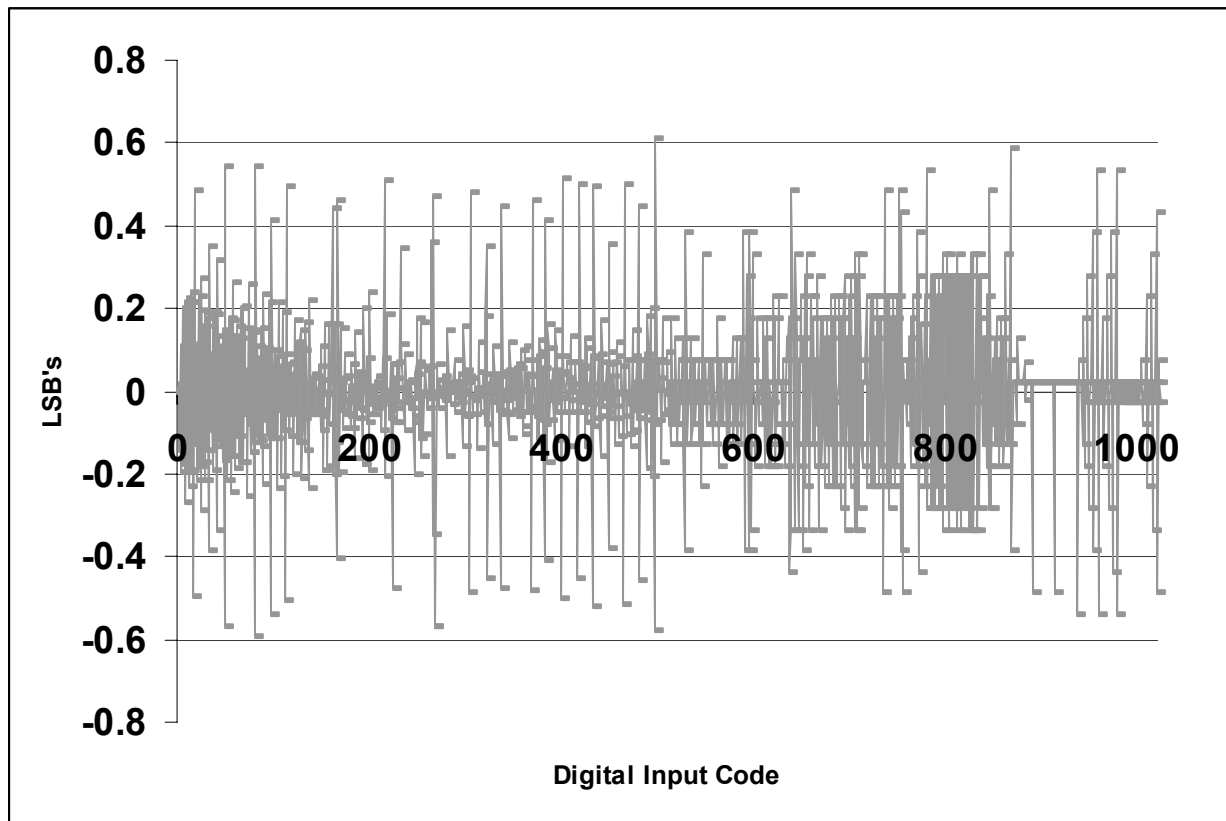


Figure. 2.3: DNL Characteristics of a 10-bit charge scaling DAC [19].

- **Integral Nonlinearity (INL)**

Another important static characteristic of a DAC is called integral nonlinearity (INL). It is defined as the difference between the data converter output values and a

reference straight line drawn through the first and last output values as shown in Fig. 2.4.

INL defines the linearity of the overall transfer curve and can be described as follows.

$INL_n = (\text{output value for the input code, } n) - (\text{output value of the reference line at the point}).$

- **Offset**

Offset of the DAC is defined as the amount of shift in the transfer characteristics when the digital input code  $D = 0$ . This shift is similar to the offset voltage for an operational amplifier. It is shown in Fig. 2.5.

- **Gain Error**

Gain Error is defined as the difference between the ideal slope and the actual slope of the transfer characteristics. It is described as follows and shown in Fig. 2.6.

$$\text{Gain Error} = (\text{ideal slope} - \text{actual slope})$$

- **Dynamic Range**

Dynamic range is defined as the ratio of the largest analog output value (Full Scale (FS)) to the smallest analog output value. The dynamic range in decibels is given by,

$$DR = 20 \log (2^N - 1) \text{ dB.} \quad (2.7)$$

For our design, which is a 10bit, charge-scaling DAC, the dynamic range is 60.19 dB.

- **Resolution**

It is described as the smallest change in the analog output with respect to the value of the reference voltage  $V_{REF}$ . The resolution is given by [29]

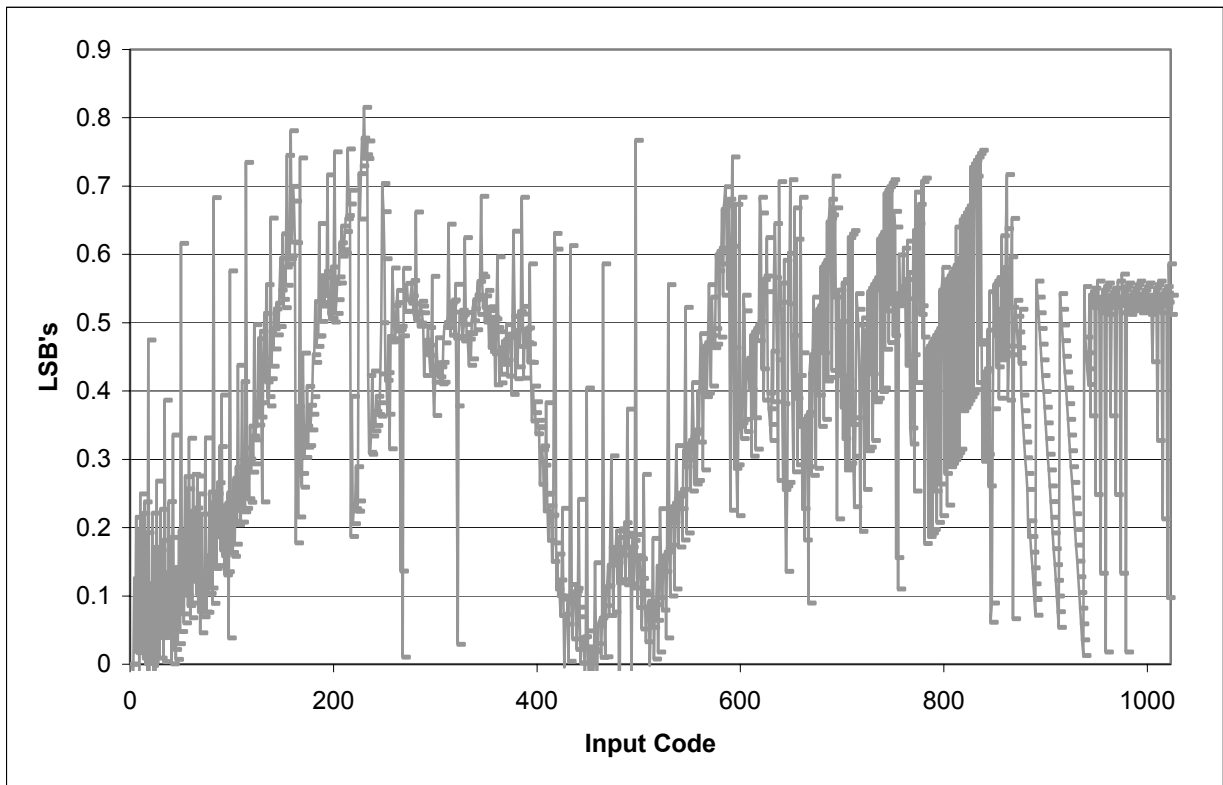


Figure.2.4: INL characteristics of a 10-bit charge scaling DAC [19].

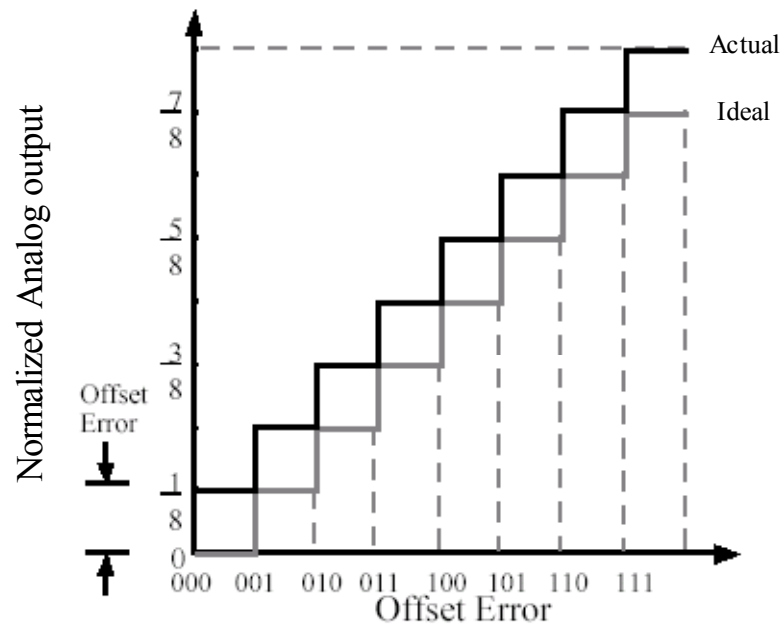


Figure 2.5: Offset in a DAC.

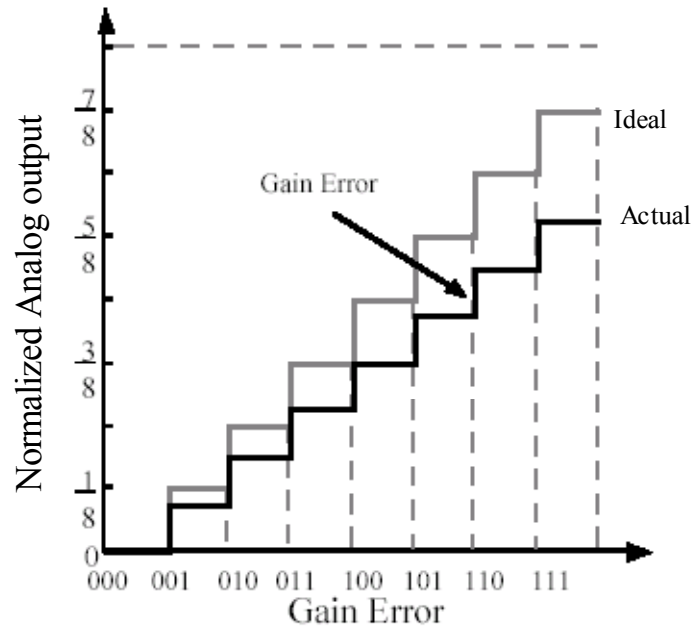


Figure 2.6: Gain error in a DAC.

$$\text{Resolution}(N) = \log_2 \left( \frac{V_{REF}}{1LSB} \right) = \log_2 \left( \frac{2V}{1.9mV} \right) = 10 \text{ bits.} \quad (2.8)$$

## 2.2 Digital-to-Analog Converter Architectures

A wide variety of of DAC architectures exist, ranging from very simple to complex. Each of course, has its own merits. There are primarily three architectures of DAC namely-

- Resistor String
- Current Steering
- Charge Scaling

- **Voltage Division**

In this architecture, the analog output voltage is divided uniformly among the resistor string as shown in Fig. 2.7 [27]. Depending on the input digital word, the switches shown close or open if the input is a ‘high’ or ‘low’ voltage, respectively. The analog output is simply the voltage division of the resistors at the selected tap. The value of the voltage at the tap associated with the  $i^{\text{th}}$  resistor is given by [27]

$$V_i = \frac{(i).V_{REF}}{2^N}, \text{ for } i = 0, 1, 2, \dots, 2^{N-1} \quad (2.9)$$

This architecture typically results in good accuracy, provided that no output current is required and that the values of the resistors are within the specified error tolerance of the converter. Another problem with this architecture is the balance between the area and power dissipation. So this architecture is not suited for high resolution DAC’s.

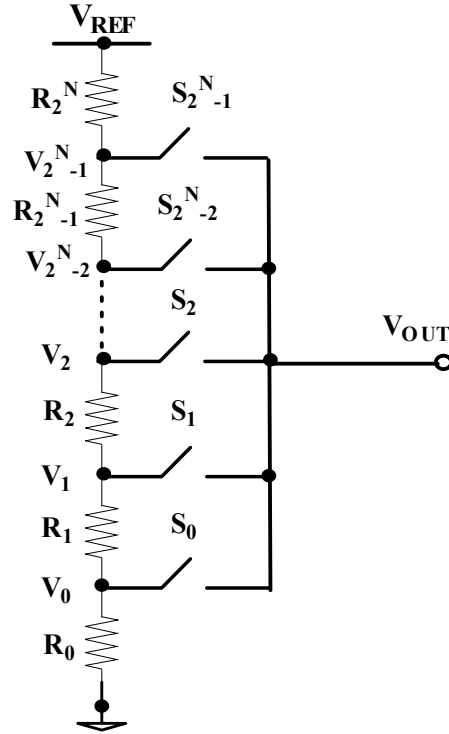


Figure 2.7: A simple resistor string DAC.

- **Current Steering**

The current steering based DAC architecture is shown in Fig. 2.8 [27]. This DAC architecture uses current through out the conversion known as current steering. This type of DAC requires precision current sources that are summed in various fashions. Since there are no current sources generating  $i_{OUT}$  when all the digital inputs are zero, the MSB,

$D_2^{N-2}$ , is offset by two index positions instead of one. The binary signal controls whether or not the current sources are connected to either  $i_{out}$  or GND. The output current  $i_{out}$  has the range of

$$0 \leq i_{out} \leq (2^N - 1) \cdot I \quad (2.10)$$

One advantage of the current steering DAC's is the high-current drive inherent in the system. Of course, the precision needed to generate high resolutions is dependent on how well the current sources can be matched or the degree to which they can be made binary weighted. Another problem associated with this architecture is the error due to the switching.

- **Charge Scaling**

A very popular architecture used in the CMOS technology is the charge scaling DAC and is shown in Fig. 2.9(a). In this architecture, a parallel array of the binary-weighted capacitors,  $2^N C$ , is connected to the op-amp, where  $C$ , is a unit capacitance of any value. After initially being discharged, the digital signal switches each capacitor to either  $V_{REF}$  or ground (GND) causing the output voltage,  $V_{OUT}$ , to be a function of the voltage division between the capacitors. Since the capacitor array totals  $2^N C$ , if the MSB is 'high' and the remaining bits are 'low', then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog voltage,  $V_{OUT}$  becomes



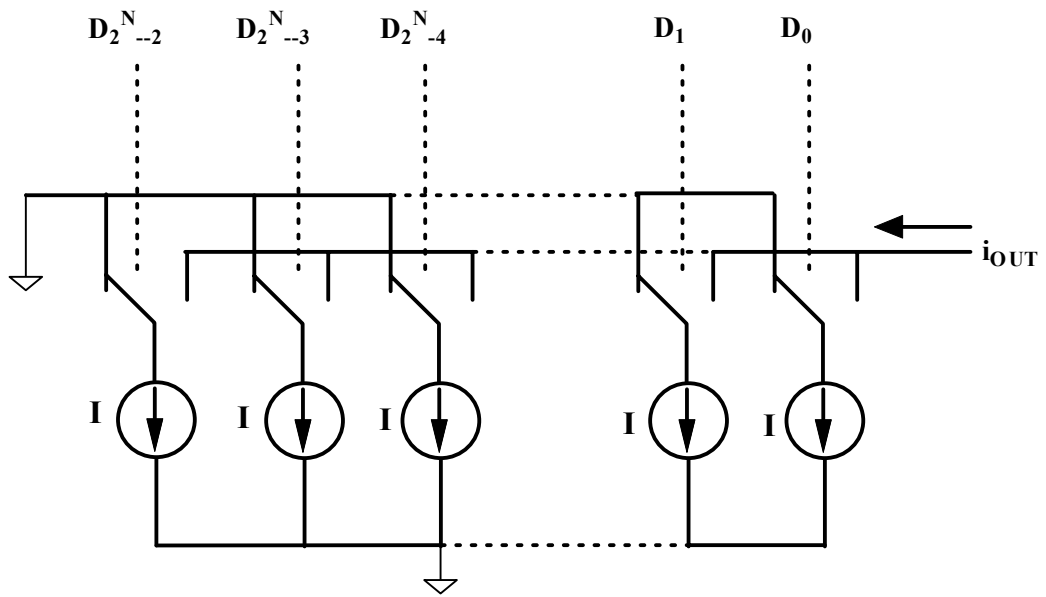


Figure 2.8: Current steering based DAC architecture.

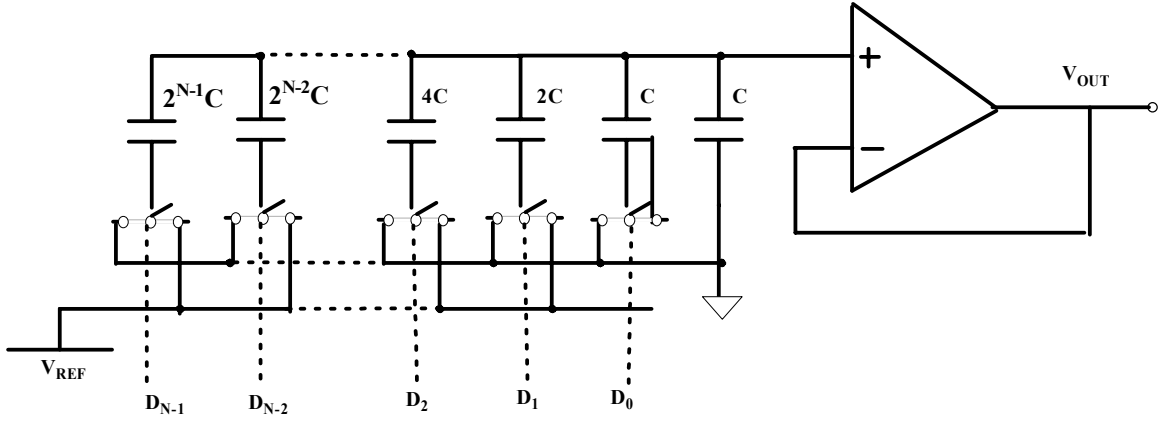


Figure 2.9 (a): Charge scaling DAC Architecture.

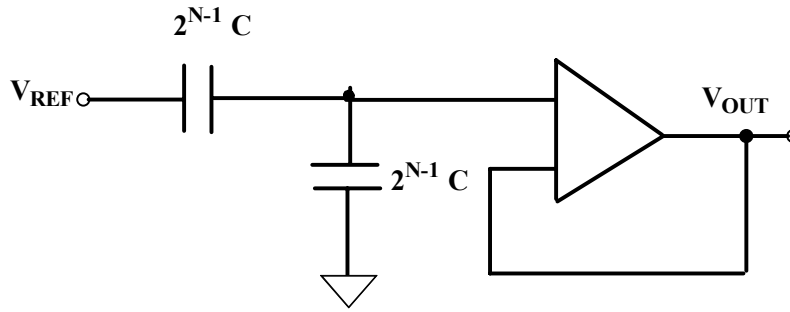


Figure 2.9 (b): Equivalent circuit with MSB =1, and all other bits set to zero.

$$V_{OUT} = \frac{V_{REF}}{2}, \quad (2.11)$$

which confirms the fact that the MSB changes the output of a DAC by  $\frac{1}{2} V_{REF}$ . Figure 2.9(b) shows the equivalent circuit under this condition. Therefore, the value of  $V_{OUT}$  for any digital word is given by [27]

$$V_{OUT} = \sum_{k=0}^{N-1} D_k 2^{k-N} \cdot V_{REF} \text{ where } k = 0, 1 \dots N-1. \quad (2.12)$$

The 10-bit DAC used in our design uses charge scaling DAC. The unit capacitance in the DAC is 10fF. The reference voltage used is 2V,  $V_{SS}$  is  $-2.5V$  and  $V_{DD}$  is  $+2.5V$ .

### 2.3 Digital-to-Analog Converter Operation

The basic circuit diagram of a 10-bit charge-scaling DAC is shown in the Fig. 2.10. This circuit converts the 10-bit digital input word to a respective analog voltage depending on the capacitive network. The various blocks associated with the DAC are operational amplifier, sample-and-hold circuit (S/H), capacitive network and the multiplexer switches to which the digital word is given. Figure 2.11 shows the integrated capacitance network, multiplexer switches and amplifier part of the Fig 2.10. Initially the input digital word is given to a multiplexer circuitry. Depending on the logic value of each bit of the word, the multiplexer chooses the particular voltage to which the capacitor is to be charged. If the input bit in the digital word is logic '0' then the multiplexer chooses the input which is connected to the 'GND' and the capacitor is charged to 'GND' and if the input bit in the digital word is logic '1' then the capacitor is charged to  $V_{REF}$ . The capacitor at the end of the network is used as a 'terminating capacitor'. Depending on the capacitors, which are charged to different voltages based on the input digital

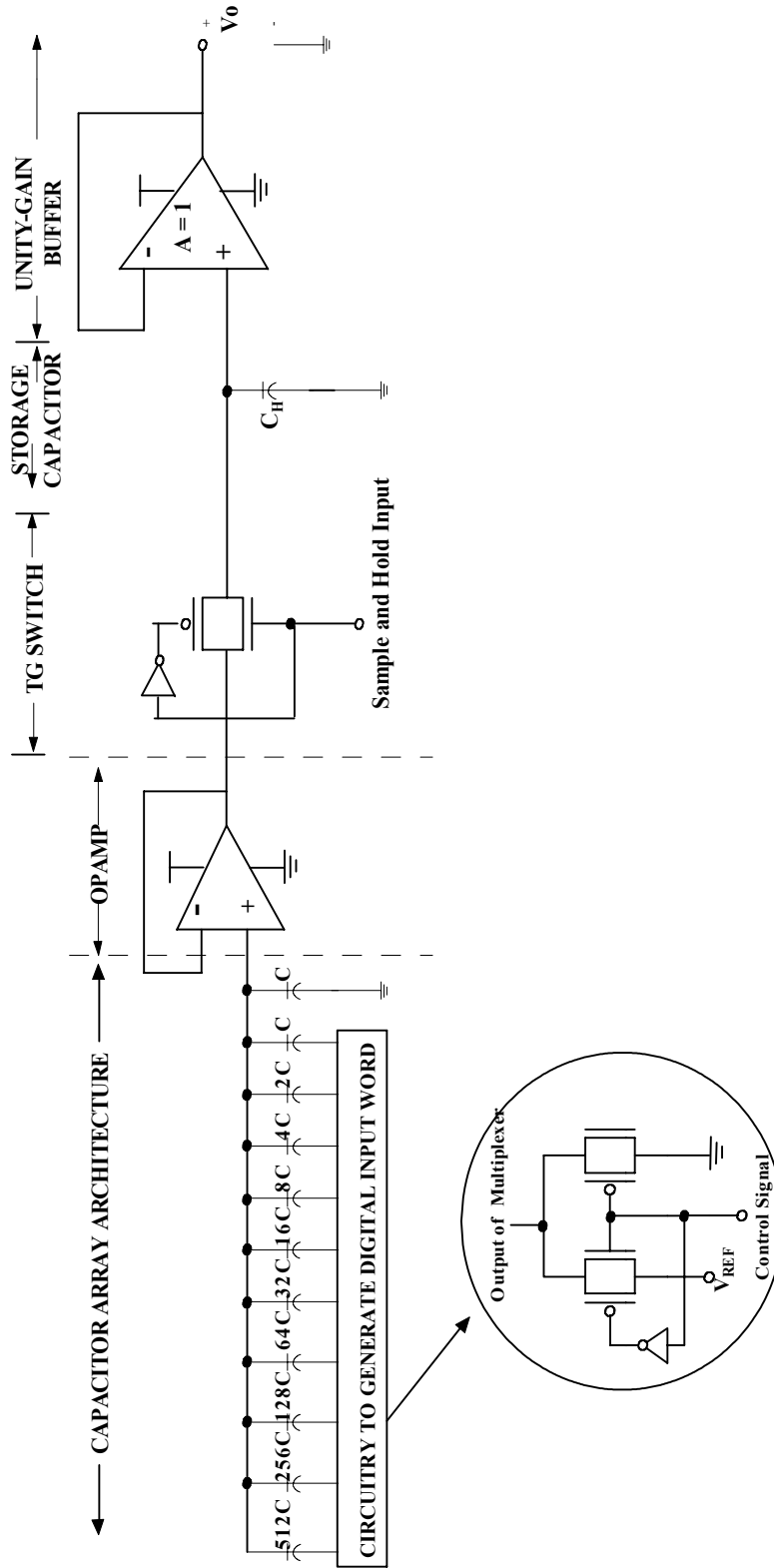


Figure 2.10: Schematic block diagram of a 10-bit charge scaling DAC.  
 Note:  $V_{DD} = +2V$ ,  $V_{SS} = -2V$ ,  $GND = 0V$ .

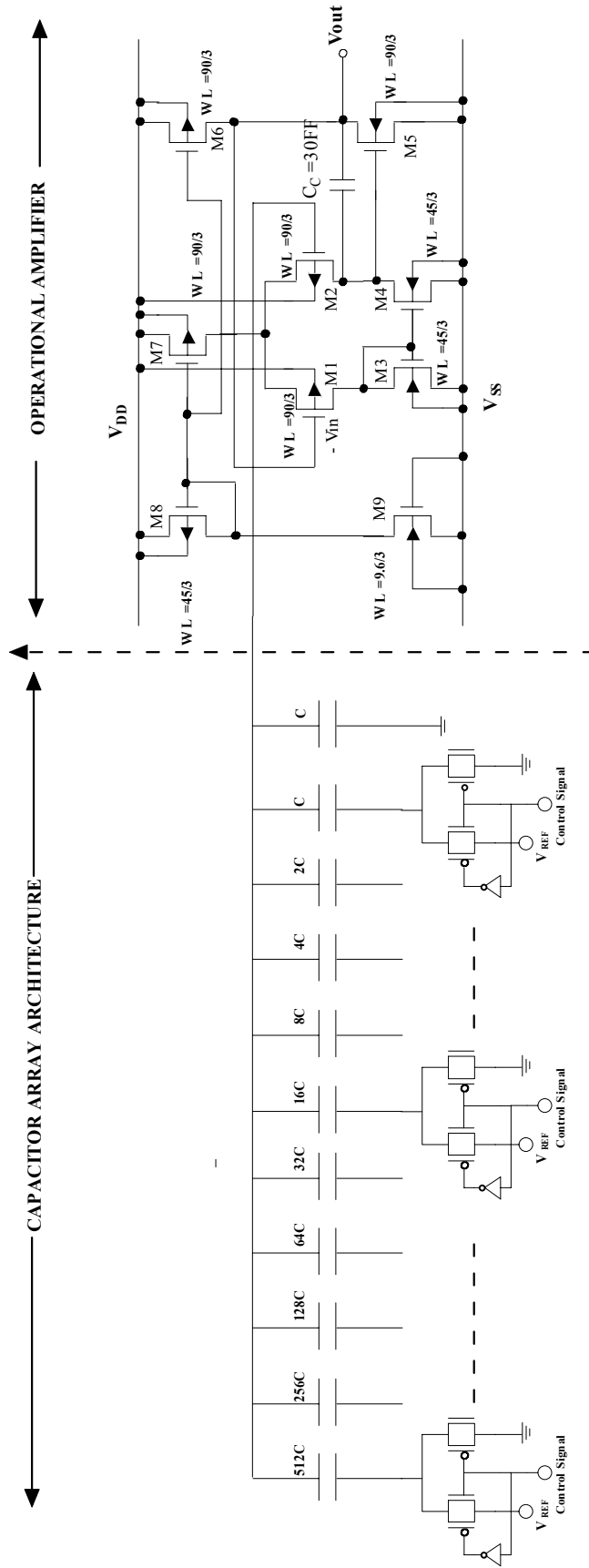


Figure. 2.11: Integrated capacitance network, multiplexer switches and amplifier part of the circuit of Fig. 2.10

The capacitor at the end of the network is used as a ‘terminating capacitor’. Depending on the capacitors, which are charged to different voltages based on the input digital words, the effective resultant analog voltage is calculated for the respective digital combination. This analog voltage is passed through the OPAMP and through the S/H circuit and appears as analog voltage. Thus, the digital to analog conversion is performed. The DAC consists of several blocks and their design is explained in following section.

### **2.3.1 Capacitor Array Design**

The capacitor architecture in the DAC is being drawn using two poly layers poly1 and poly2. The unit capacitance used in the capacitor array is 10fF. Figure 2.12 shows the layout of the unit capacitor used in the design. This design considers unit capacitor configuration since it is a very successful way of overcoming or reducing the effect of various errors introduced during fabrication. In the fabrication process of on-chip capacitors, the capacitance value of a single capacitor can vary with up to 10 to 30 percent from the desired value. Because of this, it is difficult to produce high accuracy capacitors in a standard CMOS process as well as integrated circuits, which rely on the accuracy of a single capacitance value. If, instead, capacitance ratios are used, the relative error is cancelled since it is the ratio of the capacitance that is taken in to consideration but not the single capacitance value alone. Figure 2.13 shows the layout of the capacitor array using unit capacitor configuration. The array is surrounded with dummy capacitors and guarded by the guard ring to cancel out the effect of parasitics.

The capacitors, which are present at the end of the arrays, do not have the surrounding capacitors to cancel out the relative error. To take care of these capacitors

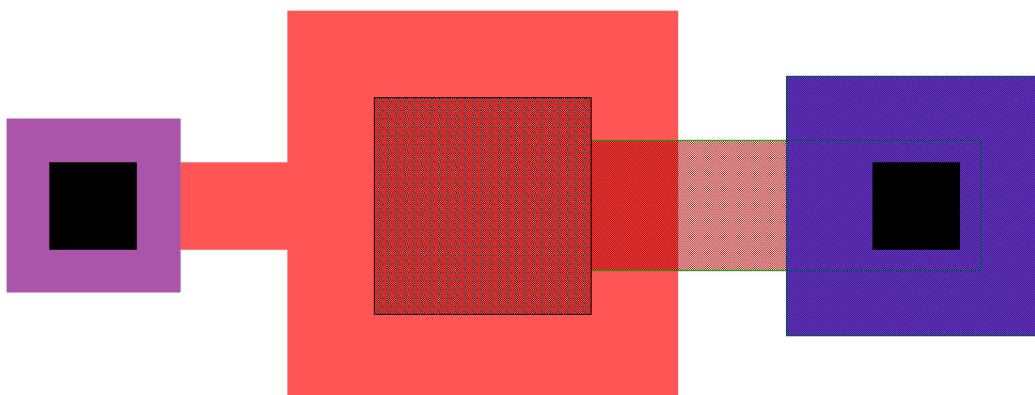


Figure 2.12: Layout of a unit capacitance made of poly1 and poly2 used in the design.

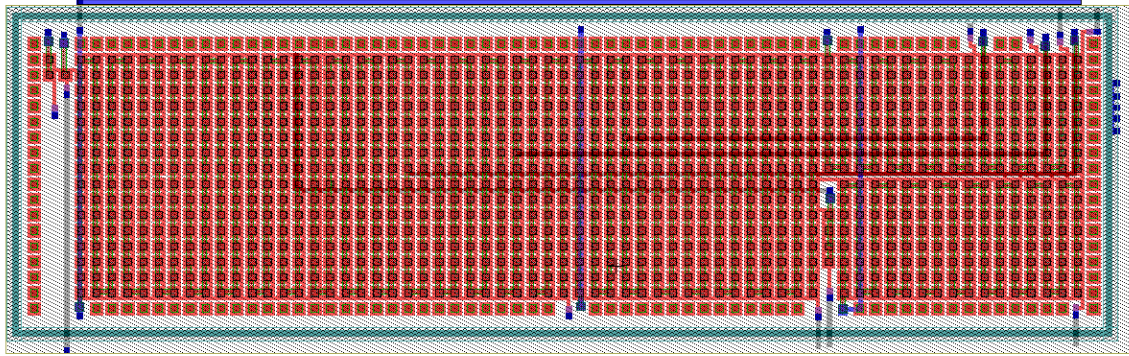


Figure 2.13: Layout of the capacitor array using unit capacitor configuration.



dummy capacitors are added to the array [31]. Figure 2.14 shows the use of dummy capacitors in the capacitor array layout. The substrate noise present in the substrate can be coupled to the capacitor through its parasitic capacitor and any voltage variation present is also coupled to other components of the chip. To avoid this coupling the capacitor array is shielded from the substrate with N-well under it and connecting it to a quiet DC potential [31]. The guard rings are used in the layout around the capacitor array to prevent from any sort of interference.

### **2.3.2 Operational Amplifier Design**

In the analog world, the most commonly used device is the operational amplifier (OPAMP). An operational amplifier is an electronic device whose output can be related to its input in terms of a known mathematical operation. This is usually achieved by using active or passive elements such as resistors and capacitors in integrators and differentiator circuits. A typical operational amplifier is characterized by a high open loop gain, high bandwidth, a very high input impedance, low output impedance and an ability to amplify differential mode signals to a large extent and at the same time, severely attenuate common mode signals. The amplifier in the 10-bit DAC (Fig.2.10) is realized by one such operational amplifier. Figure 2.15 shows the block diagram of an operational amplifier [30]. An OPAMP normally consists of four main functional blocks. First is the input differential gain stage that amplifies the voltage difference between the input terminals, independently of their average or common mode voltage. Most of the critical parameters of the OPAMP like the input noise, common mode rejection ratio (CMRR) and common mode input range (CMIR) are decided by this stage. The differential to single-ended conversion stage follows the differential amplifier and is responsible for

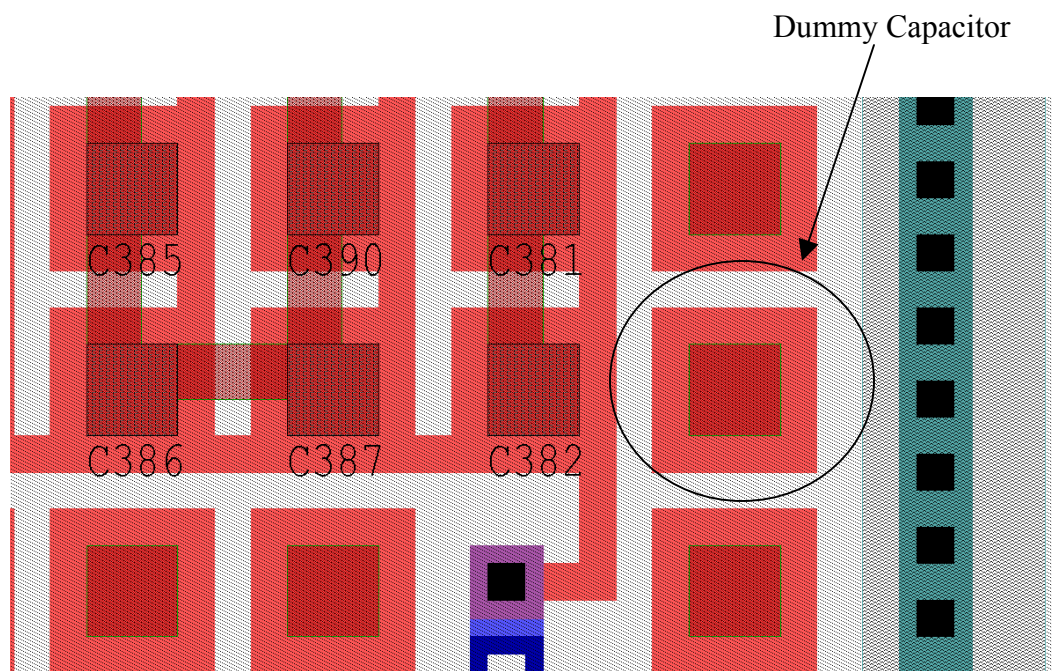


Figure 2.14: Layout showing the use of dummy capacitors to match the capacitors present at the corner of the capacitor array.

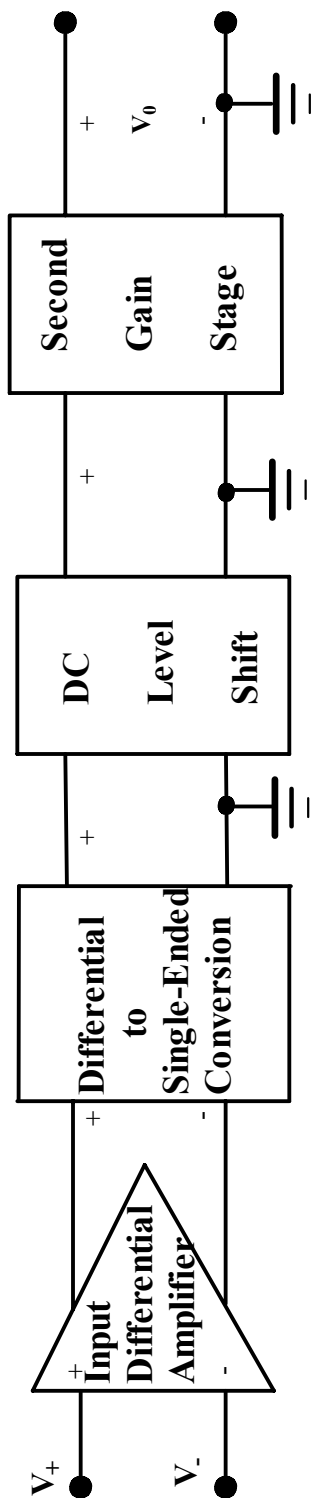


Figure 2.15: Block diagram for an integrated OPAMP.

producing a single output, which can be referenced to ground. As it is necessary to bias the second gain stage properly, a level-shifting block is introduced after the differential to single-end conversion stage. Finally, additional gain is obtained in the second gain stage.

A description as well as the design methodology of each of the stages mentioned above is carried out in the following subsections.

### **2.3.3 A Two-Stage CMOS OPAMP Topology**

The most widely used CMOS operational amplifier is a two-stage configuration as shown in Fig. 2.16. This circuit configuration provides a good voltage gain, a good common mode range and good output swing. Before the analysis of the OPAMP is done, some of the basic principles behind the working of MOS transistors are reviewed. The input differential amplifier stage is implemented by a differential pair of p-MOS transistors (M1 & M2) with their sources tied together. The differential pair is biased by current mirrors, which act as the active load too. Two current mirrors: a p-MOS current mirror (M7 & M8) and an n-MOS current mirror (M3 & M4) are used instead of just one in order to increase the common mode rejection ratio (CMRR) of the differential pair. The p-MOS current mirror serves as a constant current source and the n-MOS mirror, which sinks current, acts as an active load across which the first stage output is taken, thereby performing a differential to single-ended conversion in the process.

### **2.3.4 Current Mirrors**

Current mirrors are used extensively in MOS analog circuits both as biasing elements and as active loads to obtain high AC voltage gain [28, 29]. Enhancement-mode transistors remain in saturation when the gate is tied to the drain, as the drain-to-source voltage

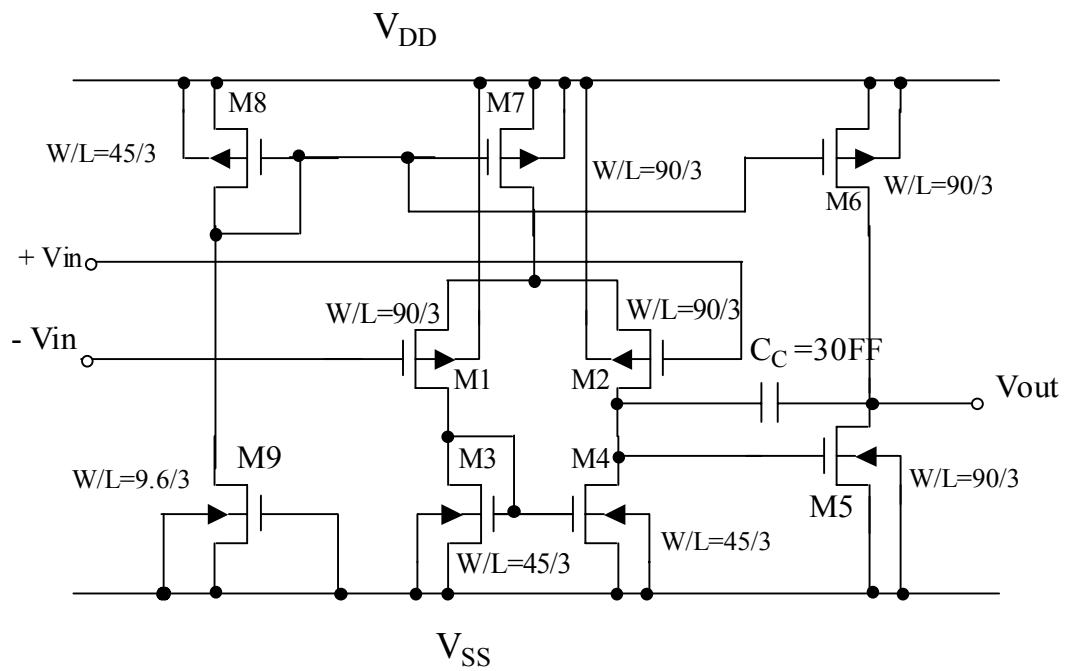


Figure 2.16: A CMOS operational amplifier.

( $V_{DS}$ ) is now always going to be greater than the gate-to-source voltage ( $V_{GS}$ ) due to the threshold voltage ( $V_{th}$ ) drop i.e

$$V_{DS} > V_{GS} - V_{th} \quad (2.13)$$

Based on Eq. (2.13), constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor. Figures 2.17 and 2.18 shows the p-MOS and n-MOS current mirrors design. A p-MOS mirror serves as a current source while the n-MOS acts as a current sink. The voltage developed across the diode-connected transistor is applied to the gate and source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, the currents, which when both transistors are in the saturation region of operation, are governed by the following equation 2.14 assuming matched transistors. The current ratio  $I_{OUT} / I_{REF}$  is determined by the aspect ratio of the transistors. The reference current that was used in the design is  $100\mu A$ . The desired output current is  $200\mu A$ .

For the p-MOS current mirror, we can write,

$$I_{OUT} / I_{REF} = (W_7 / L_7) / (W_8 / L_8) \quad (2.14)$$

For  $(W_7/L_7) / (W_8/L_8) = 2$ ,

$$I_{OUT} = 2 \times I_{REF} = 200\mu A \quad (2.15)$$

For identical sized transistors, the ratio is unity, which means that the output current mirrors the input current. Because the physical channel length that is achieved can vary substantially due to etching variations, the accurate current ratios usually results when devices of the same channel length are used, and the ratio of currents is set by the channel width. For the n-MOS current mirror design shown in Fig 2.18,

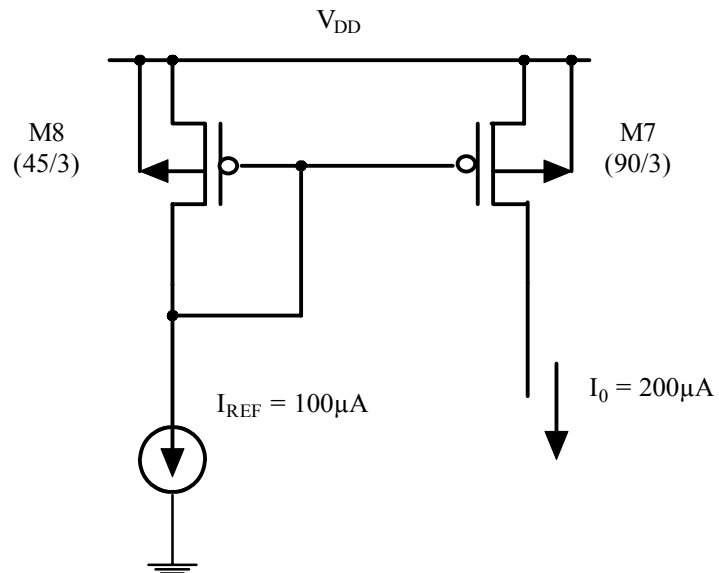


Figure 2.17: PMOS current mirror design.

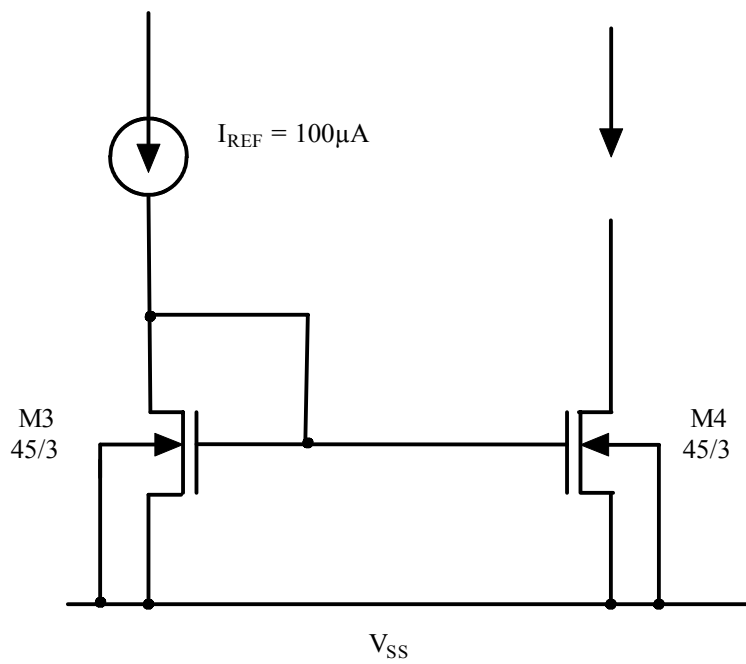


Figure 2.18: NMOS current mirror design.

$$I_{OUT} / I_{REF} = (W_4/L_4) / (W_3/L_3) \quad (2.16)$$

For  $(W_7/L_7) / (W_8/L_8) = 1$ ,

$$I_{OUT} = I_{REF} = 100\mu A. \quad (2.17)$$

### 2.3.5 Active Resistor

The reference current that is applied to the current mirror is obtained by means of an active resistor. A resistor can be obtained by simply connecting the gate of a MOSFET to its drain as shown in Fig 2.17 and 2.18. This connection forces the MOSFET to operate in saturation in accordance with the equation.

$$I_{DS} = \beta (V_{GS} - V_{th})^2 / 2 \quad (2.18)$$

Where all the symbols have their usual meanings. Since the gate is connected to the drain, the current  $I_{DS}$  is now controlled directly by  $V_{DS}$  and therefore the channel transconductance becomes the channel conductance. The small signal resistance is given by

$$r_{out} \simeq r_{ds} / (1 + g_m \cdot r_{ds}) \cong 1 / g_m \quad (2.14)$$

where  $g_m$  is the transconductance of the MOS transistor. It is defined as the ratio of the change in drain current to a change in the applied gate and is described by the following equation.

$$g_m = \delta I_{DS} / \delta V_{GS} \mid V_{DS, \text{ constant}} \quad (2.19)$$

$$\text{or } g_m = \sqrt{2\beta I_D}. \quad (2.20)$$

It is to be noted that the transconductance of a MOS increases as the square root of the drain current. Therefore, MOS amplifiers need several stages to achieve large gains due to their low  $g_m$  values.



The operational amplifier designed in this work is shown in Fig. 2.16. The small signal gain of the differential amplifier stage is described as follows [27]

$$A_1 = g_{m1} (r_{o2} \parallel r_{o4}) = \frac{2\sqrt{\beta}}{(\lambda_2 + \lambda_4)\sqrt{I_{SS}}} = \frac{2}{(\lambda_2 + \lambda_4)(V_{GS} - V_{thp})} \quad (2.21)$$

Where  $I_{SS}$  is the differential amplifier bias current and  $V_{thp}$  is the threshold voltage of the pmos transistors forming the differential pair. The differential amplifier needs to be biased by a constant current source, which is provided by the 100 $\mu$ A current source. The same current is supplied to the two stages of the operational amplifier by the p-channel current mirrors M8, M7, M6 which provide the bias current for the two stages. In the first stage i.e. the differential amplifier stage not only is the differential amplification accomplished but also the differential to single ended conversion done. Thus, the output is taken only from one of the drains of the transistors. The n-channel devices M3 and M4, which are the load for the p-channel devices, also aid in the single ended conversions. The second stage provides a level shift for the output of the differential amplifier stage and it also provides the additional gain. It is once again biased by a current source, which is also used to maximize the gain of the second stage. To get a high gain with reasonable high output resistance the minimum channel length used is 3 $\mu$ m and maximum width of the transistor used is 90 $\mu$ m. Transistor M<sub>5</sub> is critical to the frequency response, is biased at  $I_{D5} = 200\mu$ A and has  $(W/L)_5 = (W/L)_{max} = 30$ . The input pair is biased at  $-I_{D7} = 200\mu$ A. To avoid input offset voltage transistors M<sub>3</sub> and M<sub>4</sub> are dimensioned according to [28]

$$\frac{\left(\frac{W}{L}\right)_5}{2 * \left(\frac{W}{L}\right)_{3,4}} = \frac{-I_{D6}}{I_{D7}} = \frac{200\mu A}{200\mu A} = 1 \rightarrow \left(\frac{W}{L}\right)_{3,4} = \frac{1}{2} \left(\frac{W}{L}\right)_5 = 15 \quad (2.22)$$

Therefore, the  $W = 45\mu\text{m}$  for the transistors  $M_3$  and  $M_4$ . To obtain the bias current of  $100\mu\text{A}$  a MOS resistor is used with appropriate value of width. (which is the MOSFET simulating resistors). Large  $W/L$  ratios for the transistors in the operational amplifier are obtained by using the following technique. The four transistors are connected in such a way that the effective  $W/L$  ratio is four times the  $W/L$  ratio of each transistor. The technique reduces the required area, in comparison to a device laid out in a straightforward manner. The benefit of this technique is reduced junction capacitance, and is well characterized. The simplicity, modularity and predictability of the device overcome the penalty of associated area.

The physical layout of the amplifier was made using the L-EDIT 8.20 and the 'spice' netlist is extracted including parasitic capacitances. The layout of the amplifier is shown in the Fig.2.19. Figure. 2.20 shows the transfer characteristics obtained from DC sweep analysis. The output offset voltage is approximately  $33\mu\text{V}$ . Figure 2.21 shows the transient analysis of operational amplifier. An input voltage of  $500\mu\text{V}$  is applied to the inverting terminal of the OPAMP at a frequency of  $100\text{ kHz}$ . An inverted waveform is obtained at the output of the OPAMP with peak-to-peak amplitude of  $2\text{v}$ , giving a gain of 4000. Figure 2.22 shows the frequency response characteristics. Figure 2.22(a) shows the amplitude versus frequency behavior. The 3dB bandwidth of the amplifier obtained is approximately  $100\text{ kHz}$  and 3dB gain is 77. Figure 2.22(b) shows the phase versus. frequency response. The phase noise margin as shown in Fig.2.22 (b) is  $20^\circ$ . The maximum input range is  $\pm 100\text{mV}$ .

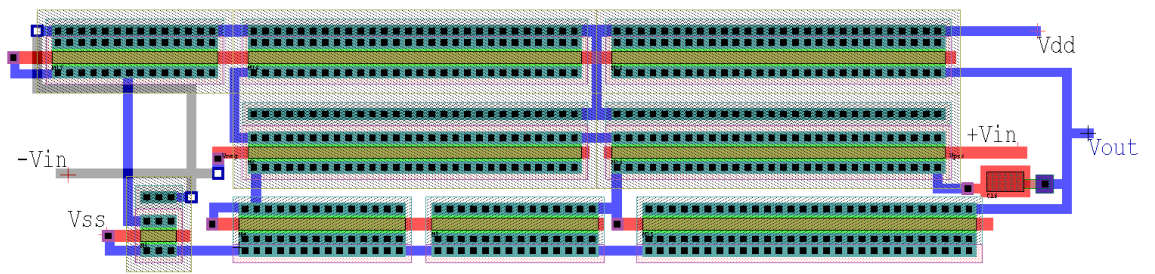


Figure 2.19: Layout of an operational amplifier design of Fig. 2.16.

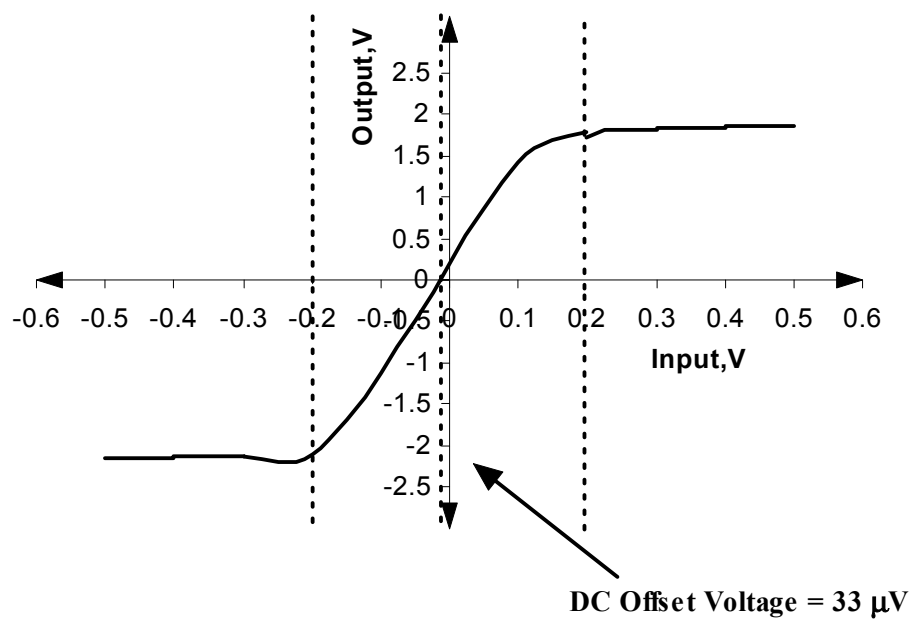


Figure 2.20: Post-layout transfer characteristics of the circuit of Fig. 2.16.

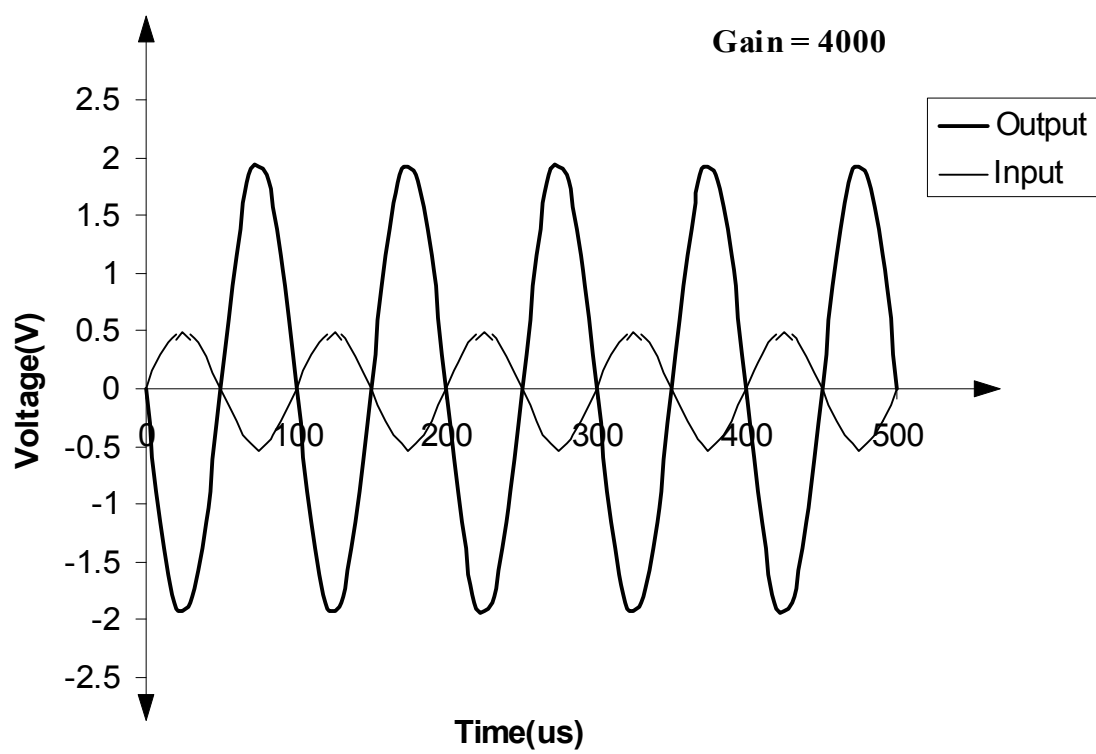


Figure 2.21: Input and Output response of the amplifier circuit of Fig. 2.16.

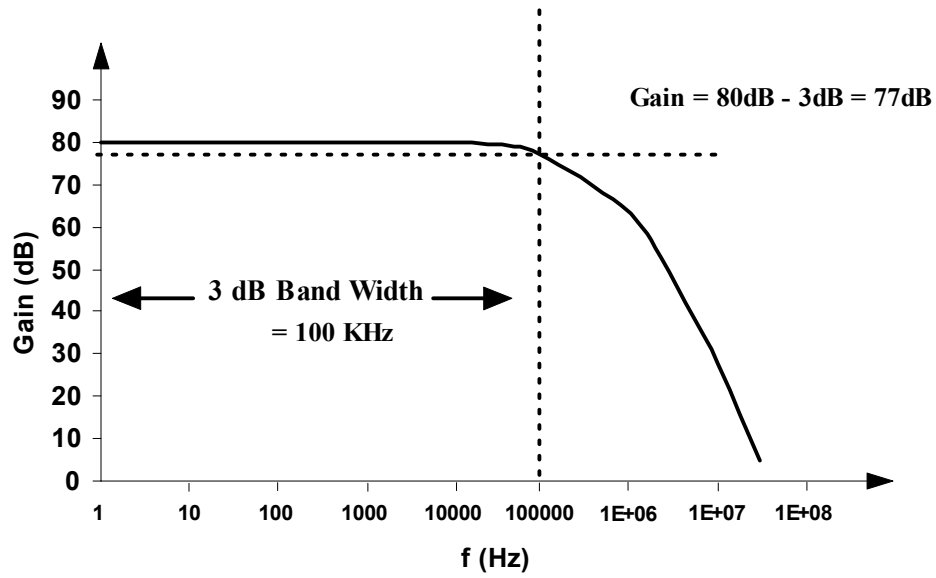


Figure 2.22(a): Frequency response characteristics of the circuit of Fig. 2.16.

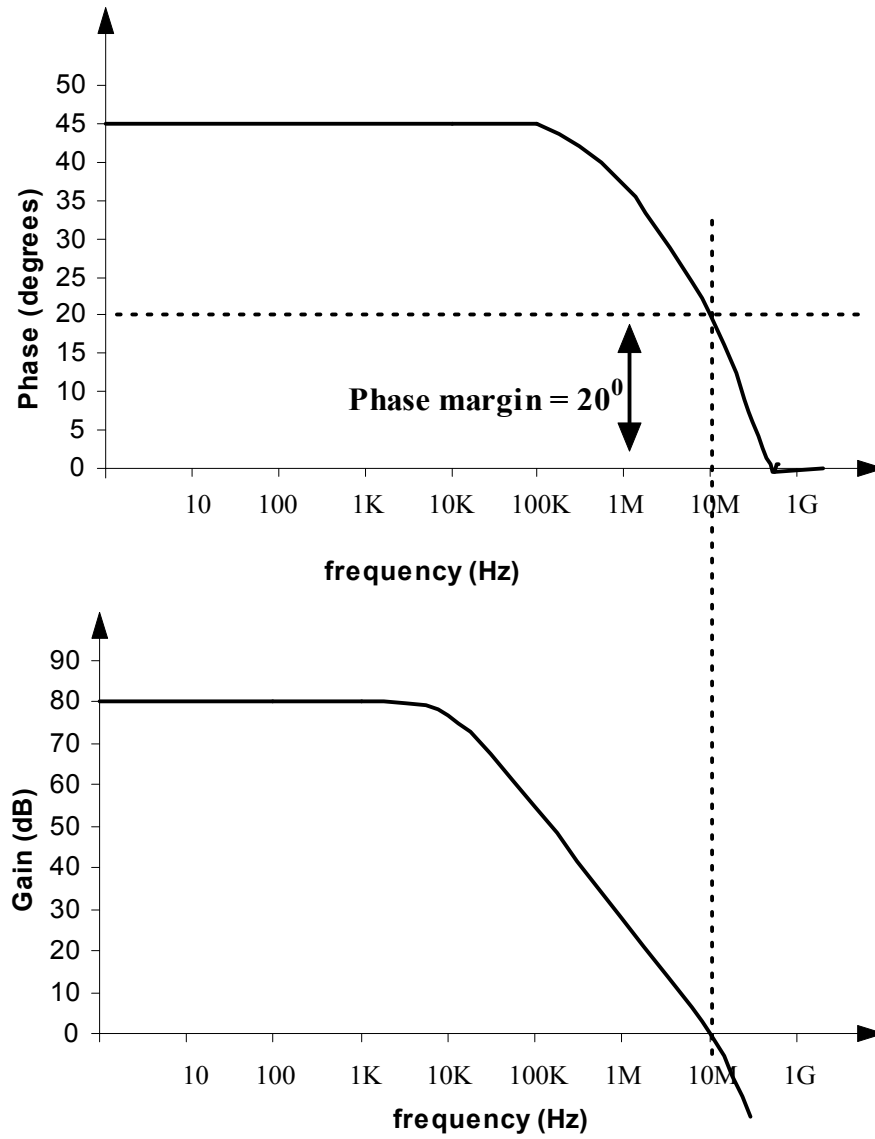


Fig. 2.22(b): Phase response characteristic of the circuit of Fig. 2.16.  
Note: The phase margin is  $20^\circ$ .

### 2.3.6 Unity Follower

A unity follower is basically an amplifier with a gain of unity. It is used mainly as a buffer amplifier in order to increase the current driving capability of the amplifier stage. An ideal unity follower would exhibit infinite input impedance, zero output impedance, large bandwidth and unity gain. The gain-bandwidth product of the amplifier is known, as it's figure-of-merit, and is a constant for any given amplifier. It is usually determined for an OPAMP by putting it in the unity follower configuration.

From basic OPAMP theory, we know that the gain of an OPAMP in its non-inverting configuration as shown in Fig. 2.23 given by

$$V_0 = \left(1 + \frac{R_f}{R}\right) V_i \quad (2.23)$$

$R_f$  and  $R$  are the feedback and series resistances of the OPAMP and  $V_i$  and  $V_0$  are the input and output voltages of the OPAMP. The gain of the OPAMP is determined by the resistive network alone and is given by,

$$A_v = \left(1 + \frac{R_f}{R}\right) \quad (2.24)$$

If  $R_f$  is zero, then the gain of the amplifier is unity. The input to be buffered is applied to the non-inverting terminal of the unity follower, and the output connected to the inverting terminal of the OPAMP in the feedback configuration. So, as the signal increases in strength at the non-inverting terminal, the signal at the inverting end increases too thus forcing the output to follow the input. Only the differential stage of the amplifier discussed was used to realize the unity follower buffer as shown in Fig 2.24. The drain of transistor M5 is coupled back to the gate of the input transistor M1. This connection



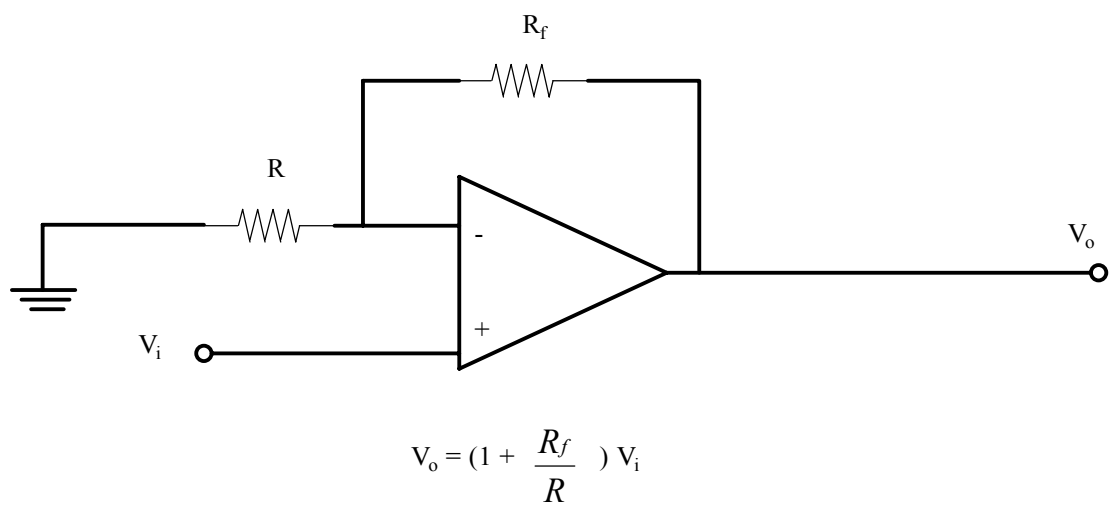


Figure.2.23: The non-inverting OPAMP configuration.

introduces feedback to the inverting terminal of the OPAMP, thus, putting it in the unity follower configuration.

### 2.3.7 Sample-and-hold Circuit

The principal application for sample-and-hold (S/H) amplifier is to maintain a constant output of the DAC during conversion. The characteristics of the S/H amplifier are crucial to system accuracy and the reliability of the analog data. As its name indicates, a S/H amplifier has two modes of operation, programmed by a digital control input. In the *sample* mode, the output follows the input, usually with a gain of unity. When the mode input switches to *hold*, the output of the S/H amplifier ideally retains the last value it had when the command to hold was given, and it retains that value until the mode input switches back to *sample*. At this time, the output ideally jumps to the input value and follows the input until the next *hold* command is given. Figure 2.25 is a block schematic of a sample-and-hold amplifier. It consists of three major components: a transmission gate switch (TG-switch), a storage capacitor  $C_H$  and a unity gain follower. Each of these elements need to be designed/chosen carefully for good performance. The operation mechanism is as follows. The TG-switch is operated by the  $V_{\text{CONTROL}}$  signal and is closed during the *sample* interval and open during *hold*. So, during *sample*, the circuit is connected to promote rapid charging of the storage capacitor,  $C_H$  and during *hold*, the capacitor,  $C_H$  is disconnected from its charging source and ideally retains its charge. The capacitor is connected to a unity-gain buffer-follower whose output follows the charge held by the storage capacitor. The unity gain buffer is used at the output to avoid the large overshoot, which might occur, on the output when the input changes quickly.

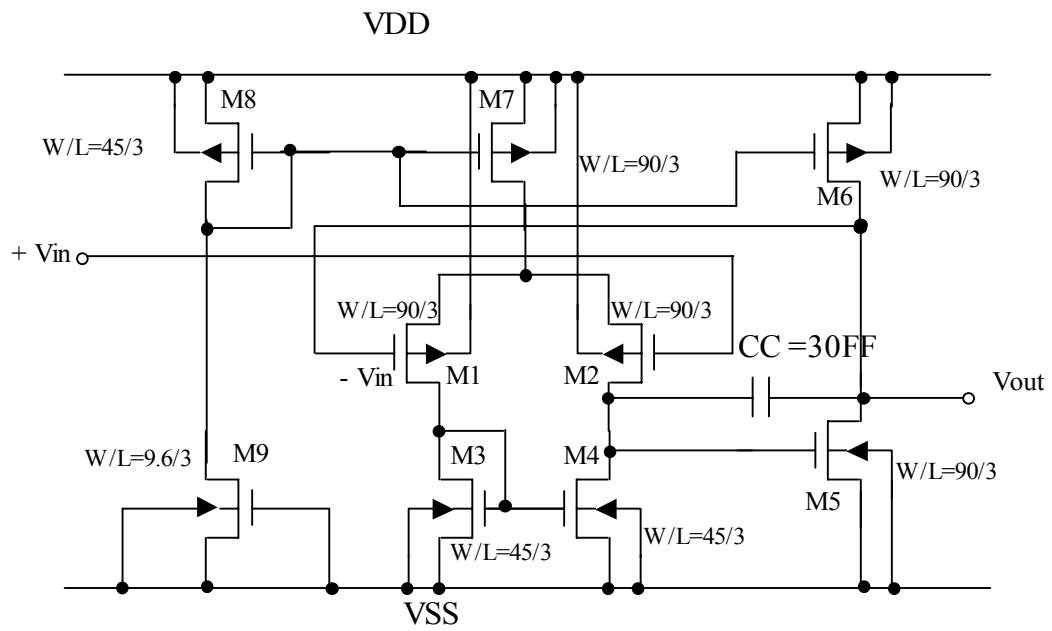


Figure.2.24: The CMOS operational amplifier as a unity gain amplifier (unity follower).

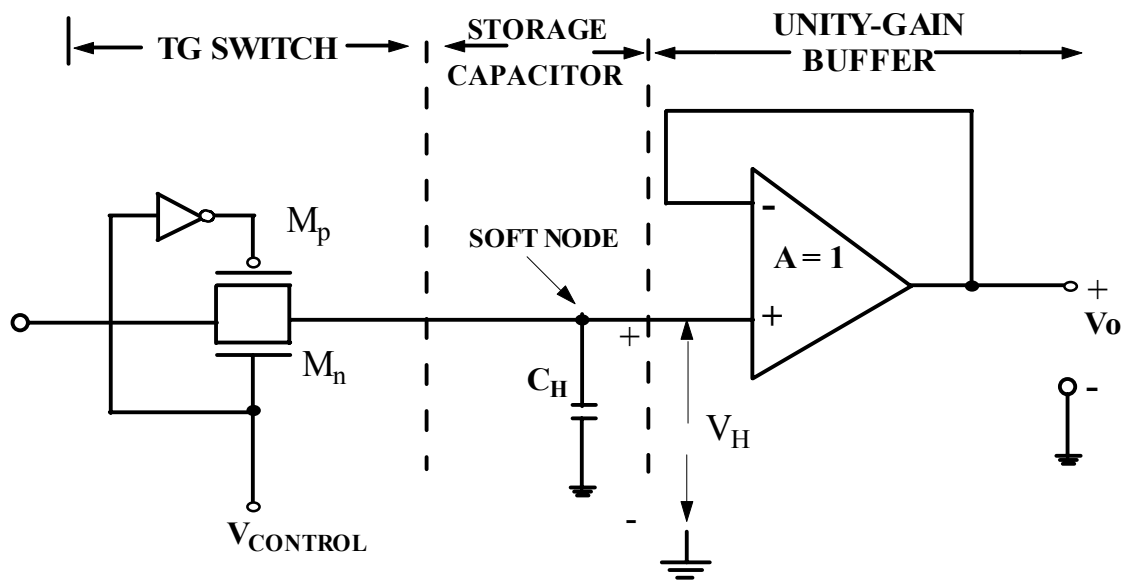


Figure 2.25: Schematic diagram of a sample-and-hold amplifier.

### 2.3.8 The Transmission Gate Switch

The input switch to the S/H amplifier is controlled by a digital signal generated from an external control and synchronizing logic to represent the two modes of operation - the *sample* and *hold*. The switch should ideally offer zero resistance to the signal when it is closed (*sample*) and infinite resistance when open (*hold*). Moreover, when closed, it should exhibit the same properties irrespective of whether the capacitor is charging or discharging. An ideal switch also takes zero time to turn on or off. A CMOS transmission gate switch (TG-switch) is constructed by paralleling an n-MOS transistor with a p-MOS transistor. The transmission gate switch can be made to turn ON or OFF for either polarity of the mode control signal by connecting a simple inverter between the gates of the transistors. Since the transmission gate has both an n-type and a p-type devices, connected in parallel, there is no degradation of the signal whether it is large or small. The expression for the charging time constant through a CMOS transistor gate can be expressed as [32]

$$\tau_n = C_H \left[ \frac{1}{\beta_n(V_{DD} - V_{tn})} + R_{eq} \right] \quad (2.26)$$

and the discharging time constant as [32]

$$\tau_p = C_H \left[ \frac{1}{\beta_p(V_{DD} - V_{tp})} + R_{eq} \right] \quad (2.27)$$

where  $C_H$  is the hold capacitor. The term  $R_{eq}$  represents the equivalent resistance of the transmission gate which remains a constant during charging and discharging. From the above two equations, if the threshold voltages of the n-MOS and p-MOS transistors are made equal and the aspect ratios of them are so adjusted such that  $\beta_n = \beta_p$ , the time to charge and discharge through the transmission gate would be equal, thus giving

symmetrical response. Since the transition from ON to OFF and vice versa is much faster now with the use of a transmission gate switch, two important terminologies with reference to S/H amplifiers are defined. *Acquisition Time* is the time required by the output of the S/H to reach its final value, within a specified error band, after the *sample* command has been given. *Aperture (Delay) Time* is the time required for the switch to open fully after the hold command is given. The held voltage is, in effect delayed by this interval and the hold command should therefore be advanced by this amount for precise timing. Needless to say, both these times are reduced significantly by the use of a transmission gate switch rather than a pass gate.

### **2.3.9 The Storage Capacitor**

The storage capacitor limits the slew rate in the *sample* mode and determines the ‘droop’ in the *hold* mode of operation. The slew rate is the rate at which the voltage across the capacitor can change with respect to time and is entirely a function of the input signal frequency. The equivalent circuit of the S/H amplifier during *sample* is that of a low-pass filter with the series resistance of the filter consisting of the TG-switch resistance when closed, and the storage capacitor  $C_H$ . For the voltage of the capacitor to follow the input signal fairly well, the RC time constant of the filter should be close to the time period of the input signal. The value of the storage capacitor to be used is therefore a function of the input signal frequency. The other consideration for the value of the storage capacitor is the droop rate. ‘Droop’ is the gradual drop in the ‘held’ voltage by the capacitor with time, during the *hold* period. Obviously, this introduces errors in the digital-to-analog conversion process, as the voltage level at any time after the instant it was sampled would be different from the level at which it was sampled.

The storage capacitor  $C_H$  was implemented using the Poly1 and Poly2 layers in standard CMOS process. The parallel plate capacitance used in the design is 12 pF. Figure 2.26 shows the S/H CMOS circuit. The layout of the sample-and-hold CMOS circuit of Fig 2.26 is shown in Fig. 2.27. The post-layout SPICE simulations were performed. Figure 2.28 shows the post-layout simulated sample and hold response of the circuit of Fig 2.26. The input to the circuit is a 4V p-p sine wave and the control voltage given to the circuit is 5V p-p pulse. When the pulse is HIGH, the circuit samples the input and when the pulse is LOW, the circuit holds its previous state. A microvolt signal was applied to the input of the OPAMP and a control signal  $V_{\text{control}}$  was applied to the sample-and-hold circuit as shown in Fig. 2.29. The amplified signal from the OPAMP was reproduced by the unity follower with a total offset of about 33 $\mu$ V. Figure 2.30 shows the circuit behavior of the circuit of Fig. 2.29 obtained from post-layout simulations.

## 2.4 10-bit Digital to Analog Converter

Figure 2.31 shows the layout of a 10-bit DAC. The 10-bit charge scaling DAC is tested by giving various combinations of digital input words and the respective analog output voltage is obtained. The reference voltage used in the design is 2.0V. The 10-bit charge scaling DAC has about 1024 digital word combinations and is quantized within the reference voltage of 2.0V with a step of 1.9mV. This is obtained as follows

Total number of input combinations = 1024 (since it is  $2^{10}$  combinations of input)

The reference voltage used is 2V. The least significant change in the output value is

$$\text{LSB} = \frac{2}{1024} = 1.9\text{mV}. \quad (2.28)$$

Figure. 2.32(a) and (b) show the DAC output characteristics, for all combinations of the digital input word starting from ‘0000000000’ to all ‘1111111111’s.



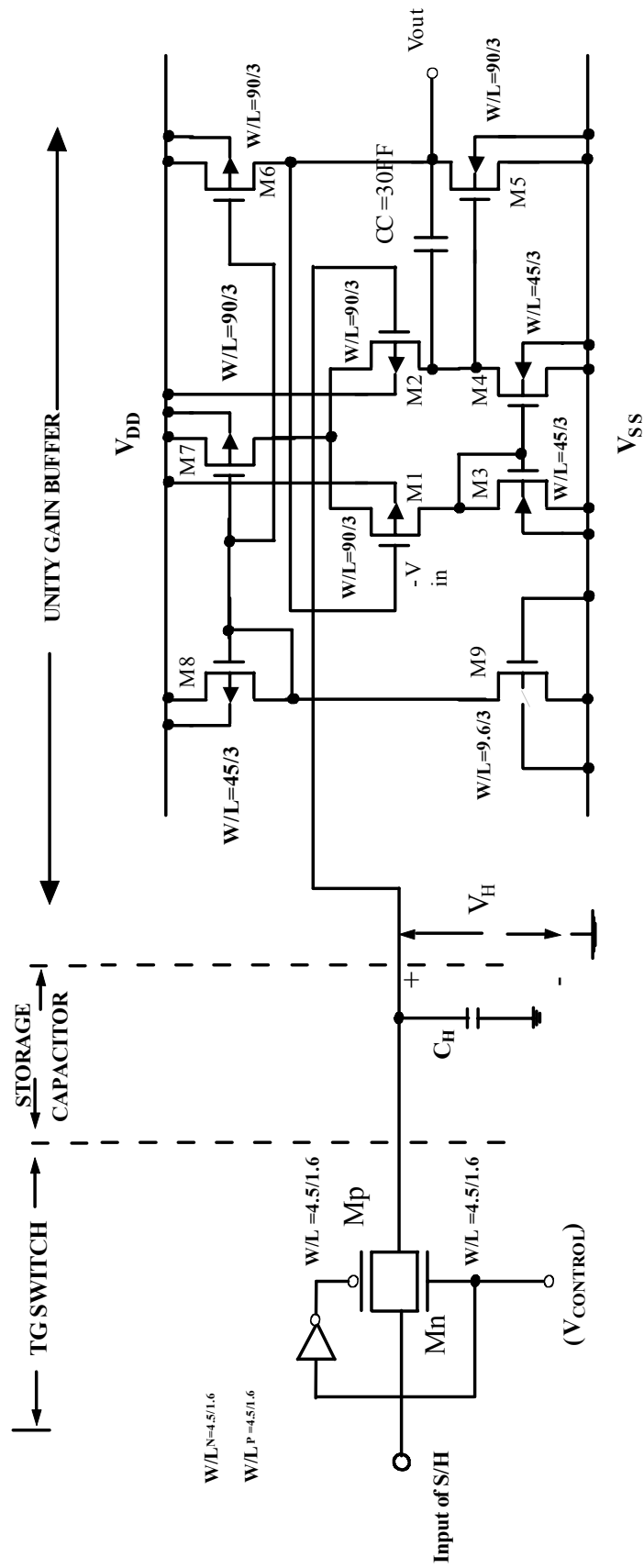


Figure 2.26: Sample-and-hold CMOS circuit

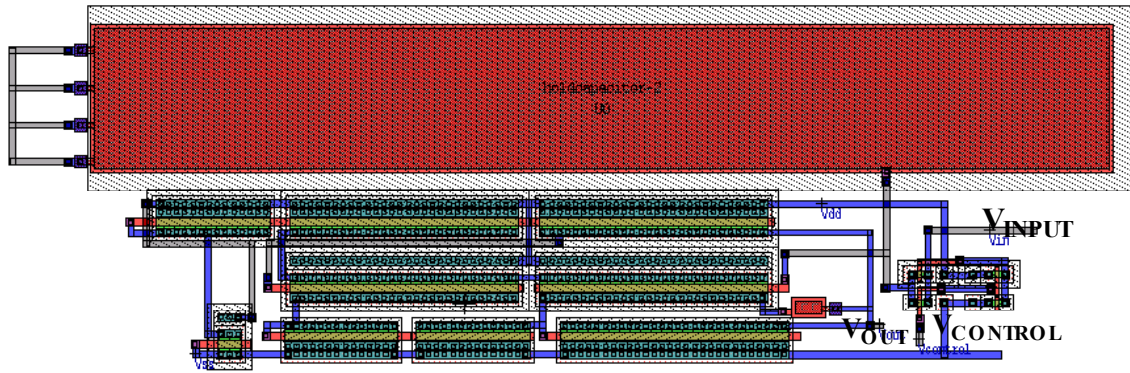


Figure.2.27: Layout of a CMOS sample-and-hold circuit (S/H) circuit.

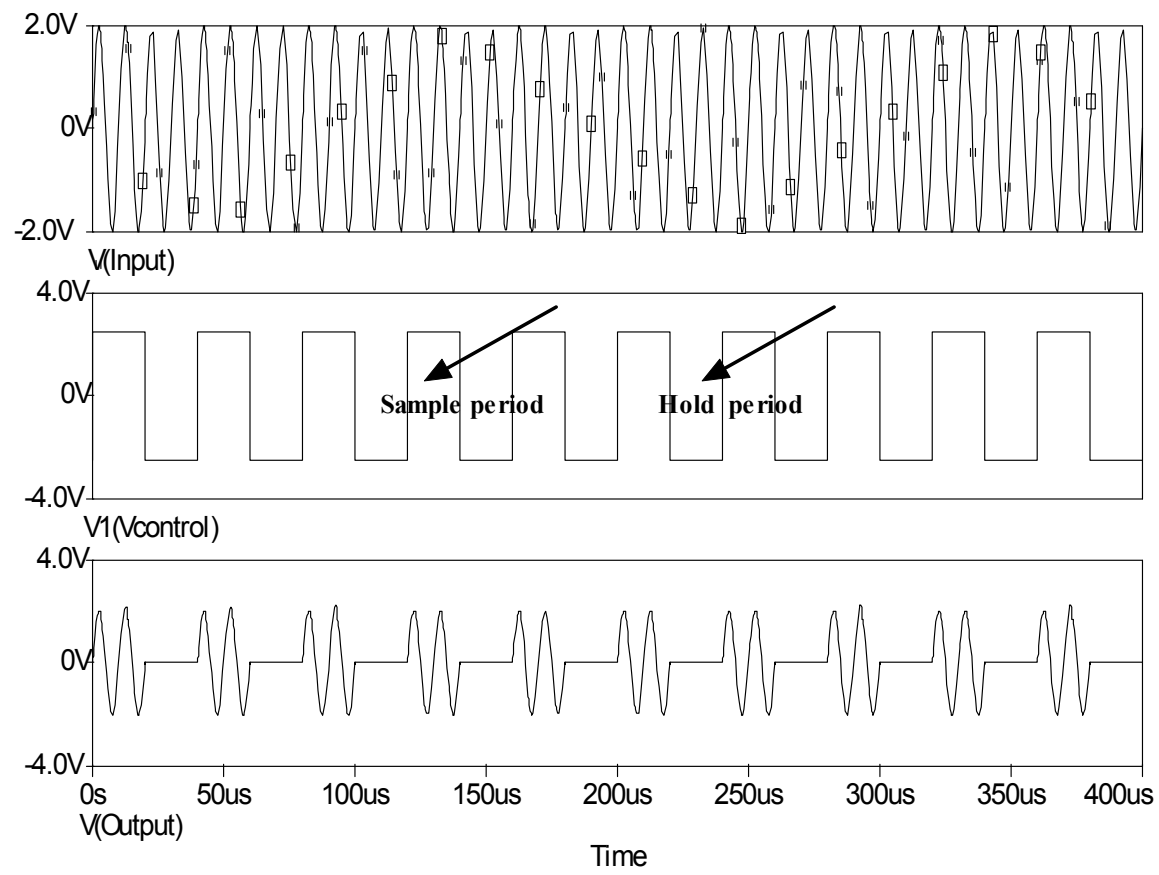


Figure 2.28: Sample-and-hold circuit response.  
 Note: Sample and hold period are as shown in figure.

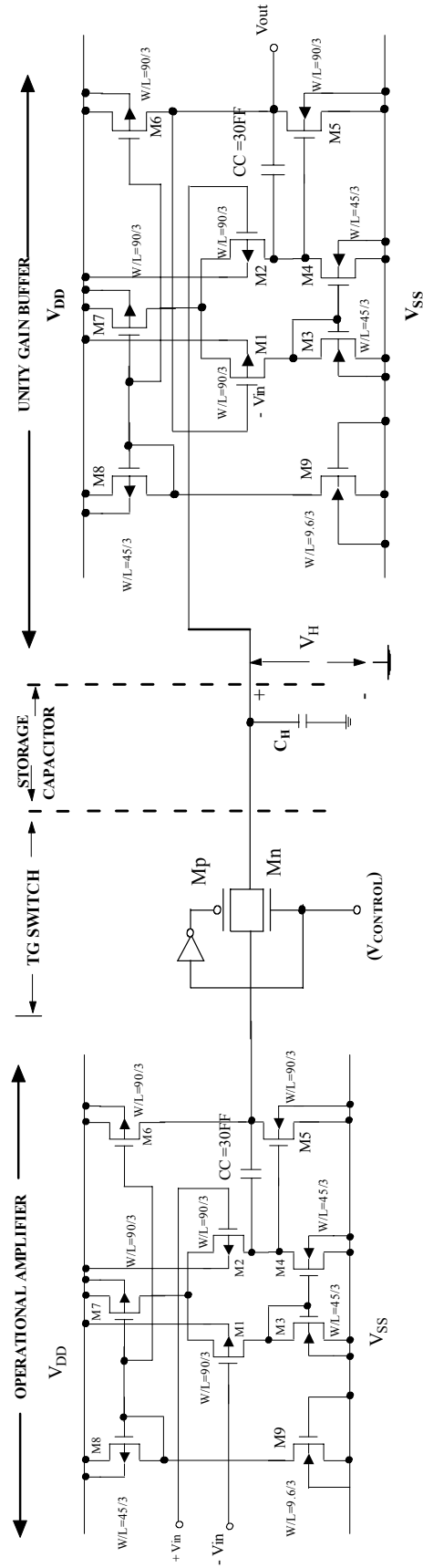


Figure 2.29: Schematic block diagram showing op-amp, TG-switch, storage capacitor and unity gain buffer.

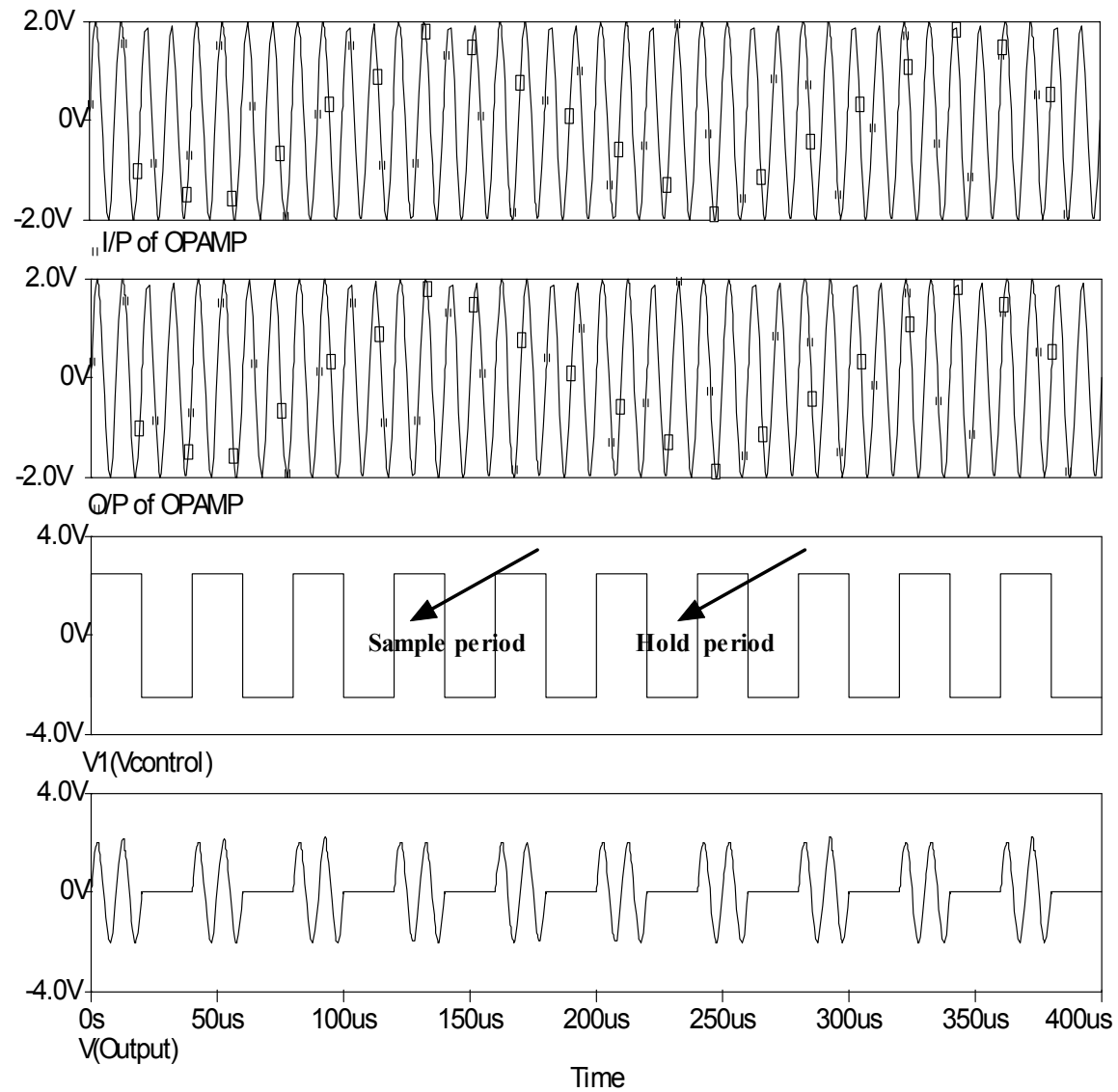


Figure 2.30: Sample-and-hold response of the circuit of Fig. 2.26 obtained from post-layout SPICE simulations.  
 Note. Input signal peak-to-peak voltage is 4V.

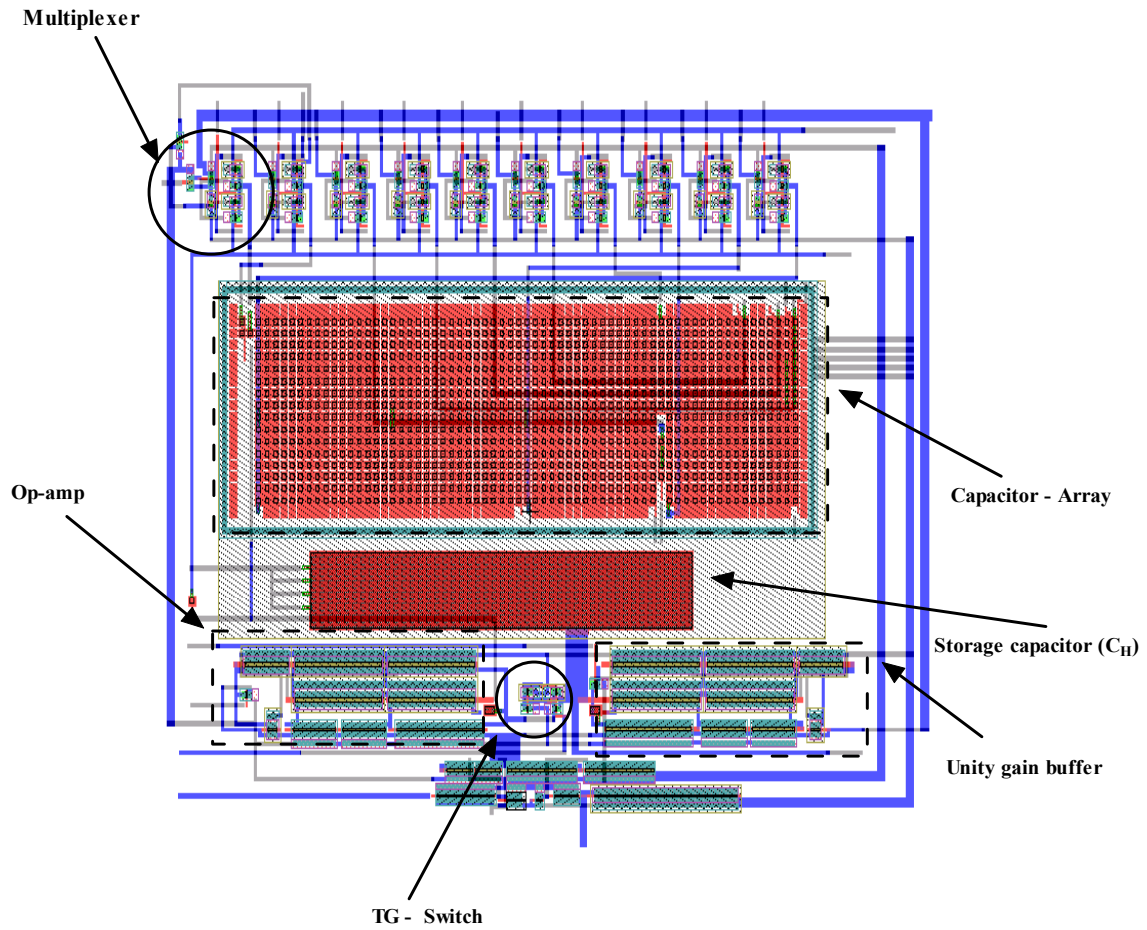
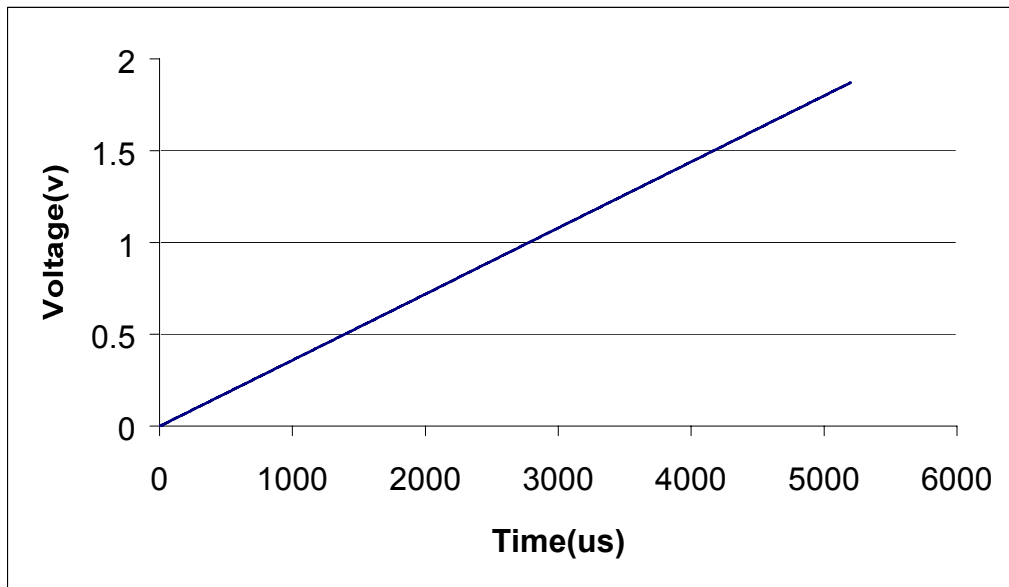
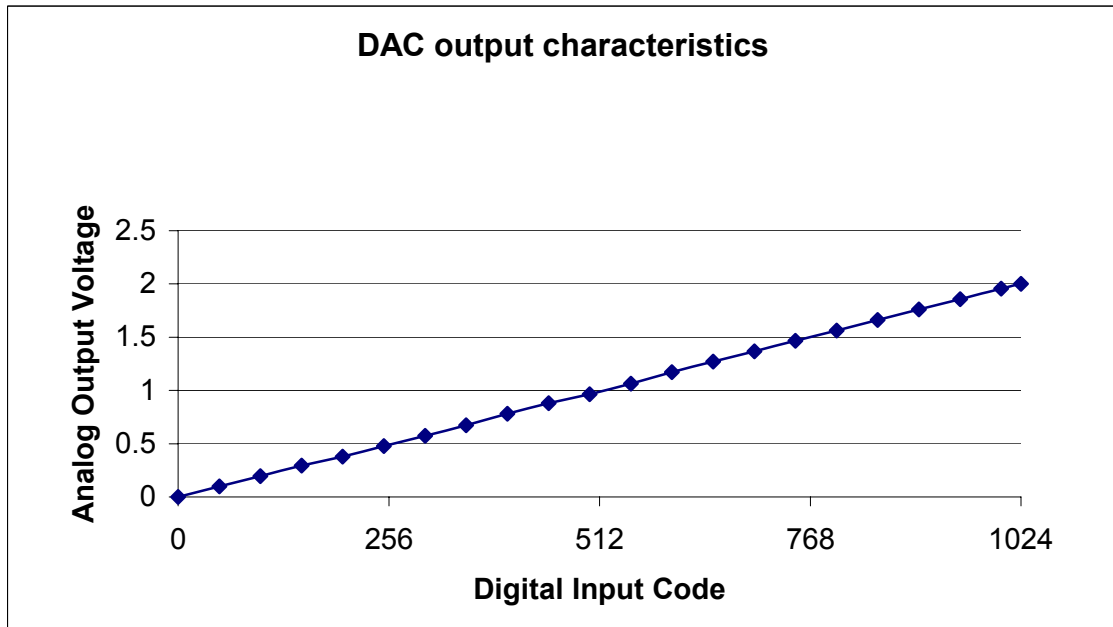


Figure 2.31: Layout of a 10-bit charge-scaling DAC.



(a)



(b)

Figure.2.32 DAC output response for all (0000000000 – 1111111111) combinations of the input digital word.

## Chapter 3

### Built-in Current Sensor Design

This chapter focuses on  $I_{DDQ}$  testing using built-in current sensors (BICS), the design and implementation of the BICS in a 10-bit charge scaling DAC, the fault simulation and detection methodology. It also discusses previously proposed schemes for  $I_{DDQ}$  testing and the important physical faults commonly seen in the design of integrated circuits. Simulations and design considerations for the BICS are also discussed.

#### 3.1 Current Testing in CMOS Integrated Circuits Using BICS

$I_{DDQ}$  testing of CMOS ICs is shown very efficient for improving test quality. The test methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects such as gate oxide shorts, floating gates and bridging faults, which are not very well modeled by the classic fault models, or undetectable by conventional logic tests [1]. In addition,  $I_{DDQ}$  testing can be used as a reliability predictor due to its ability to detect defects that do not yet involve faulty circuit behavior, but could be transformed into functional failures at an early stage of circuit life. Due to obvious quality and reliability improvements, this approach became powerful complement to the conventional logic testing. Quiescent current monitoring is considered as an interesting and efficient technique for mixed-signal testing, where fault detection of analog parts requires the precise measure of the  $I_{DDQ}$ . In analog circuits, the quiescent current, termed as  $I_{PS}$ , may in the order of  $\mu$ As or even mAs. Under fault conditions, the normal values of  $I_{PS}$  may be increased or decreased or generally distorted. Thus, fault detection can be accomplished by monitoring the  $I_{PS}$  current fluctuations. Figure 3.1 shows the fault free  $I_{DDQ}$  current in the quiescent state, which is about 1mA and shooting to 3mA when fault



is injected in the CUT [19]. Elevated  $I_{DDQ}$  does not necessarily result in nonfunctional behavior. However, data are available confirming that  $I_{DDQ}$  failures will result in reliability problems [33]. Considerable impact can be made towards achieving higher quality by incorporating  $I_{DDQ}$  testing along with conventional logic testing.

Built-in current sensors (BICS) have speed and resolution enhancements over off-chip current sensors, mainly because the large transient currents in the output drivers are by-passed and less parasitic are encountered. On chip current testing is both time-efficient and sensitive. Moreover, on-chip current tests can also be used as an on-line testing tool, and is important when components are to be used in high reliability systems. For high speed and high sensitivity, unaffected by large pad currents, a fast built-in current testing circuit is desired [34]. In the present work, a simple design of a built-in current sensor is presented to detect bridging faults in a 10-bit charge scaling DAC. A novel method has been introduced for the fault injection to simulate physical defects present in a chip.

### **3.2 $I_{DDQ}$ Hardware**

$I_{DDQ}$  measurements require analog circuitry that can ideally measure current below 1  $\mu\text{A}$  in the range 10 KHz- 33 MHz [35]. Different methodologies exist for  $I_{DDQ}$  testing.  $I_{DDQ}$  testing can be classified in two groups, 1) external  $I_{DDQ}$  testing and 2) internal  $I_{DDQ}$  testing. External  $I_{DDQ}$  testing monitors power supply current through the power pins of the integrated circuit package while internal  $I_{DDQ}$  testing monitors power supply current built-in current sensors [36].

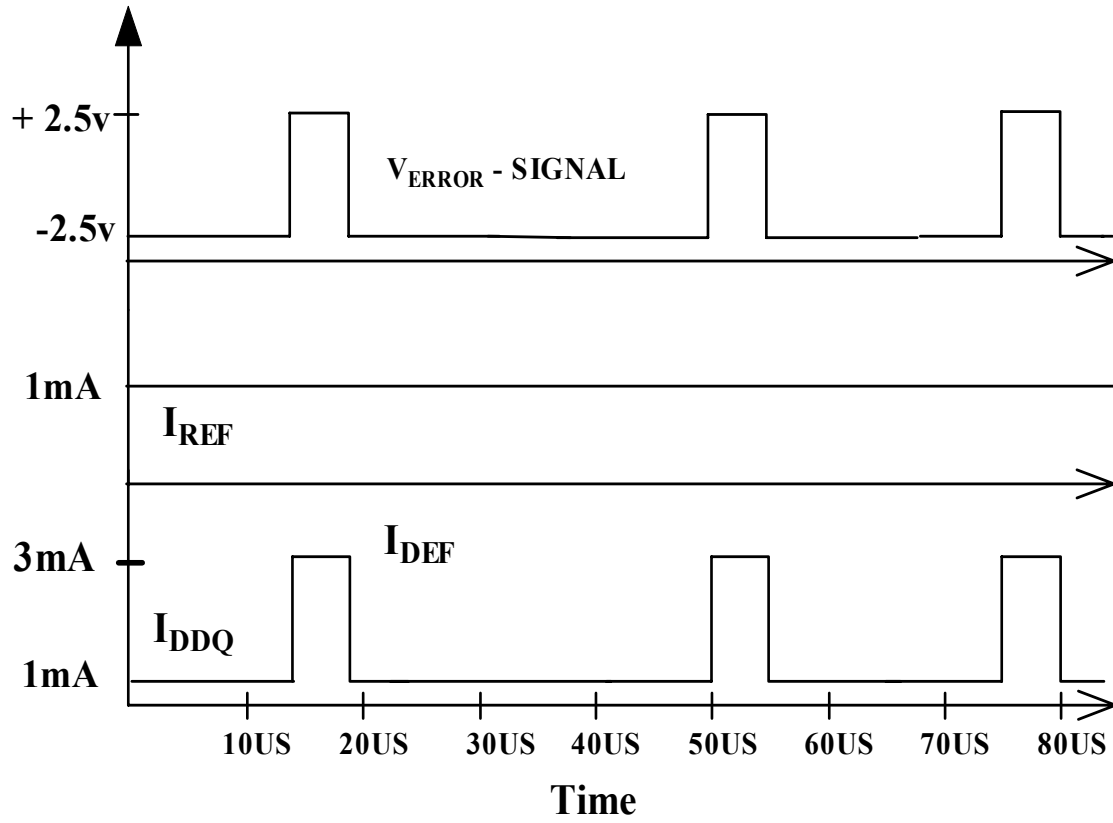


Figure 3.1: Faulty ( $I_{\text{DEF}}$ ) and fault-free ( $I_{\text{REF}}$ )  $I_{\text{DDQ}}$  current.

Note:  $I_{\text{REF}}$  is same as  $I_{\text{DDQ}}$ .  $I_{\text{DEF}}$  is the current in presence of faults.  $V_{\text{ERROR}}$  is the signal output.

### 3.2.1 External $I_{DDQ}$ Testing

The simplest form of hardware for testing is the automatic testing equipment (ATE) precision measurement unit. It can be connected to the CUT's power pin and used to measure  $I_{DDQ}$ . This strategy is acceptable if the number of measurements is less than 20; otherwise test time becomes expensive [1]. Figure 3.2 shows off-chip instrumentation schematic. Figure 3.2 (a) illustrates an approach for an off-chip  $I_{DDQ}$  instrumentation [33]. The tester is connected in series with the  $V_{DD}$  line of the CUT.  $C_{DD}$  is the total capacitance at the  $V_{DD}$  node and includes that due to the IC itself and any capacitance added by the tester and instrumentation circuit. The tester measures  $dV_o/dt$  during the quiescent time and can estimate  $I_{DDQ}$  if  $C_{DD}$  is known using [1].

$$I_{DDQ} = C_{DD} dV_o/dt \quad (3.1)$$

Figure 3.2 (b) shows another schematic for off-chip  $I_{DDQ}$  current measurement [35]. An off-chip sensor monitoring the power supply current is a simple implementation of  $I_{DDQ}$  testing and widely used in production testing. The transistor  $Q_1$  is ON only during transient when the CUT is drawing large currents. To filter the high impedance noise at high frequencies, a small capacitor  $C_1$  in the range of 2-2.5nF is added in between the sense circuit and the CUT [37]. Once transients are settled, the  $Q_1$  is OFF and capacitor  $C_1$  supplies the static current to the CUT.  $I_{DDQ}$  is measured by the voltage drop across the transistor  $Q_1$ .

Off-chip current measurement technique has the ability to detect vast majority of manufacturing defects, including those that are not detected by the traditional stuck-at fault testing [34]. However, off-chip measurement techniques have speed and sensitivity

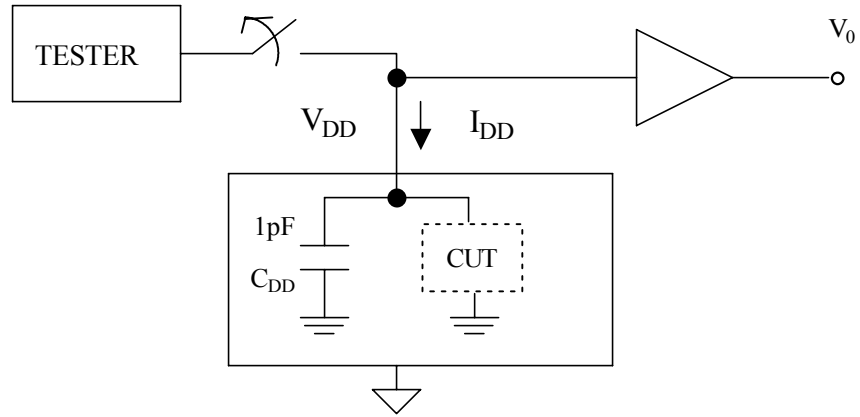


Figure 3.2 (a): Off-chip  $I_{DDQ}$  current measurement using an automatic test equipment.

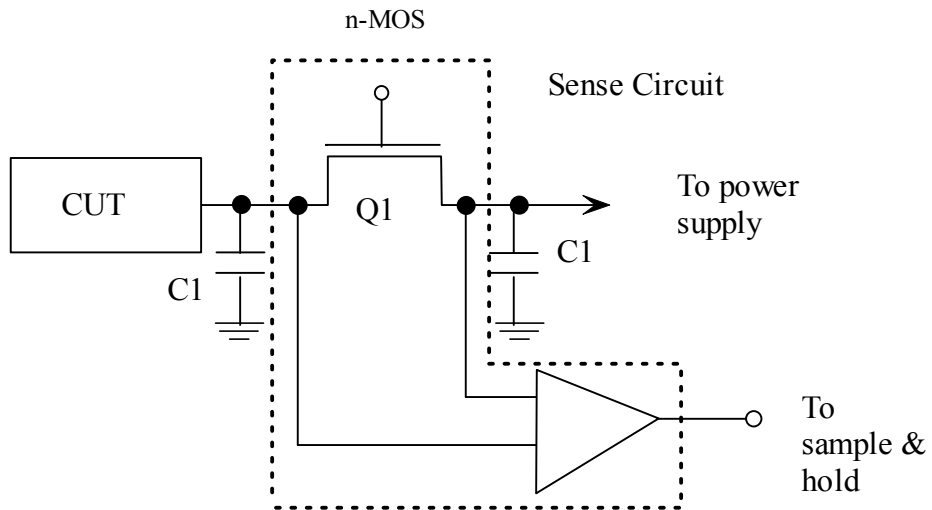


Figure 3.2(b): Off-chip  $I_{DDQ}$  current measurement.

limitations [38]. Low-current resolution is critical in detecting defects such as floating gates, which do not cause large abnormal currents. Off-chip measurements may not detect this small current due to its sensitivity limitations. Several other factors can degrade off-chip  $I_{DDQ}$  instrumentation. 1) All testers have current probes, which offer significant capacitive loading at the power supply, causing a large voltage drop across it, and lack in DC accuracy [1,20]. 2) The test board exists in a noisy electrical environment and long leads are used and electromagnetic fields are high [35]. Current measurement is slow and susceptible to static noise in the power supply bus. Considerable noise is therefore introduced into the measurement. 3) Above all, the major portion of the  $I_{DDQ}$  current in CMOS VLSI chips is generated at the output pad circuits, and abnormal  $I_{DDQ}$  current is overshadowed by the output currents [36]. Owing to these limitations with off-chip current measurements, the built-in current sensor is a preferred approach in many applications. It can be integrated in to the CMOS design to test for physical faults in the circuit.

### **3.2.2 Internal $I_{DDQ}$ Testing**

The effectiveness of  $I_{DDQ}$  testing can be enhanced if built-in current sensors are applied on chip to monitor defect –related abnormal currents in the power supply buses [34]. This testing technique applies on-chip current sensors that detect abnormal power bus currents and overcomes the limitations of the off-chip  $I_{DDQ}$  current measurements. Essentially, this technique adds a BIC sensor in series with  $V_{DD}$  or GND lines of the circuit under test. A series of input stimuli is applied to the device under test while monitoring the current of the power supply ( $V_{DD}$ ) or ground (GND) terminals in the quiescent state conditions after the inputs have changed and prior to the next input change

[35]. Figure 3.3 shows the block diagram of the  $I_{DDQ}$  testing with BICS. The many advantages of BICS over the off-chip current testing or the ATE, include: reduction of test equipment cost, increase of testing rate, improvement of the detectability and high current sensing resolution [38].

Typically, sub-threshold current in the transistors, which are ‘off’ in a CMOS static circuit should be negligibly small. However, in some cases, due to charge presence in a gate oxide or latch-up, the sub-threshold current may be large enough to become an essential component of  $I_{DDQ}$ . The BICS can be designed to detect this current also.

### **3.3 Physical Faults in CMOS Integrated Circuits**

In CMOS technology, the most commonly observed physical failures are bridges, opens, stuck-at-faults and gate oxide shorts (GOS). These defects create indeterminate logic levels at the defect site [1]. Very large-scale integrated circuits processing defects cause shorts or break in one or more of the different conductive levels of the device [36]. We briefly discuss these physical defects that cause an increase in the quiescent current.

#### **3.3.1 Open Faults**

Figure 3.4 shows a 2-input NAND open circuit defect. Logic gate inputs that are unconnected or floating inputs are usually in high impedance or floating node-state and cause elevated  $I_{DDQ}$  [34]. In Fig. 3.4, node  $V_N$  is in the floating node-state. For an open defect, a floating gate may assume a voltage because of parasitic capacitances and cause the transistor to be partially conducting [37]. Hence, a single floating gate may not cause a logical malfunction. It may cause only additional circuit delay and abnormal bus current [34]. In Fig. 3.4, when the node voltage ( $V_N$ ), reaches a steady state value, then the output voltage correspondingly exhibits a logically stuck behavior and this output value can be

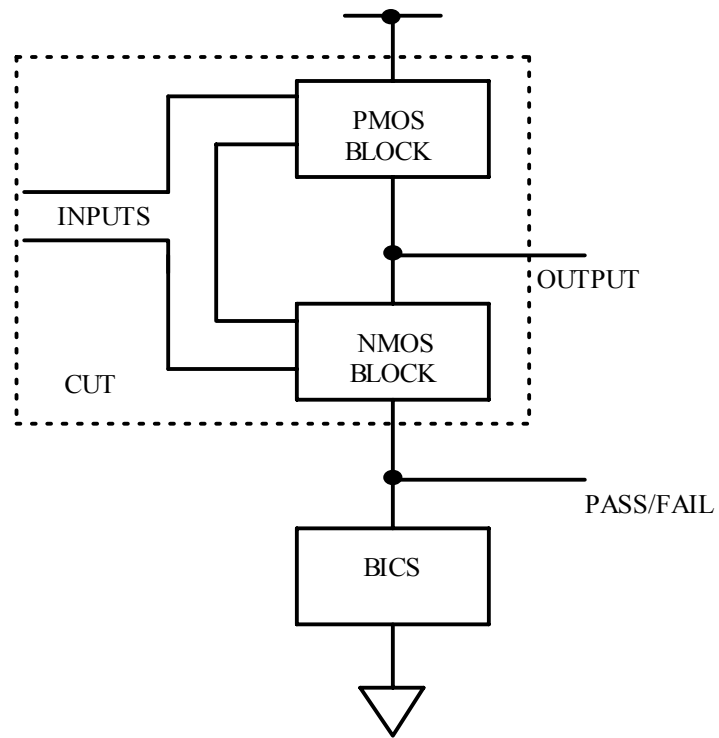


Figure 3.3: Block diagram of  $I_{DDQ}$  testing.

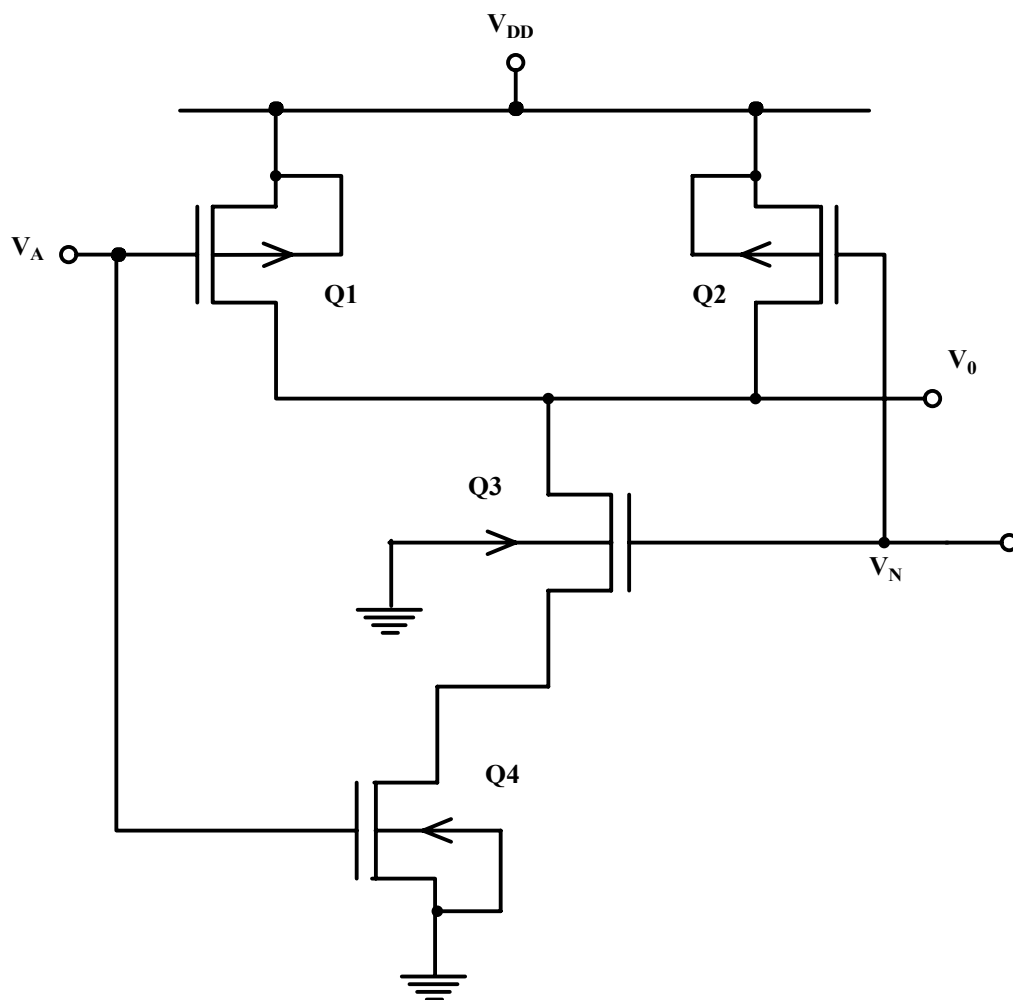


Figure 3.4: Open circuit defect.



weak or strong logic voltage. Open faults, however, may cause only a small rise in  $I_{DDQ}$  current, which the off-chip current sensor may not detect because of its low-resolution [1]. It can be detected using BIC sensors. An open source or open drain terminal in a transistor may also cause additional power-bus current for certain input states. In this scope of work, we deal with bridging faults.

### 3.3.2 Bridging Faults

The short circuit faults in very large-scale integrated circuits are popularly termed as bridging faults. When  $I_{DDQ}$  measurements are used, a bridge is detected if the two nets, which compromise it, have opposite logic values in the fault-free circuit [37] and are connected by a bridge due to the introduction of the fault in the circuit. Bridging faults can appear either at the logical output of a gate or at the transistor nodes internal to a gate. Inter-gate bridges between the outputs of independent logic gates can also occur. Bridging fault could be between the following nodes 1) drain and source, 2) drain and gate, 3) source and gate, and 4) bulk and gate. Examples of bridging fault are shown in Figs. 3.5 and 3.6, respectively. Figure 3.5 shows example of possible drain to source bridging faults in an inverter chain in the form of low resistance bridges ( $R_1$ ,  $R_2$  and  $R_4$ ). Resistance bridge,  $R_3$  is an example of inter-gate bridge. Figure 3.6 shows examples of gate to source and gate to drain bridges in an NAND gate circuit.

Bridging faults can be modeled between adjacent metal lines in a 10-bit charge scaling DAC at different conducting levels. We have introduced faults in the 10-bit charge scaling DAC by using “fault-injection transistors” instead of hard metal shorts invented in our group [19]. The introduction of a fault via the “fault-injection”

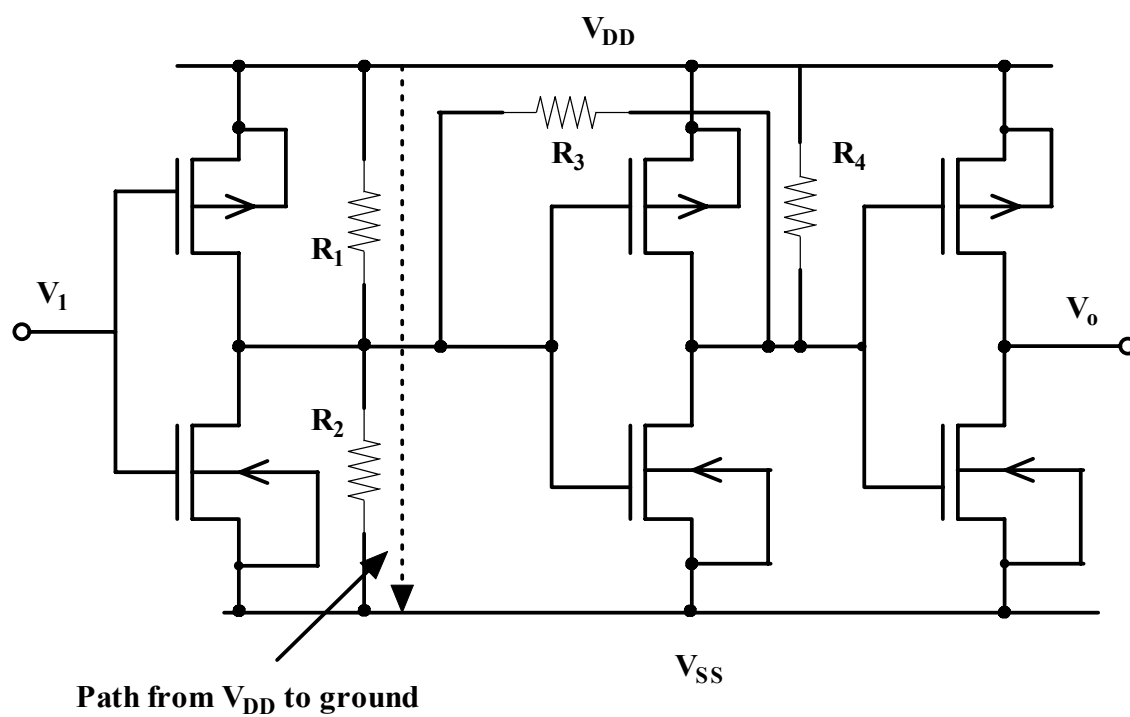


Figure 3.5: Drain-source and inner-gate bridging faults in an inverter chain.

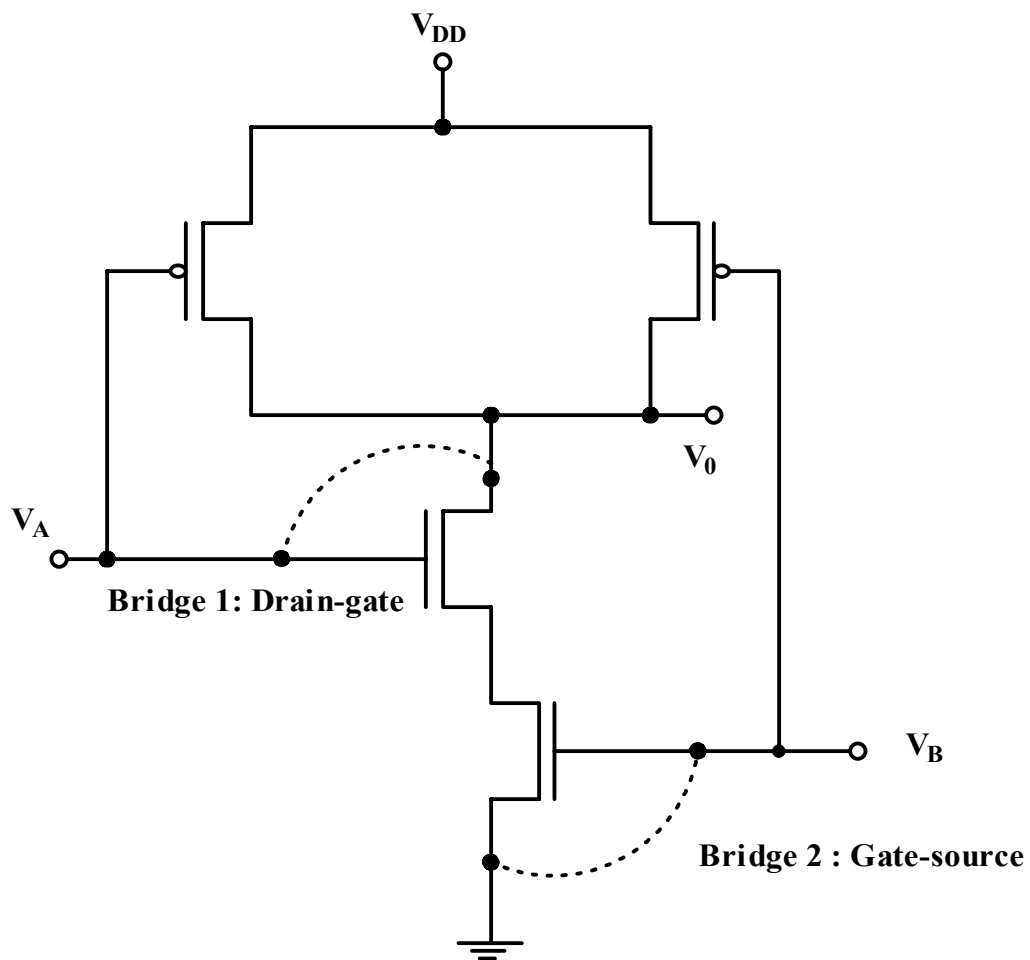


Figure 3.6: Bridging defect.

transistor enables the 10-bit DAC to function fault-free under the normal conditions. The faults considered include source-drain bridge, drain-gate bridge and source-gate bridge. Bridging defect cannot be modeled by the stuck-at model approach, since a bridge often does not behave as a permanent stuck node to a logic value [37].  $I_{DDQ}$  testing using BICS is an effective method of detecting bridging shorts.

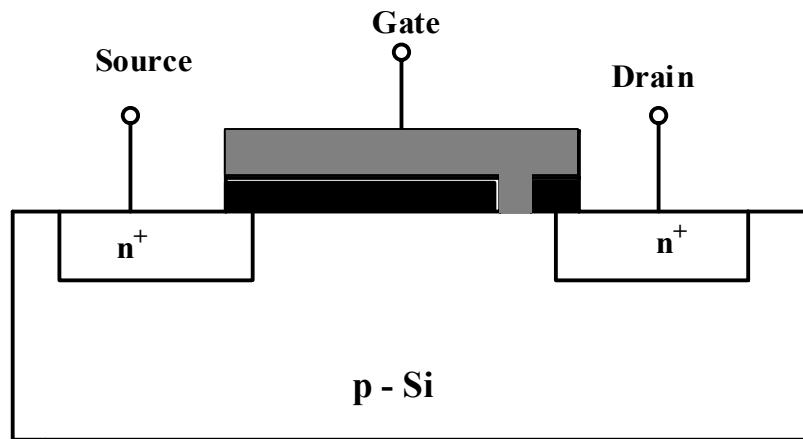
### **3.3.3 Gate-Oxide Short Defects**

Gate-oxide short (GOS) defects occur frequently in CMOS technology. The principle physical reasons for GOS are the breakdown of the gate oxide and the manufacturing spot defects in lithography and processes on the active area and polysilicon masks [38]. Figure 3.7 illustrates the circuit level gate oxide short defect model [37]. These defects can be seen as short-circuits between the gate electrode and the conducting channel of the device through  $\text{SiO}_2$ . GOS short causes an undesirable current injection in to the channel [36, 38]. This current injection forces a substantial increase in the quiescent current. The diode-resistor combination could be used to model the rectifying behavior of the new current path introduced by the defect [38].

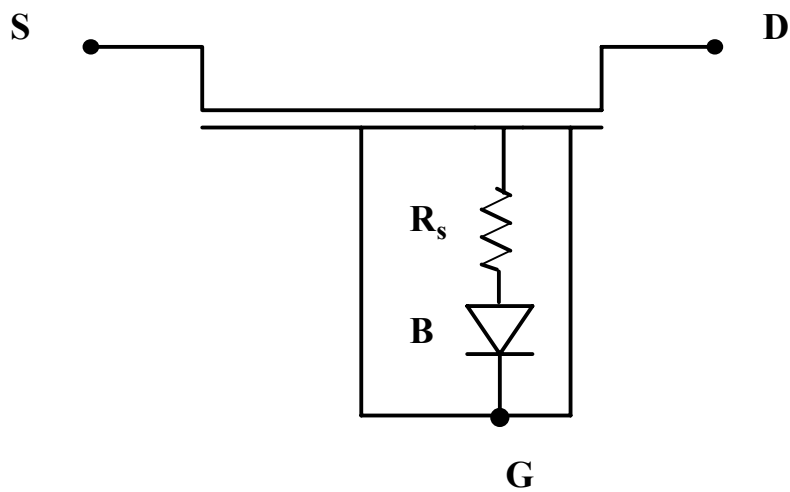
These defects are unlikely to produce logical errors, but cause important deviation of parametric specification especially important in low power equipment [39].

## **3.4 Definition and Description of $I_{DDQ}$ of a Faulty Circuit**

$I_{DDQ}$ 's definition is the level of power supply current in a CMOS circuit when all the nodes are in a quiescent state. Static CMOS circuits use very little power and at stand-by or quiescent state, it draws practically negligible leakage current [35]. In steady state, there should not be a current path between  $V_{DD}$  and GND path. Ideally, in a static CMOS circuit, quiescent current should be zero except for associated p-n junction leakage



(a)



(b)

Figure 3.7(a): Gate-oxide-short (GOS) in a MOSFET.

Figure 3.7(b). Equivalent circuit model.  $R_s$  is the effective resistance of the short. **B** models the rectifying behavior of new current path introduced by the defect.

currents. Any abnormal elevation of current should indicate presence of defects. To assure low stand-by power consumption, many CMOS integrated circuit manufacturers include  $I_{DDQ}$  testing with other traditional DC parametric tests [36].

### 3.4.1 Description of $I_{DDQ}$ of a Faulty Inverter

Figure 3.8 shows how an  $I_{DDQ}$  test can identify defects. The current in static CMOS is not constant during transient [40]. When an output transition occurs, a peak of  $I_{DDQ}$  current is observed. This peak is due to charging and discharging of the load capacitance at the output circuit and corresponds to the short circuit. When the transition is completed, the circuit is in the quiescent state.  $I_{DDQ}$  is very sensitive to physical faults in the circuit. In mixed-signal CMOS circuits such as data converters,  $I_{DDQ}$  is around 1mA, which increases in presence of defects.

Let us evaluate current testing in CMOS circuits in the presence of bridging faults. Two nodes connected by a bridge must be driven to opposite logic levels under fault-free conditions for bridging fault to occur. In Fig.3.8, a typical bridge is one between the node  $V_O$  and  $V_{DD}$ . To detect this defect, input pattern must drive the node  $V_{O1}$  to the logic low value ('0'), as this node is assumed to be bridged with the power rail. Thus, a path from power to ground appears allowing the existence of an abnormal high  $I_{DDQ}$  current.  $I_{DDQ}$  value is directly dependent on the resistance offered by the conducting path and hence on the size of the transistors in the conducting path. The presence of the physical fault causing the high abnormal current can be effectively detected by  $I_{DDQ}$  testing using BICS. A set of realistic bridges have been modeled between adjacent metal lines in a 10-bit charge scaling DAC at three different (conducting levels), to

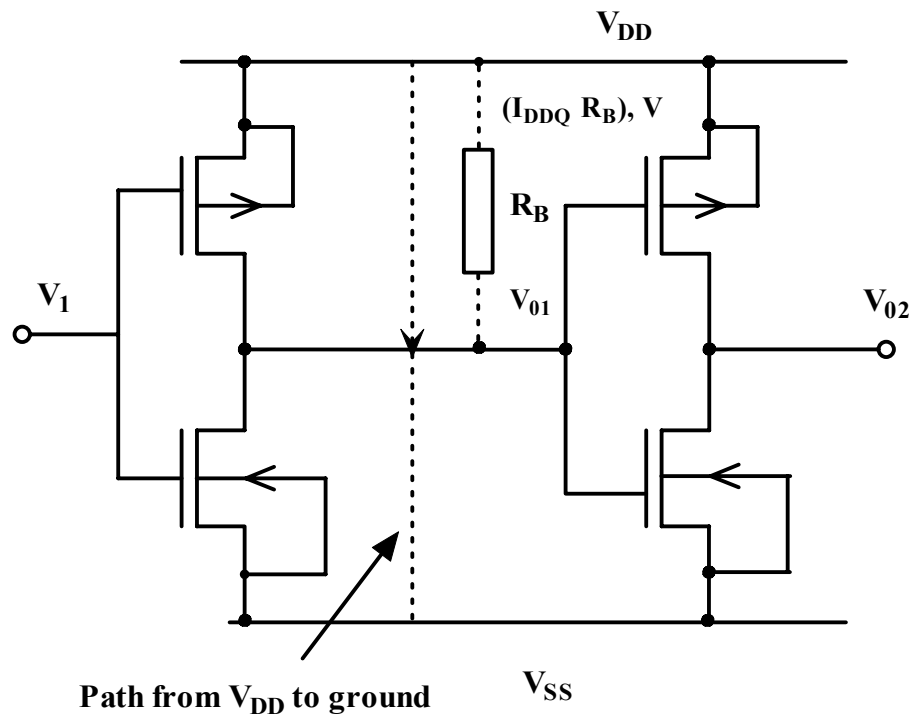


Figure 3.8: Bridging fault causing  $I_{DDQ}R_B$  drop and a path to the ground.

examine the effect on the value of  $I_{DDQ}$  and detect the presence of the fault using the BICS.

### **3.5 The Design Considerations of BICS**

A simple design of a BIC sensor built into the 10-bit charge scaling DAC is presented using the current mode design. It determines whether the circuit quiescent current is below or above a threshold level. Previously proposed schemes and the characteristics required for a good BICS are discussed briefly in this section.

#### **3.5.1 Previously Proposed Schemes**

Different BICS schemes have been proposed for detection of the abnormal  $I_{DDQ}$  current and the physical faults commonly observed. While most BICS designs concentrate on mere detection of the fault, some can detect the location of the fault as well [41]. The entire design is divided into  $n$  sub blocks (SB) where  $n$  equals the number of outputs. The divided SB's are checked individually through their corresponding output and a faulty area is easily detected by observing the outputs. The performance impact of a BICS on a circuit under test (CUT) is the key issue to be considered when designing BICS. Insertion of the BIC sensor between CUT and GND involves series voltages, and these voltages could degrade the performance of the CUT [40,11]. A large number of earlier BICS are based on voltage amplifiers such as differential amplifiers or sense amplifiers. The stability of the BICS is limited in this case since the quiescent point (Q-point) of an amplifier may not be stable and can vary with the change of dc supply voltage,  $V_{DD}$ . The detection time and hardware overhead is increased due to the extra hardware required to stabilize the Q-point.



To overcome problems of slow detecting time, resolution, instability of the BICS and large impact on the CUT performance, the current-mode circuit design approach has been adopted using a single power supply. In this work, simple design of a BICS employing current mirrors and current differential amplifier has been proposed. It has minimum area overhead in the chip and no impact on overall performance.

Characteristics required for a good BIC sensor are [39]:

1. Detection of abnormal static and dynamic characteristics of the CUT.
2. Minimal disturbance of the static and dynamic characteristics of the CUT.
3. The design should be simple and compact to minimize the additional area necessary to build it.
4. The  $I_{DDQ}$  test should have good resolution and speed.

### 3.5.2 The Design of the BICS

Figure 3.9 shows the CMOS circuit diagram of the built-in current sensor. It consists of a current differential amplifier ( $M_2, M_3$ ), two current mirror pairs ( $M_1, M_2$  and  $M_3, M_4$ ) and an inverter. The n-MOS current mirror ( $M_1, M_2$ ) is used to mirror the current from the constant current source which is used as the reference current  $I_{REF}$  for the BICS. The current mirror ( $M_3, M_4$ ) is used to mirror the difference current ( $I_{DEF}-I_{REF}$ ) to the current inverter, which acts as a current comparator. The differential pair ( $M_2, M_3$ ) calculates the difference current between the reference current  $I_{REF}$  and the defective current  $I_{DEF}$  from the CUT. The W/L size of the n-MOS current mirrors ( $M_1, M_2$ ) is set to 27/1.6 and ( $M_3, M_4$ ) is set to 72/1.6. Therefore  $I_{D3} = I_{DEF}-I_{REF}$ . The constant reference current is set to approximately the same value as the quiescent state current when the

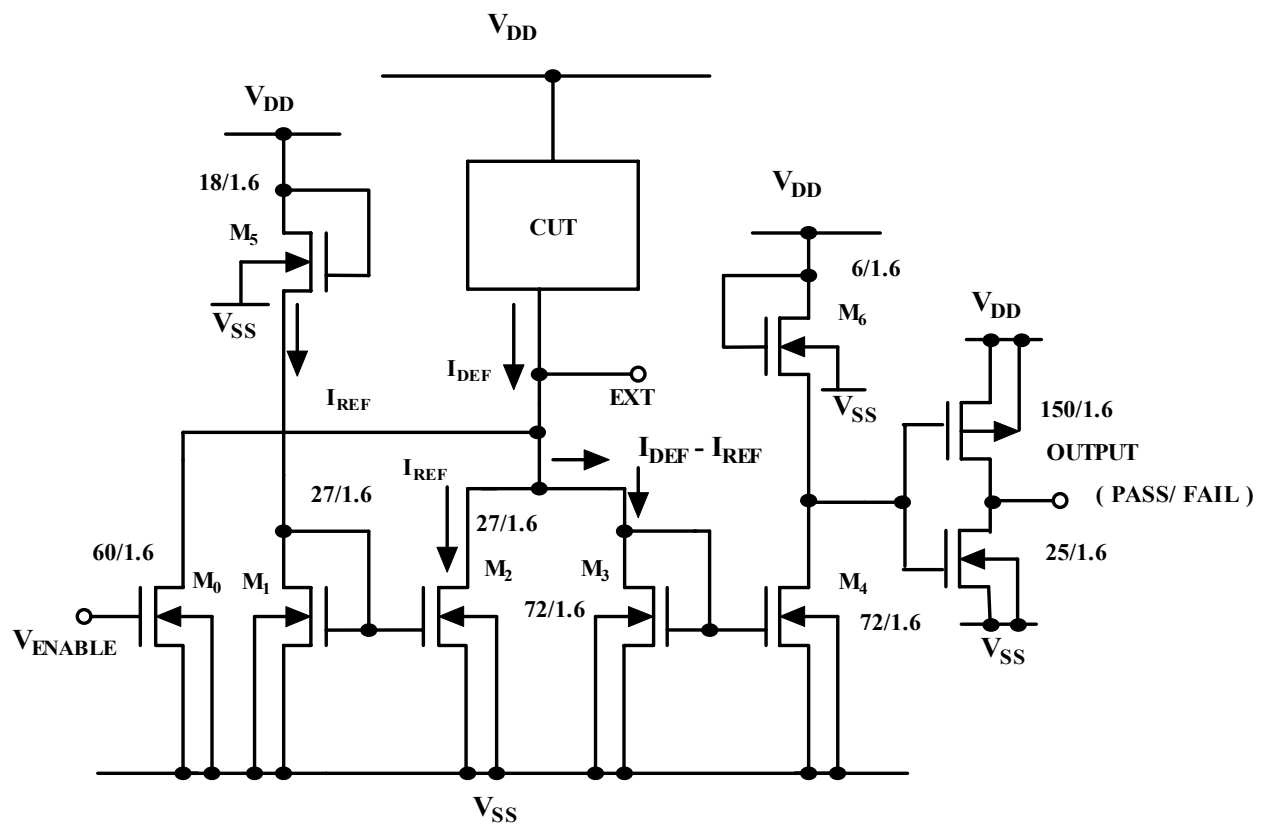


Figure 3.9: CMOS built-in current sensor circuit.

CUT is fault free. In the present design, the reference current,  $I_{REF}$  is set to 1mA. The output inverter buffer has an aspect ratio  $((W/L)_P / (W/L)_N)$  of 6/1 to counter capacitive parasitics at the output node and detect the presence of the physical fault through the PASS/FAIL flag at the output.

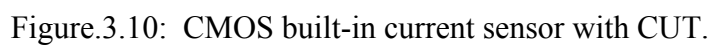
The proposed scheme operates in two modes: the normal mode and the test mode. The mode of operation is controlled by ' $V_{ENABLE}$ ' signal applied to the gate of transistor  $M_0$ . The W/L size of the  $M_0$  is 60/1.6. This enables the 10-bit charge scaling DAC, which is the CUT to operate as fault-free in the normal mode of operation. Further explanation on the design is provided in section 3.6.

### 3.6 The Implementation of BICS

Figure 3.10 explains the basic structure of the BIC sensor connected between CUT and GND in  $I_{DDQ}$  testing. The BICS is inserted in series with GND or  $V_{SS}$  line of the circuit under test. The proposed BICS works in two modes: the normal mode and the test mode. The mode of operation is decided by the  $V_{ENABLE}$  signal. In the normal mode ( $V_{ENABLE} = '1'$ ), the BICS is isolated from the CUT. In the test mode ( $V_{ENABLE} = '0'$ ), the quiescent current from the CUT is diverted in to the BICS and compared with reference current to detect the presence of the fault.

#### 3.6.1 BICS in Normal Mode

During the normal operation, the signal ' $V_{ENABLE}$ ' is at logic '1' and all the  $I_{DD}$  current flows to ground through  $M_0$  (control transistor). When switching occurs,  $M_0$  is turned on. Therefore, the n-MOS current mirrors have no effect on dynamic current. It follows that the BICS's output is not affected by the dynamic current. Thus, in the normal mode, the BICS is totally isolated from the 10-bit DAC (CUT). Since in normal mode the



current coming from the CUT is same as the reference current the difference current  $I_{DEF} - I_{REF}$  becomes negligible and the output of the BICS is at logic '0'. In the normal mode, it cannot detect the presence of any physical fault in the CUT.

Since the BICS is inserted in series with GND line of the CUT, it causes a voltage drop and large capacitance between the CUT and the substrate. These effects cause performance degradation and ground level shift. To reduce these extra undesirable effects, an extra pin EXT is added to the proposed BICS. Pin EXT is connected to the drain of transistor  $M_0$ . In the test mode, it is left floating. In the normal mode, EXT gets connected to logic '0'. In the normal mode, since the EXT pin is grounded by passing the BICS, the disturbance of the ground level shift during normal operation of the circuit never happens. Therefore, there is no impact on the performance of the DAC, while the BICS is in normal mode.

### **3.6.2 BICS in Test Mode**

During the test mode, the ' $V_{ENABLE}$ ' signal is at logic '0'. The  $I_{DDQ}$  current from the CUT is diverted by the BICS and the n-MOS current mirror pair replicates the reference current to the current differential amplifier which assigned a value nearly same as the fault-free current. This mirrored reference current is compared with defective current  $I_{DEF}$  current coming from the CUT. The output of the current comparator, which is in the form of PASS/FAIL, will detect the presence of the fault.

The difference current is converted to a voltage by mirroring it and getting the drop of  $V_{DS}$  across the transistor  $M_4$ . In the test mode, the difference current is large which turns-ON  $M_4$  heavily and forces its output node pulled-down to logic '0' and is detected as PASS/FAIL output '1', indicating presence of defects in CUT. In the testing

mode, EXT pin is floating. The 'V<sub>ENABLE</sub>' signal is connected to GND and M<sub>0</sub> is off. The timing diagram and detailed analysis of BICS are explained in the following sections.

### 3.6.3 Detailed Analysis of the BICS

The current differential amplifier and the current mirror are most important parts of the proposed BICS. Performance of the current mirror greatly affects the BICS's ability to detect abnormal current due to physical defects. The current mirror has a property that, in a constant current stage, the reference current in one branch of the circuit is mirrored in the other branch [22]. The current differential amplifier on the other hand receives reference current I<sub>REF</sub> one input, and the defective current I<sub>DEF</sub> from CUT as the other input. The differential amplifier calculates the difference between the two currents. The other n-MOS current mirror mirrors the difference current calculated by the current differential amplifier to the inverter (M<sub>4</sub>, M<sub>6</sub>) which acts as comparator (Fig.3.10). The output of the current comparator is used as the PASS/FAIL flag. If the I<sub>DDQ</sub> is greater than the reference current, we presume there are defects within the functional circuit. If the I<sub>DEF</sub> is less than the I<sub>REF</sub>, we assume that the functional circuit is free from physical defects that induce abnormal I<sub>DDQ</sub> current. Functionally, in inverter,  $I_D = |I_{REF} - I_{DEF}|$ . If  $I_{DEF} > I_{REF}$ , then the PASS/FAIL output shows a logic '1'. Conversely if  $I_{DEF} < I_{REF}$ , a logic '0' will appear at the PASS/FAIL output. Input impedance of the inverter is very large [23]. Because of the high input impedance of the current comparator and the utilization of the current mirror along with current differential amplifier, even a very small difference between I<sub>DEF</sub> and I<sub>REF</sub> can be distinguished. That means the BICS can achieve a high resolution. Several SPICE simulations were performed to determine the functionality and performance of the BICS design.

### 3.7 Layout, Simulation and Timing Diagrams for BICS

#### 3.7.1 Current Mirror Circuit

The simplest form of constant current source consists of current mirrors constructed by passing a reference current through a diode-connected (gate tied to drain) transistor as shown in Fig. 3.11. The voltage developed across the diode-connected transistor provides the constant current output. The current ratio  $I_{OUT} / I_{REF}$  is determined by the aspect ratio of the transistors in the current mirror circuit design. Both n-MOS transistors have the same W/L ratio of 27/1.6. The output current of the current mirror circuit mirrors the input current to it. Therefore,

$$I_{OUT} / I_{REF} = 1 \quad (22)$$

In our design,

$$I_{OUT} = I_{REF} = 1\text{mA}.$$

#### 3.7.2 Current Differential Amplifier

The current differential amplifier used in our design is the most important part of the BICS. The current differential amplifier calculates the difference between the reference current  $I_{REF}$  and defective current  $I_{DEF}$ . Figure 3.12 shows the circuit diagram of differential amplifier. The currents  $I_{REF}$  ( $i_1$ ) and  $I_{DEF}$  ( $i_2$ ) are the input currents of the amplifier. The difference current ( $I_{DEF} - I_{REF}$  or  $i_2 - i_1$ ) is calculated and mirrored to output of the current differential amplifier. The BICS design comprises of two n-MOS current mirrors and a current differential amplifier. One n-MOS current mirror provides the reference current as one input to the differential amplifier and the other input current comes from the CUT. The other n-MOS current mirror replicates the difference current to

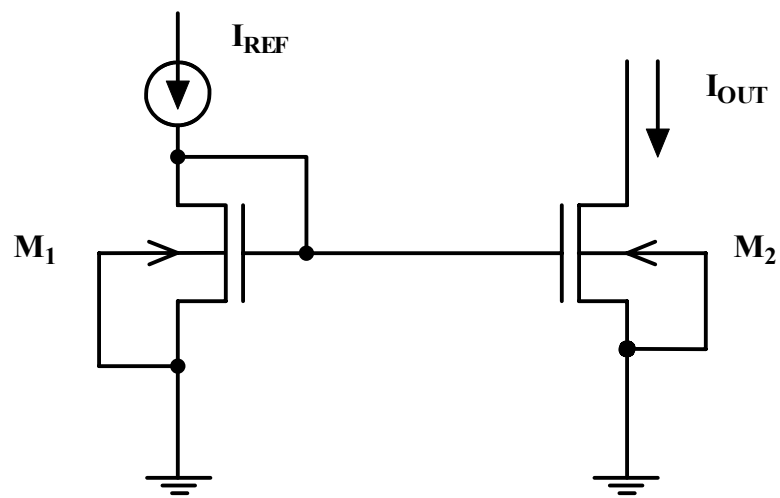


Figure 3.11: n-MOS current mirror circuit.



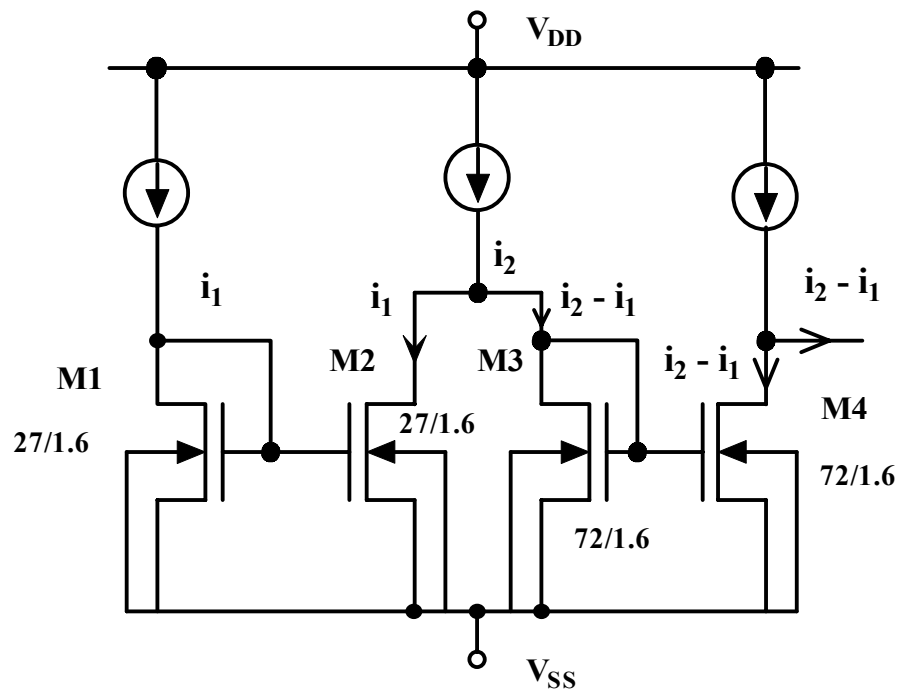


Figure 3.12: Schematic of a current differential amplifier.

the output inverter which acts as a current comparator. The proper design of the current mirrors is most crucial for working of the BICS. The input impedance of the current differential amplifier is simply the small-signal resistance of a diode connected MOSFET, and is given by

$$R_{in} = 1/g_m. \quad (23)$$

The current differential amplifier finds applications in both low-power and high-speed circuit design.

### 3.7.3 BICS

Figure 3.9 shows the circuit diagram of the BICS. It comprises of two current differential amplifiers and a current comparator. It operates in two modes: 1) normal mode and 2) test mode. The test signal is applied to an n-MOS transistor,  $M_0$  ( $W/L = 60/1.6$ ), which decides the mode of operation. When the test signal is '0', the BICS is in the test mode. When the test signal is at logic '1', the BICS is isolated from the CUT and its output is at logic '0'. The output inverter buffer has an aspect ratio  $((W/L)_p/(W/L)_N)$  of 6/1. Figure 3.13 shows the layout of the BICS of the circuit shown in the Fig. 3.9.

## 3.8 Fault Detection, Simulation and Testing

The primary reason for a fault is a defect in the integrated circuit. A manufacturing defect causes unacceptable discrepancy between its expected performance at circuit design and actual IC performance after physical realization [34]. A defect may be any spot of missing or extra material that may occur in any integrated circuit layer.

Two nodes are connected if there is at least one path of conducting transistors

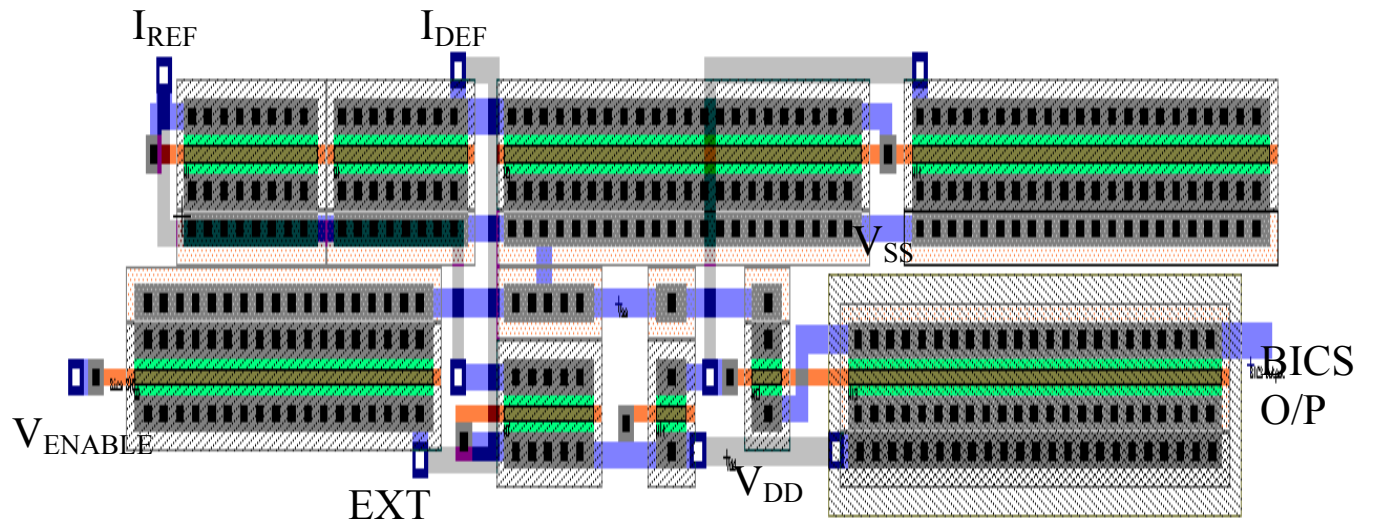


Figure 3.13: Layout of a built-in current sensor circuit.

between them. If the two nodes are at opposite potentials under fault-free conditions, a conducting path between them will increase the  $I_{DDQ}$  current due to fault in the circuit.

After transient switching, each node in a digital circuit is one of the following four states

1.  $V_{DD}$  state: This state occurs when the node is connected to  $V_{DD}$ .
2. GND state: This state occurs when the node is connected to GND.
3. Z state: The high-impedance state occurs when the node is neither  $V_{DD}$  nor GND connected.
4. X state: This state occurs when the node is both  $V_{DD}$ -connected and GND-connected [34].

The ‘X’ state should never occur in fault-free CMOS integrated circuits. Many defects cause an X state to occur in CMOS integrated circuits. Thus, we can view testing as a way to detect the X state, which causes detectable abnormal steady state current. Bridging faults have been induced in the DAC at various conducting levels using a fault-injection transistor (FIT), discussed further ahead, which cause abnormal elevation of the steady state current.

### **3.8.1 Fault-Injection Transistor**

In this work, four bridging faults have been placed in the 10-bit DAC design using fault-injection n-MOS transistors. Activating the fault-injection transistor activates the fault. The use of a fault-injection transistor for the fault simulation prevents permanent damage to the 10-bit DAC by introduction of a physical metal short. This enables the operation of the DAC without any performance degradation in the normal mode. Figure 3.14 (a) shows the fault-injection transistor. To create an internal bridging fault, the fault-injection transistor is connected to opposite potentials. When the gate of fault-injection transistor

$M_E$ ) is connected to  $V_{DD}$ , a low resistance path is created between its drain and source nodes and a path from  $V_{DD}$  to GND is formed. In the Fig. 3.14(b), an internal bridging fault is created in the CMOS inverter between the drain and source nodes using the fault-injection transistor. Logic '0' is applied at the input of the inverter. Therefore, the output of the inverter is at logic '1' or  $V_{DD}$ . When the logic '1' is applied to the gate ( $V_E$ ) of the n-MOS fault-injection transistor ( $M_E$ ), it turns on. This causes a low resistance path between the output of the inverter and the  $V_{SS}$ . This gives rise to an excessive  $I_{DDQ}$  current as a path from  $V_{DD}$  to GND is created, which can be detected by the BICS.

Figure 3.15 shows the layout of a 10-bit charge scaling DAC with BICS. The area of the DAC alone is  $692 \times 502 \mu m^2$ . The entire area of the CUT along with BICS is  $692 \times 516 \mu m^2$ . Therefore the BICS occupies only  $242 \times 40 \mu m^2$  of the entire chip area. Four defects have been introduced using fault-injection transistors. The n-MOS fault-injection transistor ( $M_E$ ) is designed for W/L equal to 4.5/1.6. The fault-injection transistors are activated externally using ERROR signals  $V_{E1}$ ,  $V_{E2}$ ,  $V_{E3}$  and  $V_{E4}$ , respectively. Error signal  $V_{E1}$  is applied to the gate of the fault-injection transistor in defect 1, which forms a short between the source and drain in the operational amplifier circuit shown in Fig. 3.16. Error signal  $V_{E2}$  is applied to the gate of the fault-injection transistor in defect 2, which forms a short between the drain and gate in the unity gain buffer circuit shown in Fig. 3.17 for S/H. Error signal  $V_{E3}$  is applied to the gate of the fault-injection transistor in defect 3, which forms a short between the gate and the source in the multiplexer circuit shown in Fig. 3.18. Error signal  $V_{E4}$  is applied to the gate of the fault-injection transistor in defect 4, which forms a short between the gate and the substrate in the multiplexer circuit shown in Fig. 3.19.

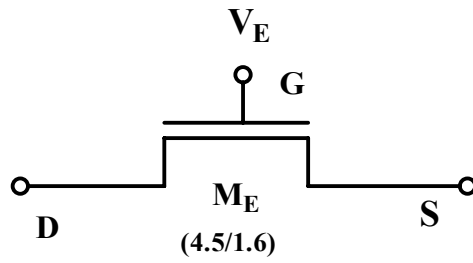


Figure 3.14 (a): Fault-injection transistor (FIT).

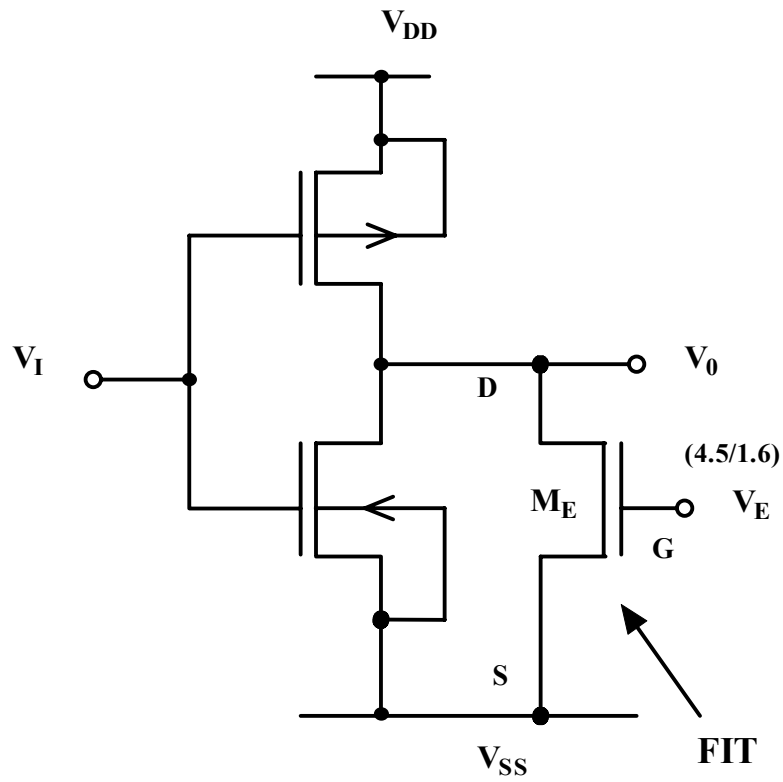


Figure. 3.14 (b) Fault-injection transistor between drain and source nodes of a CMOS inverter.

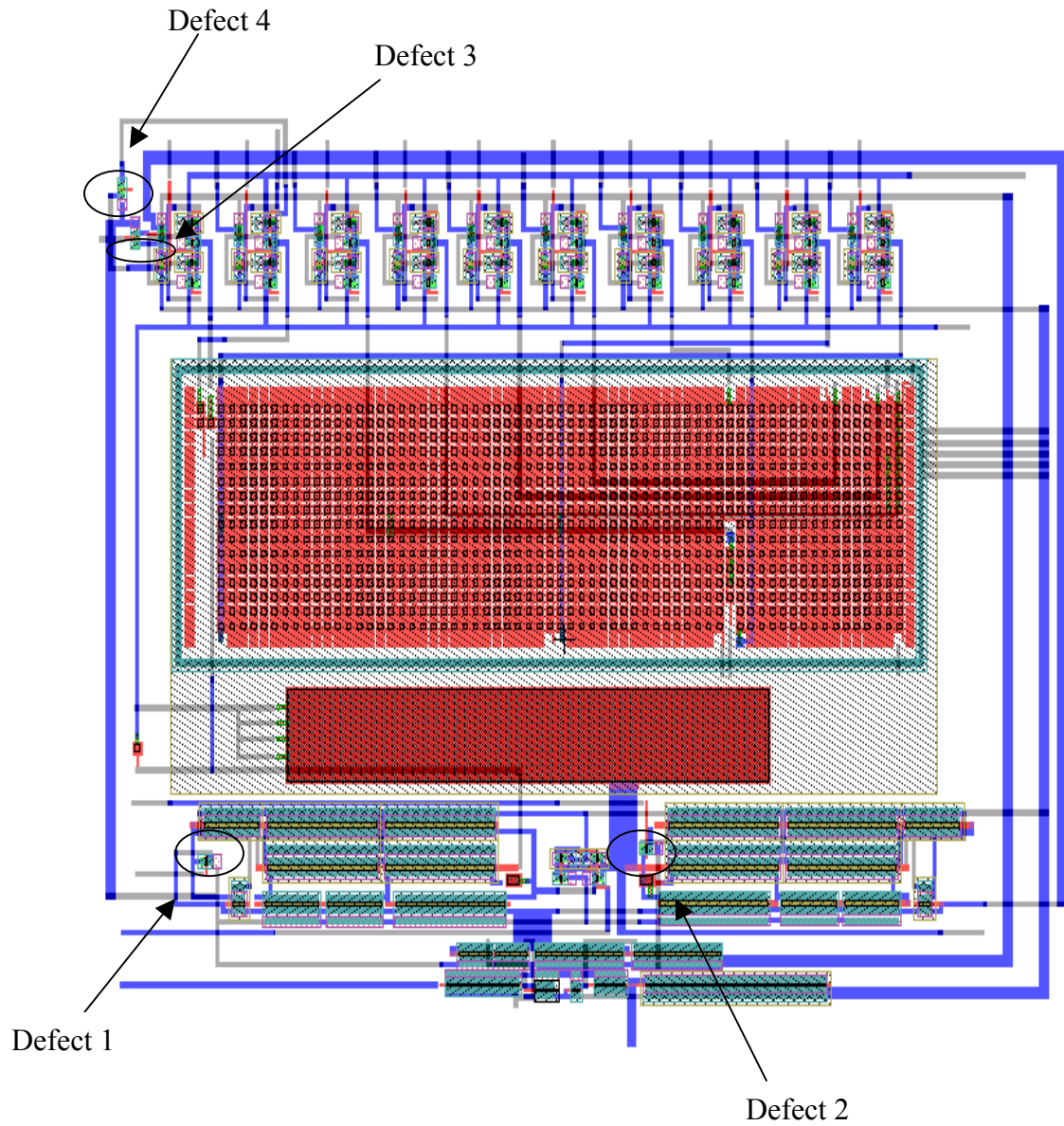


Figure 3.15: Layout of a 10-bit DAC with BICS showing the defects induced in the CUT using fault-injection transistors.

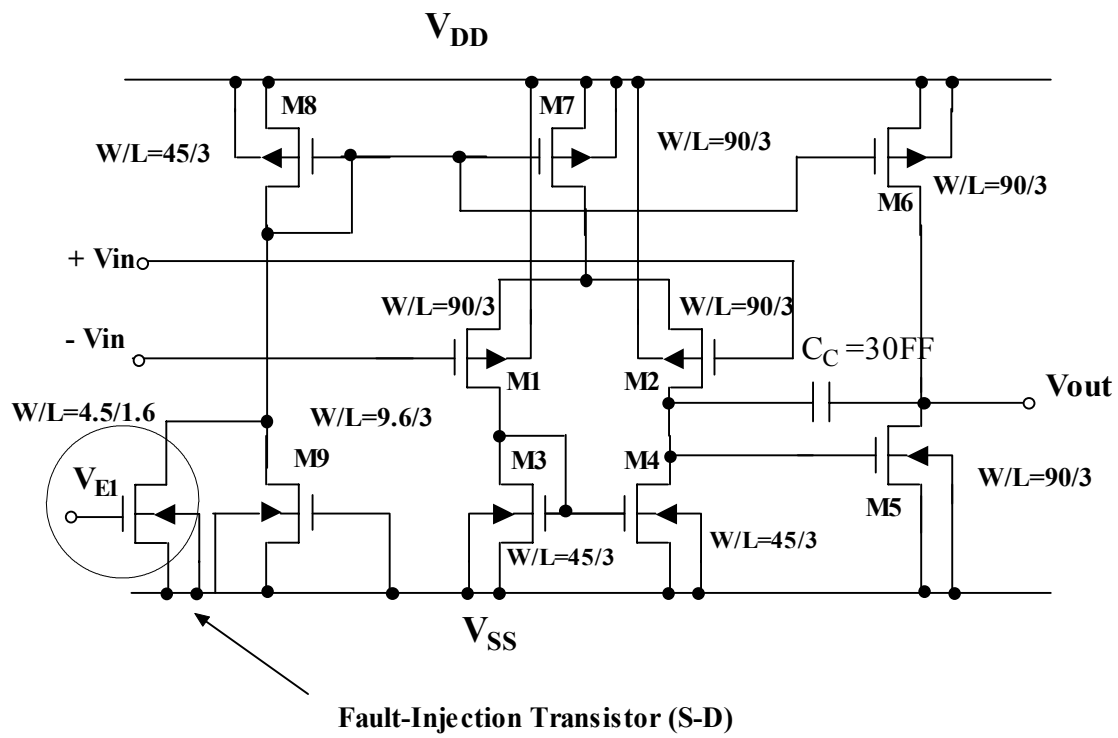


Figure.3.16: CMOS operational amplifier circuit with defect 1 introduced using a FIT.



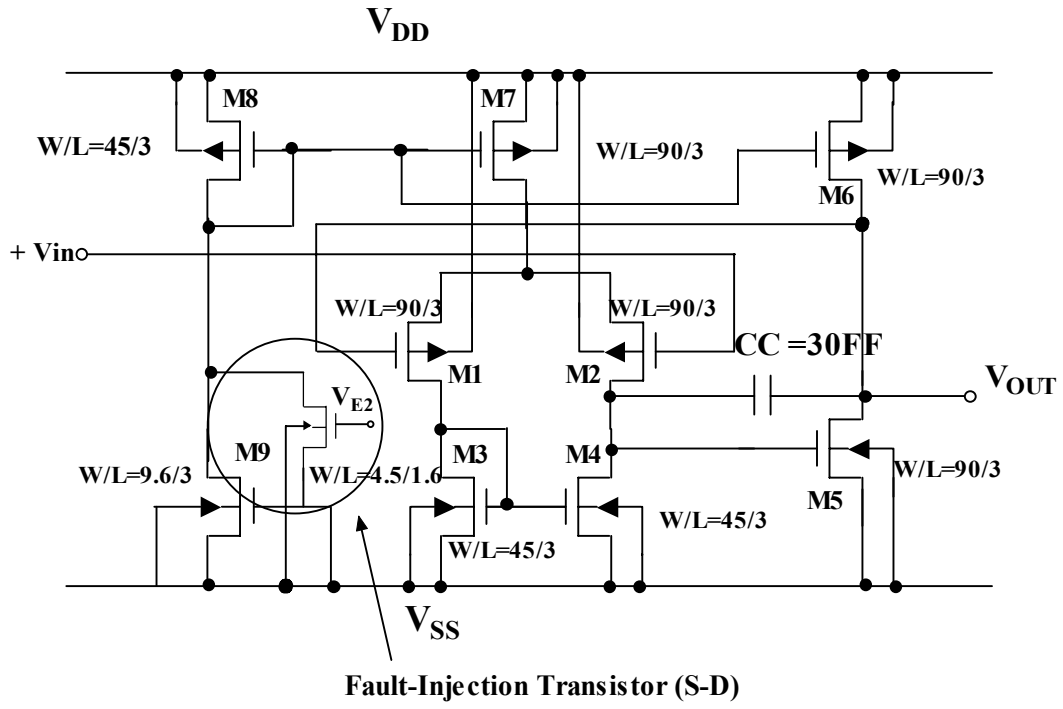


Figure 3.17: CMOS unity gain buffer circuit for S/H with defect 2 introduced using a FIT.

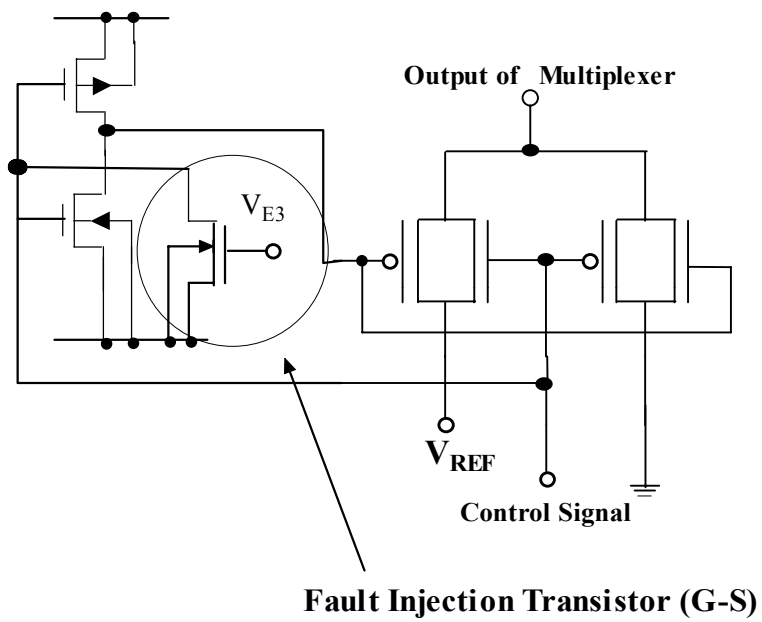


Figure 3.18: CMOS MUX circuit with defect 3 introduced using a FIT.

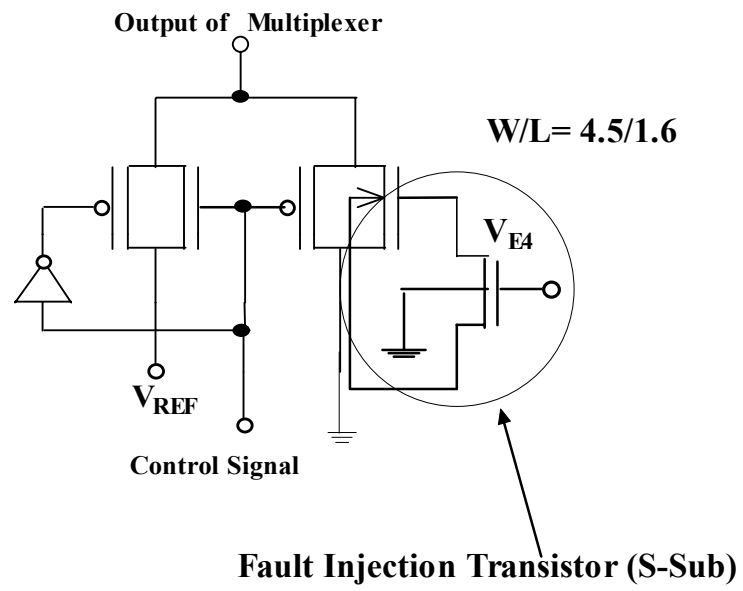


Figure 3.19: CMOS MUX circuit with defect 4 introduced using a FIT.

## Chapter 4

### Theoretical and Experimental Results

This Chapter discusses theoretical results obtained from post-layout PSPICE (MicroSim Pspice A/D Simulator, V.8) simulations on  $I_{DDQ}$  testing of a 10-bit charge scaling DAC. SPICE level 3 MOS model parameters were used in simulation [42], which are summarized in Appendix A. The chip was designed using L-EDIT, V.8.03 in standard  $1.5\mu\text{m}$  n-well CMOS technology. The chip occupies an area of  $692\mu\text{m} \times 516\mu\text{m}$  and includes  $240\mu\text{m} \times 40\mu\text{m}$  area of BICS. DAC design was put in  $2.25\text{mm} \times 2.25\text{mm}$  size, 40-pin pad frame for fabrication and testing. In the following sections, theoretical results (simulated from PSPICE) and experimentally measured values will be presented and discussed. HP 1660CS logic analyzer was used for testing the packaged device described in Appendix B.

#### 4.1 Simulation Results

Figure 4.1 shows the layout of a 10-bit charge scaling digital-to-analog converter with four fault injection transistors distributed across the chip. FIT-1 is injected in the operational amplifier part of the chip. FIT-2 is injected in S/H circuit of the chip. FIT-3 and FIT-4 are injected in the multiplexer parts of the chip. Figure 4.2 shows the chip layout of 10-bit charge scaling DAC including BICS within a pad frame of  $2.25\text{mm} \times 2.25\text{mm}$  size. . The area of the DAC alone is  $692 \times 502\mu\text{m}^2$ . The entire area of the CUT along with BICS is  $692 \times 516\mu\text{m}^2$ . Therefore the BICS occupies only  $242 \times 40\mu\text{m}^2$  of the entire chip area. Figure 4.3 shows the microchip photograph of 10-bit charge scaling

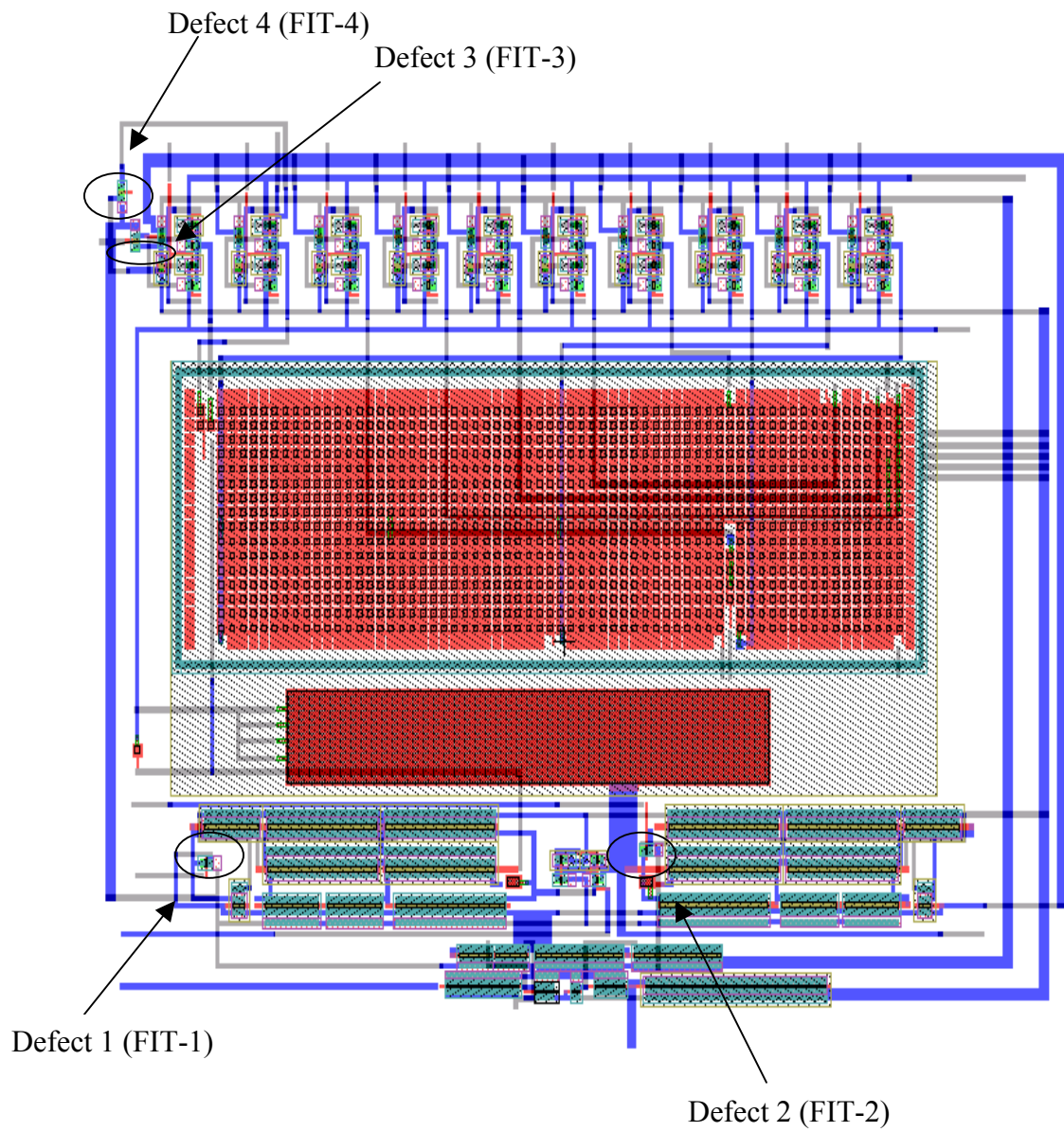


Figure 4.1: CMOS chip layout of a 10-bit charge scaling DAC with four fault injection transistors distributed across the chip.

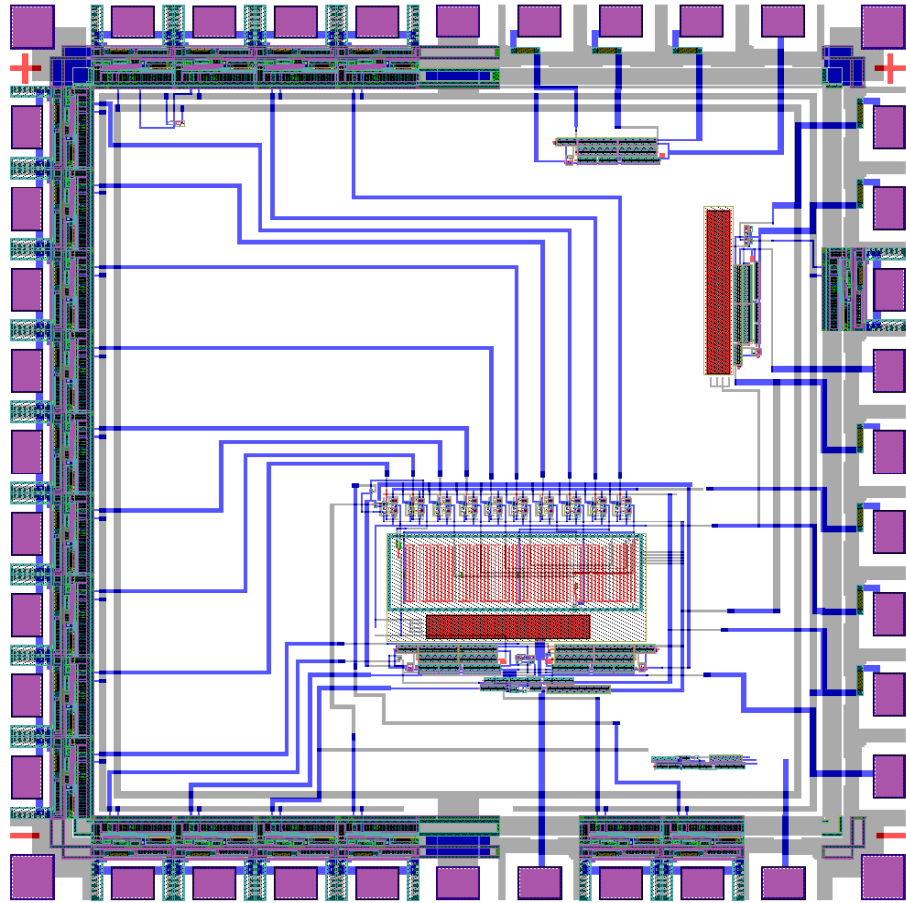


Figure 4.2: CMOS chip layout of a 10-bit charge scaling DAC including BICS within a padframe of  $2.25\text{mm} \times 2.25\text{mm}$  size.

DAC and BICS for  $I_{DDQ}$  testing. Figure 4.4 shows the simulated and measured characteristics of the 10-bit charge scaling DAC when the faults are not activated. The equivalent analog output voltage is shown for all the 1024 input combinations. Figure 4.5 shows the measured DNL characteristics of the 10-bit charge scaling DAC when the faults are not activated. DNL is within  $\pm 0.6$  LSB. Figure 4.6 shows the measured INL characteristics of the 10-bit charge scaling DAC when the faults are not activated. INL is less than 1 LSB.

Figure 4.7 shows the simulated output of the opamp when the fault ( $V_{EI}$ ) is activated (Fig 3.16). When the opamp is given a sine wave of 1mV p-p, the output obtained is a sine wave of 105mV p-p with a gain of 105. Offset voltage is increased to 1.9V from 33 $\mu$ V without faults. Figure 4.8 shows the transfer function with the fault activated with significant non-linearity introduced in the narrow transition region. Figure 4.9 shows the gain versus frequency response of opamp with fault activated. The amplifier 3dB gain with the fault activated is 38dB as compared to 77dB when the fault is deactivated. The bandwidth is increased to 3 MHz from 100 KHz without fault (Fig 2.16).

Figure 4.10 shows the simulated output response of the multiplexer circuit when FIT-3 is deactivated (Fig. 3.18). When the  $V_{CONTROL}$  goes HIGH the multiplexer chooses the  $V_{REF}$  and when  $V_{CONTROL}$  goes LOW, the multiplexer chooses GND input. The output waveform obtained is a pulse of 2.5V p-p. Figure 4.11 shows the simulated output response of the multiplexer circuit when FIT-3 is activated (Fig 3.18). The output waveform obtained is 1.7V p-p. Figure 4.12 shows the simulated BICS output when the

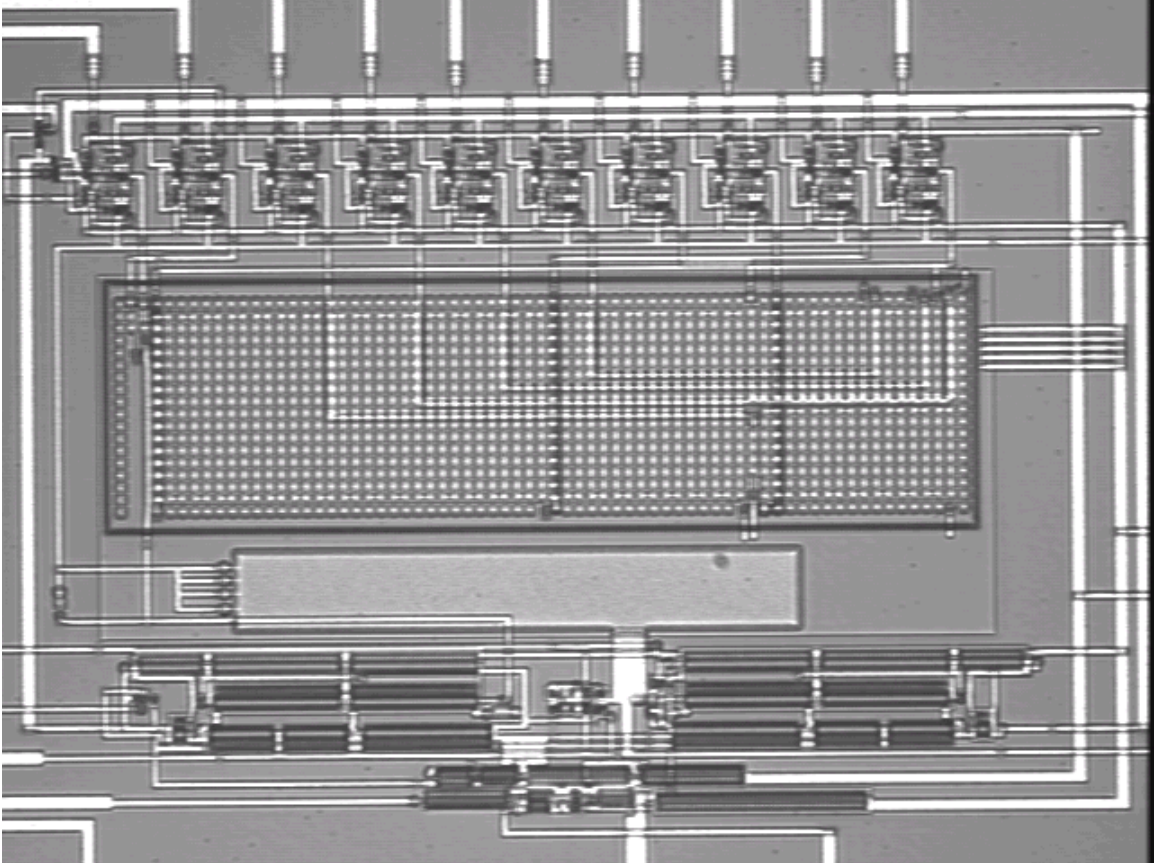


Figure 4.3: Microchip photograph of 10-bit charge scaling DAC and BICS for  $I_{DDQ}$  testing.



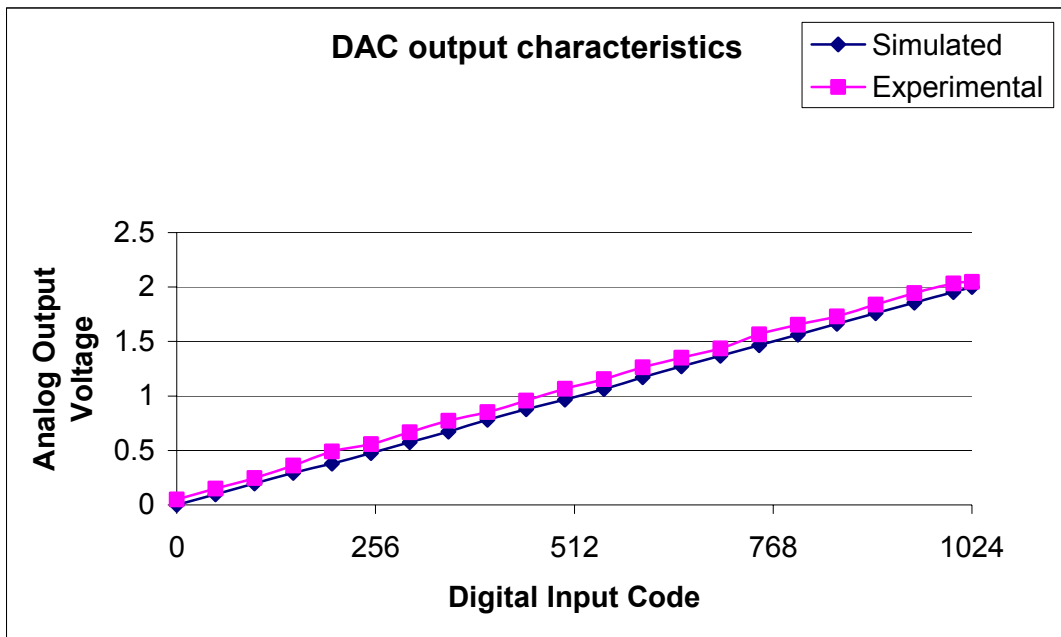


Figure 4.4: simulated and measured characteristics of a 10-bit charge scaling DAC.  
Note: Faults are not activated.

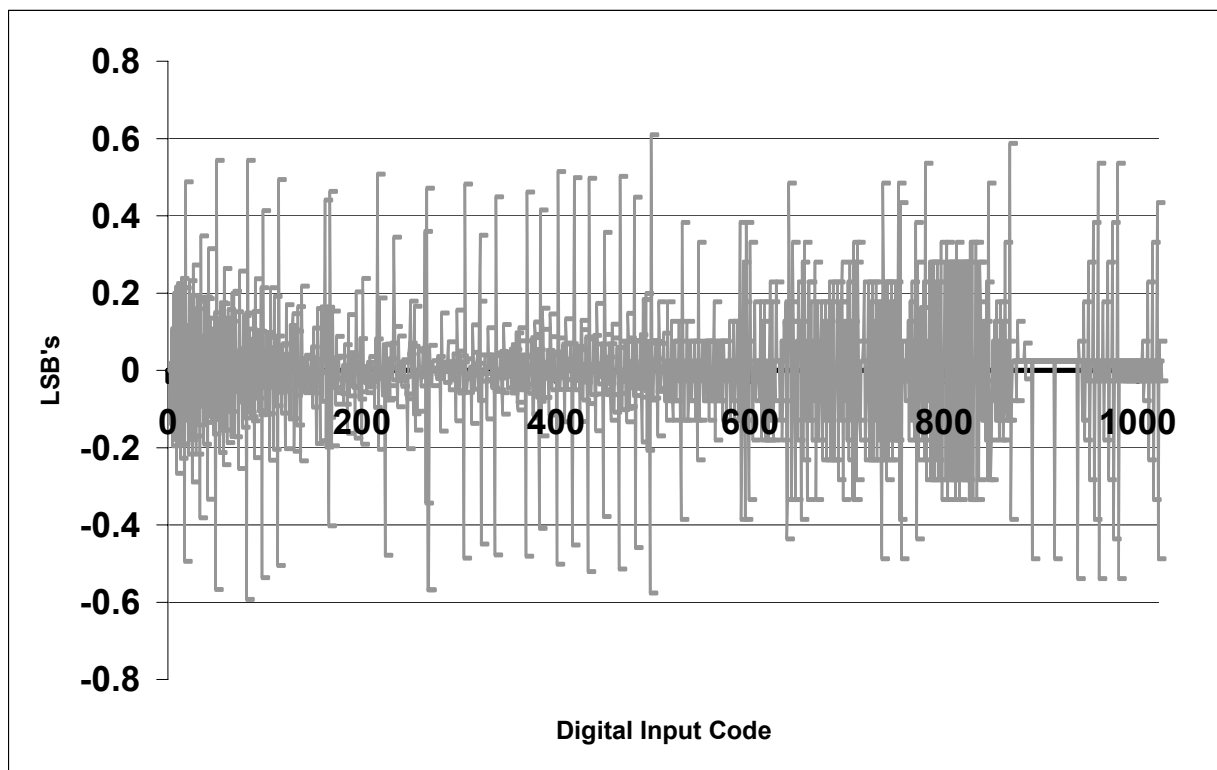


Figure 4.5: Measured DNL characteristics of a 10-bit charge scaling DAC.  
Note: Faults are not activated.

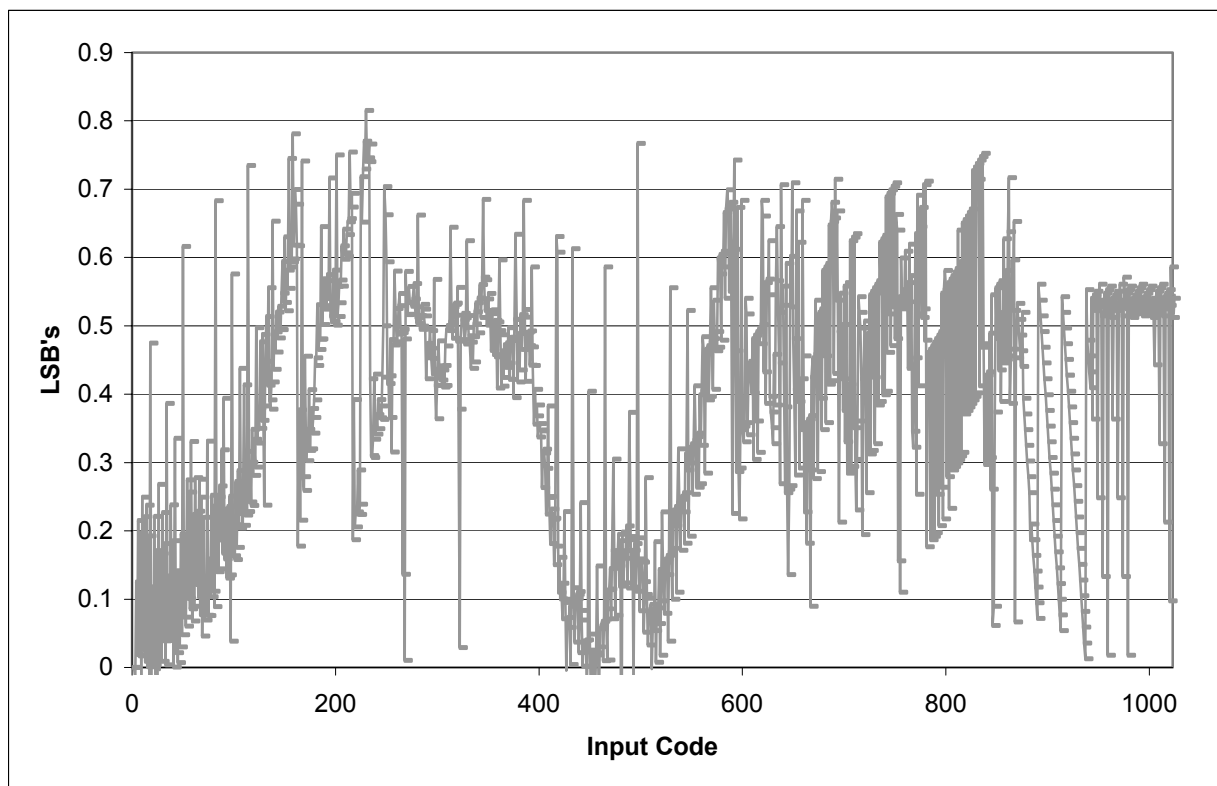


Figure.4.6: Measured INL characteristics of a 10-bit Charge Scaling DAC.  
Note: Faults are not activated.

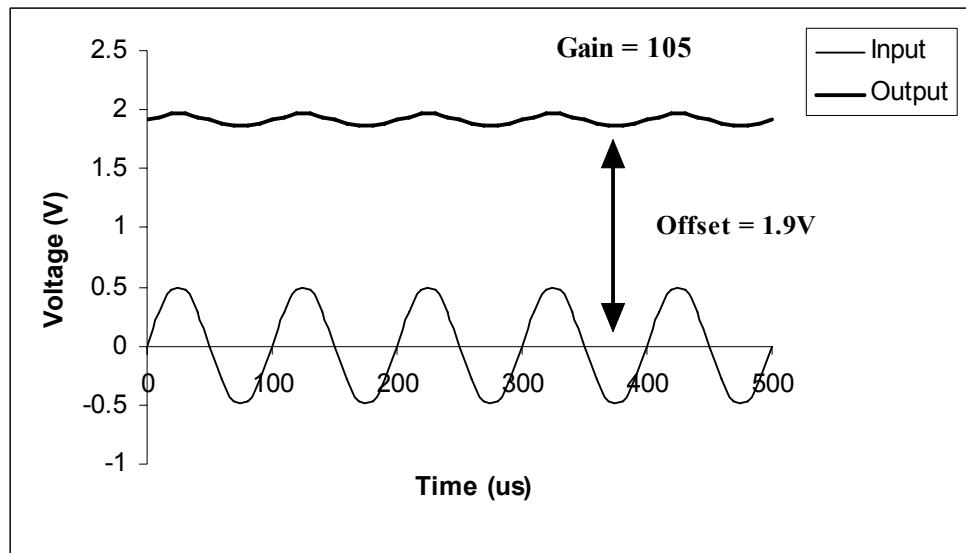


Figure: 4.7 Voltage gain response of op-amp with fault introduced.  
Note: Input is applied at the non-inverting input.

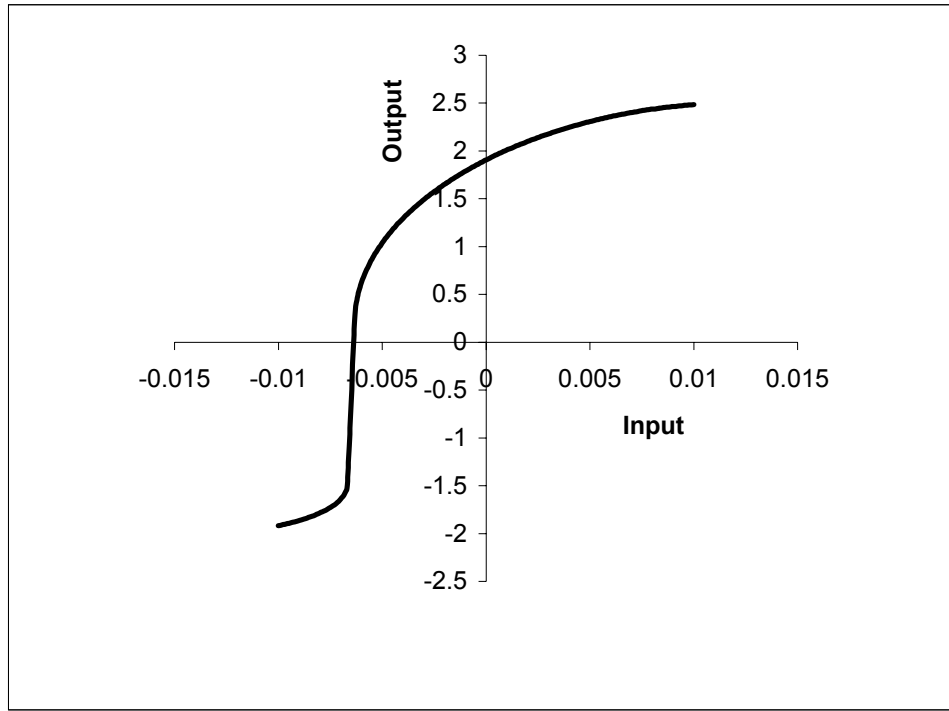


Figure 4.8: Transfer function of op-amp with fault ( $V_{EI}$ ) induced.

Gain = 41dB  
3dB Gain = 41dB - 3dB = 38dB

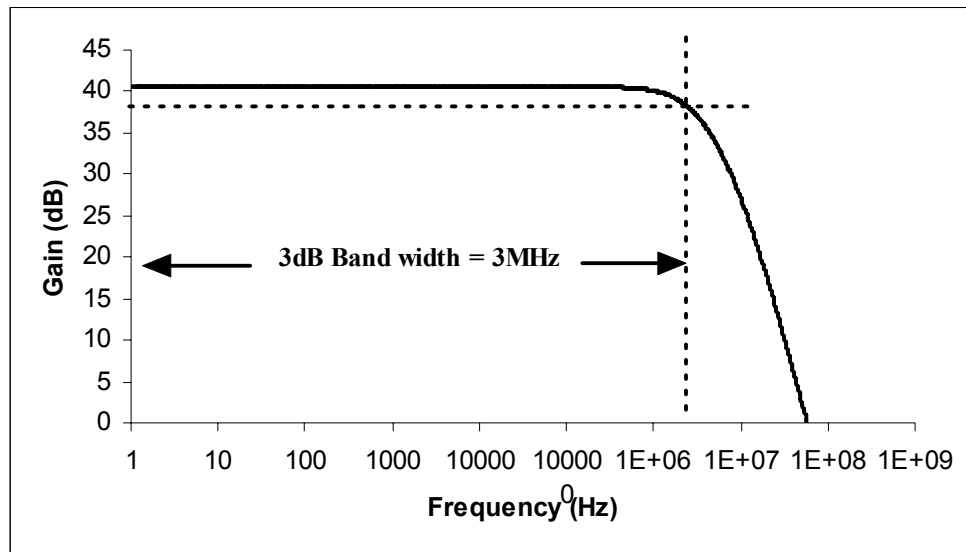


Figure 4.9: Gain versus frequency response of the CMOS opamp circuit with fault introduced.

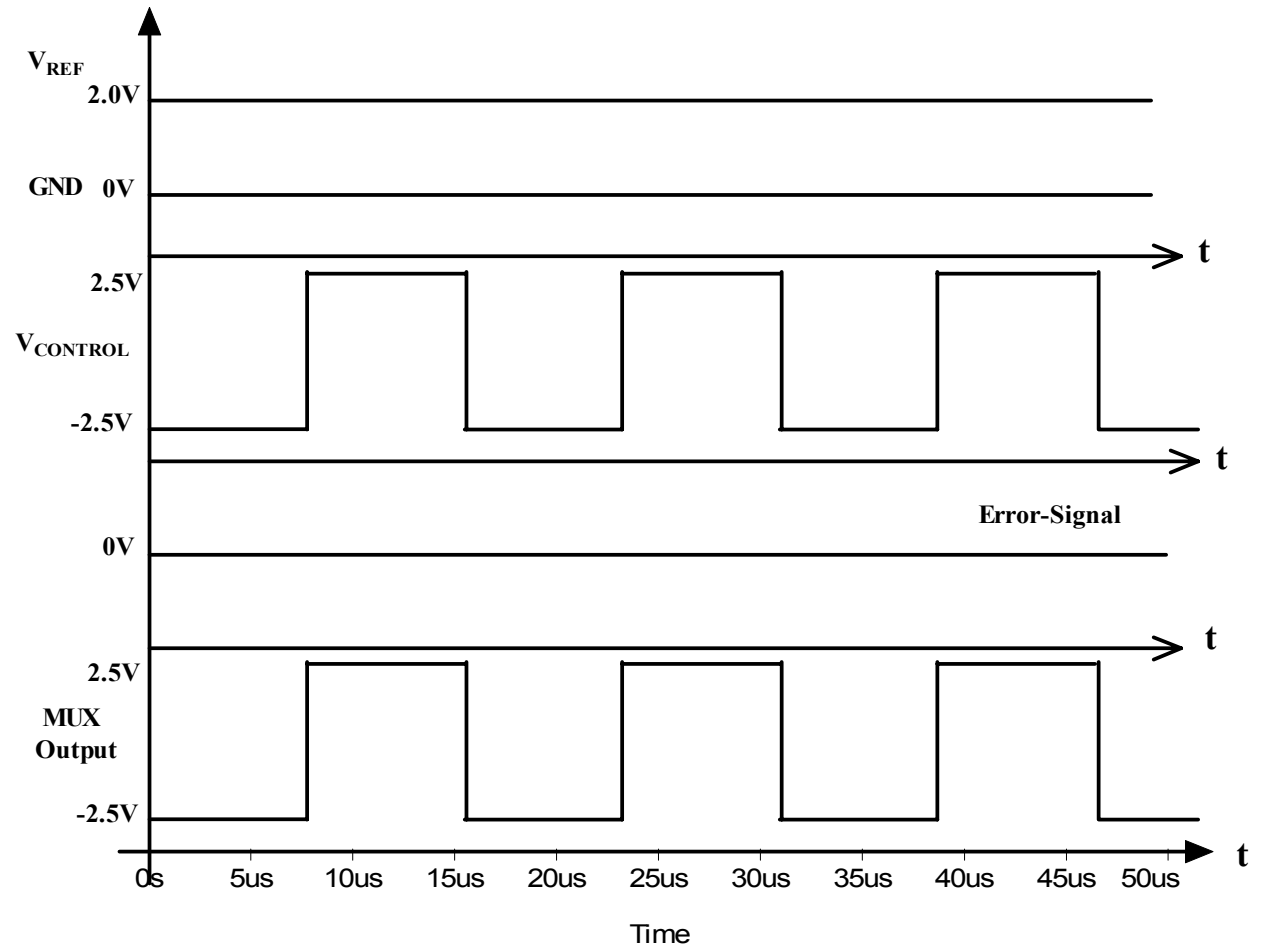


Figure 4.10: Simulated output response of the multiplexer circuit of Fig 3.18 without defect.

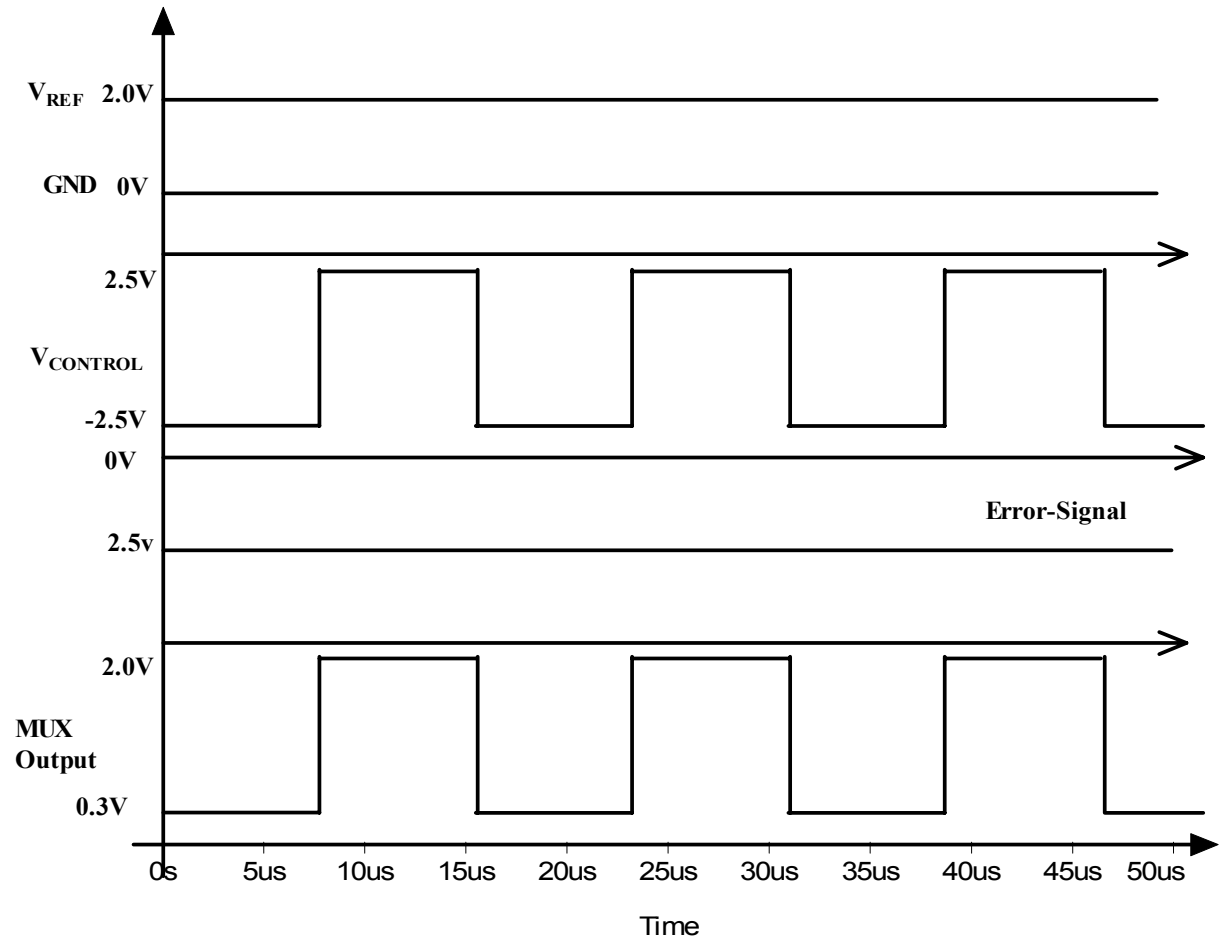


Figure 4.11: Simulated output response of the multiplexer circuit of Fig. 3.18 with fault activated.



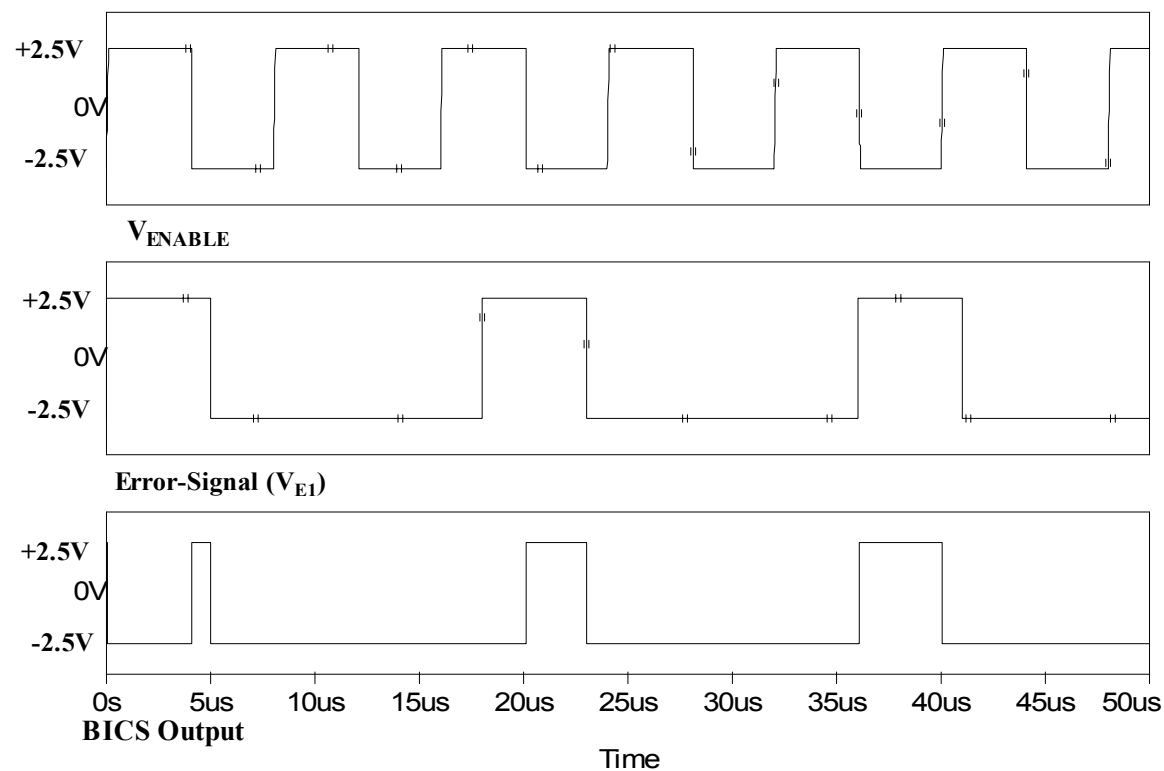


Figure 4.12: Simulated BICS output of the circuit of Fig. 3.16 when Error-signal-1 for defect-1 is activated.

FIT-1 is activated. FIT-1 is a defect injected between the source and drain of the operational amplifier circuit (Fig.3.16) of the chip (Fig 4.2). In Fig. 4.12, when the  $V_{ENABLE}$  signal is 'high', the BICS is by-passed and the defect is not detected. When the  $V_{ENABLE}$  signal is 'low', the BICS is enabled and if the Error-signal is 'high', the BICS detects the faults and the output of the BICS is 'high'. Figure 4.13 shows the simulated BICS output when the FIT-2 is activated (Fig.3.17). FIT-2 is a defect injected between the gate and drain of the unity gain buffer in the S/H circuit (Fig. 3.17) of the chip (Fig. 4.2). In Fig. 4.13, when the  $V_{ENABLE}$  signal is 'high' the BICS is by-passed and the defect is not detected. When the  $V_{ENABLE}$  signal is 'low' the BICS is enabled and if the Error-signal is 'high' the BICS detects the faults and the output of the BICS is 'high'. Figure 4.14 shows the simulated BICS output when the FIT-3 is activated. FIT-3 is a defect injected between the gate and source of the multiplexer circuit of Fig. 3.18 of the chip (Fig. 4.2). In Fig. 4.14 when the  $V_{ENABLE}$  signal is 'high', the BICS is by-passed and the defect is not detected. When the  $V_{ENABLE}$  signal is 'low', the BICS is enabled and if the Error-signal is 'high', the BICS detects the faults and the output of the BICS is 'high'. Figure 4.15 shows the simulated BICS output when the FIT-4 is activated. FIT-4 is a gate oxide short injected between the gate and substrate of the multiplexer circuit of Fig 3.19 of the chip (Fig 4.2). When the  $V_{ENABLE}$  signal is 'high', the BICS is by-passed and the defect is not detected. When the  $V_{ENABLE}$  signal is 'low', the BICS is enabled and if the Error-signal is 'high' the BICS detects the faults and the output of the BICS is 'high'.

Figure. 4.16 shows the CMOS circuit diagram of a 10-bit charge scaling DAC with four fault injection transistors. Figure 4.17 shows the simulated output of the

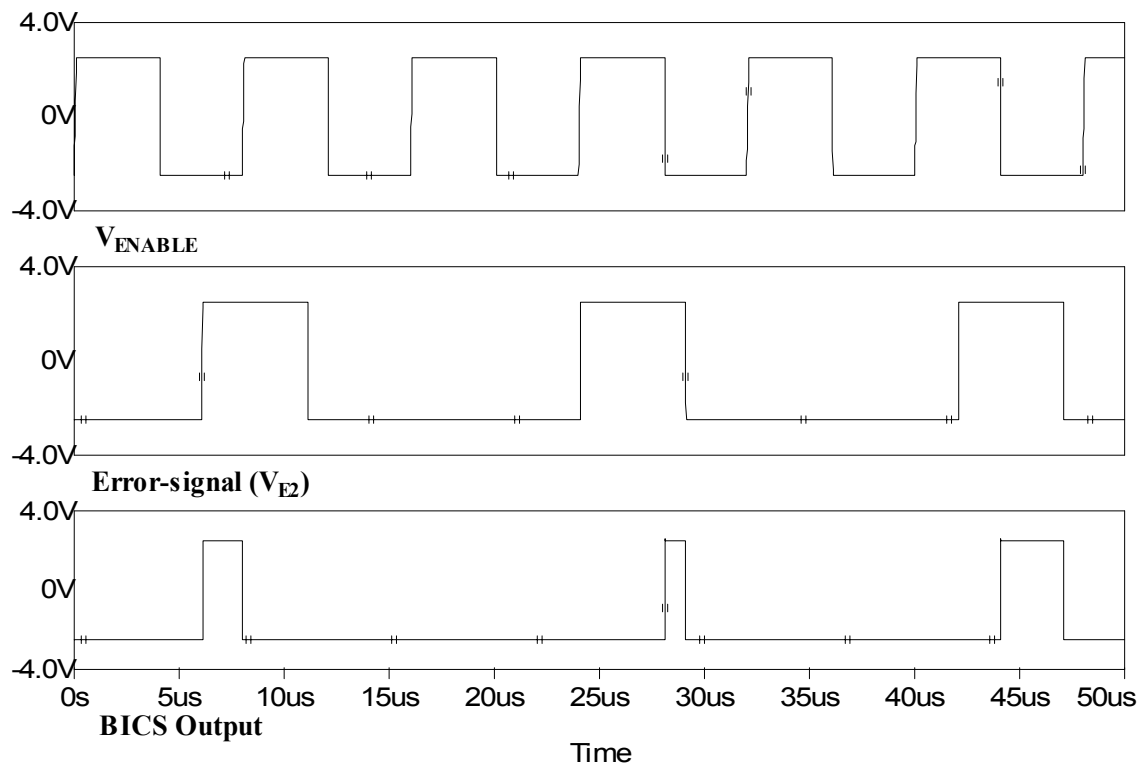


Figure 4.13: Simulated BICS output of the circuit of Fig. 3.17 when Error-signal-2 for defect-2 is activated.

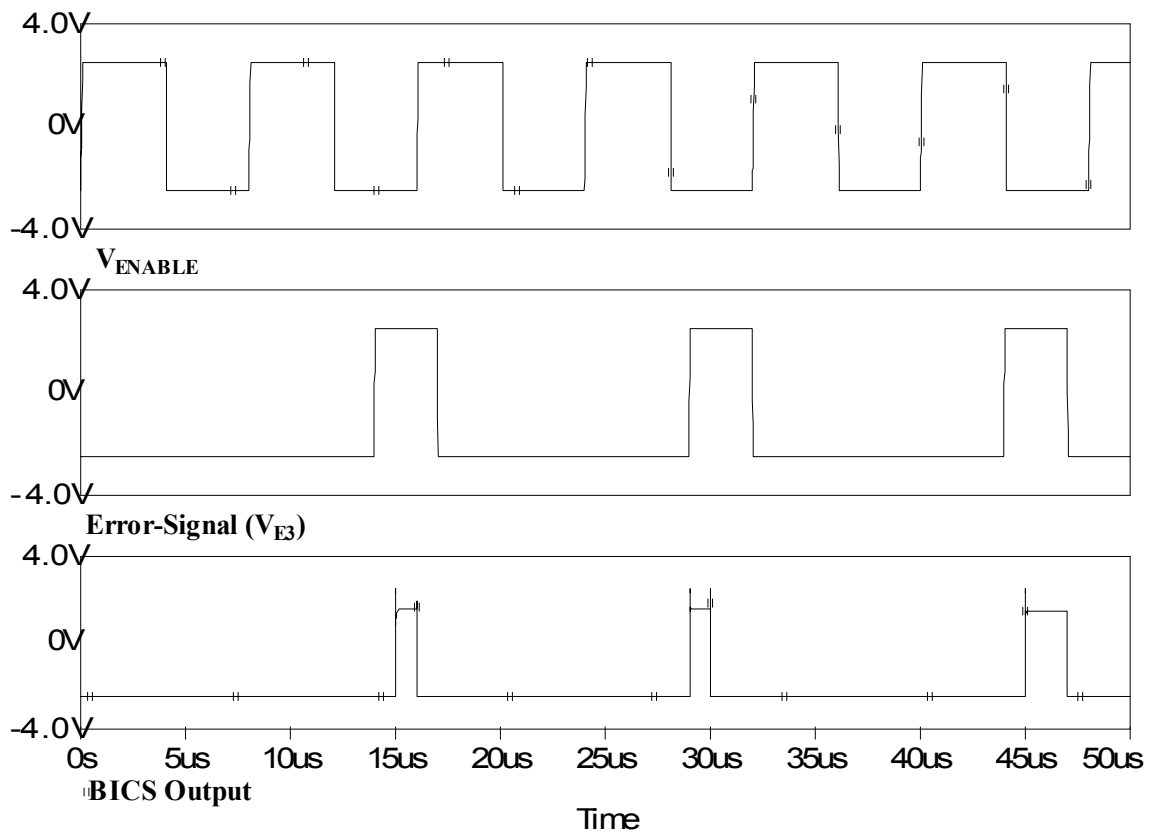


Figure 4.14: Simulated BICS output of the circuit of Fig. 3.18 when Error-signal-3 for defect-3 is activated.

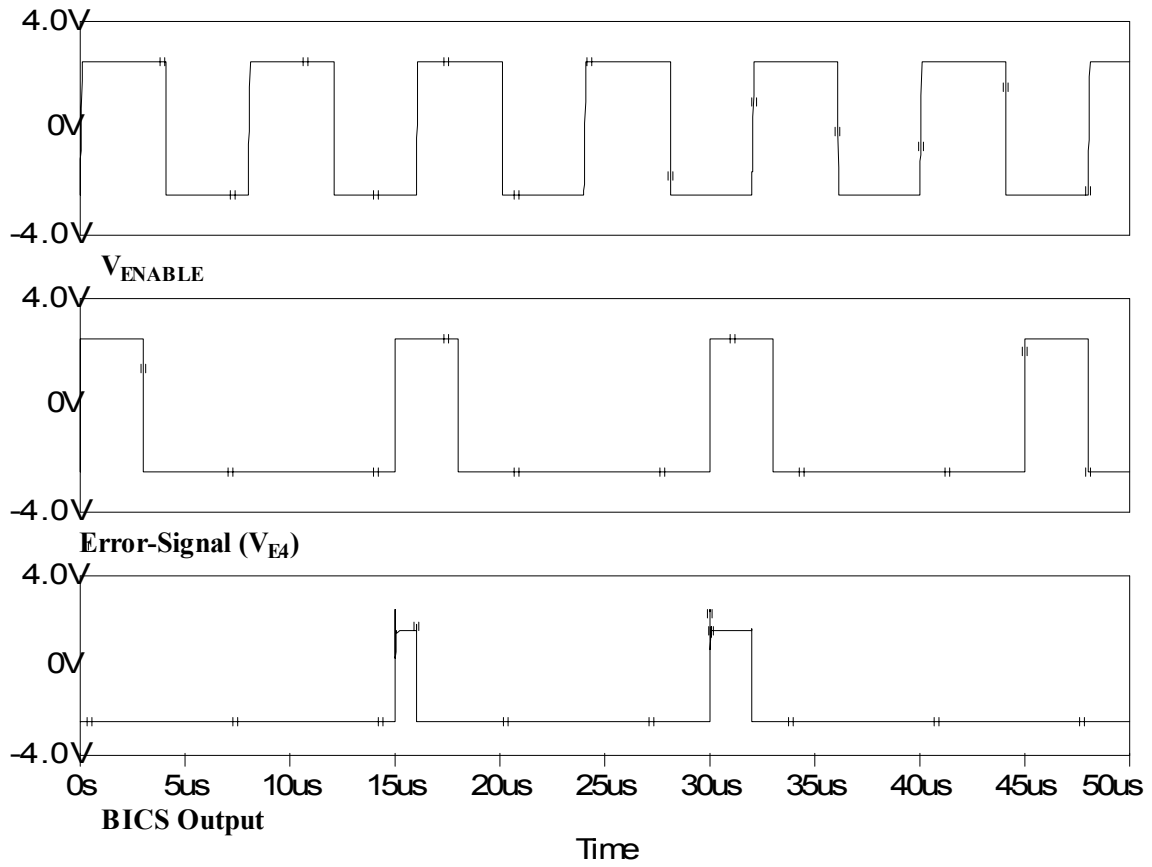


Figure 4.15: Simulated BICS output of the circuit of Fig.3.19 when Error-signal-4 for defect-4 is activated.

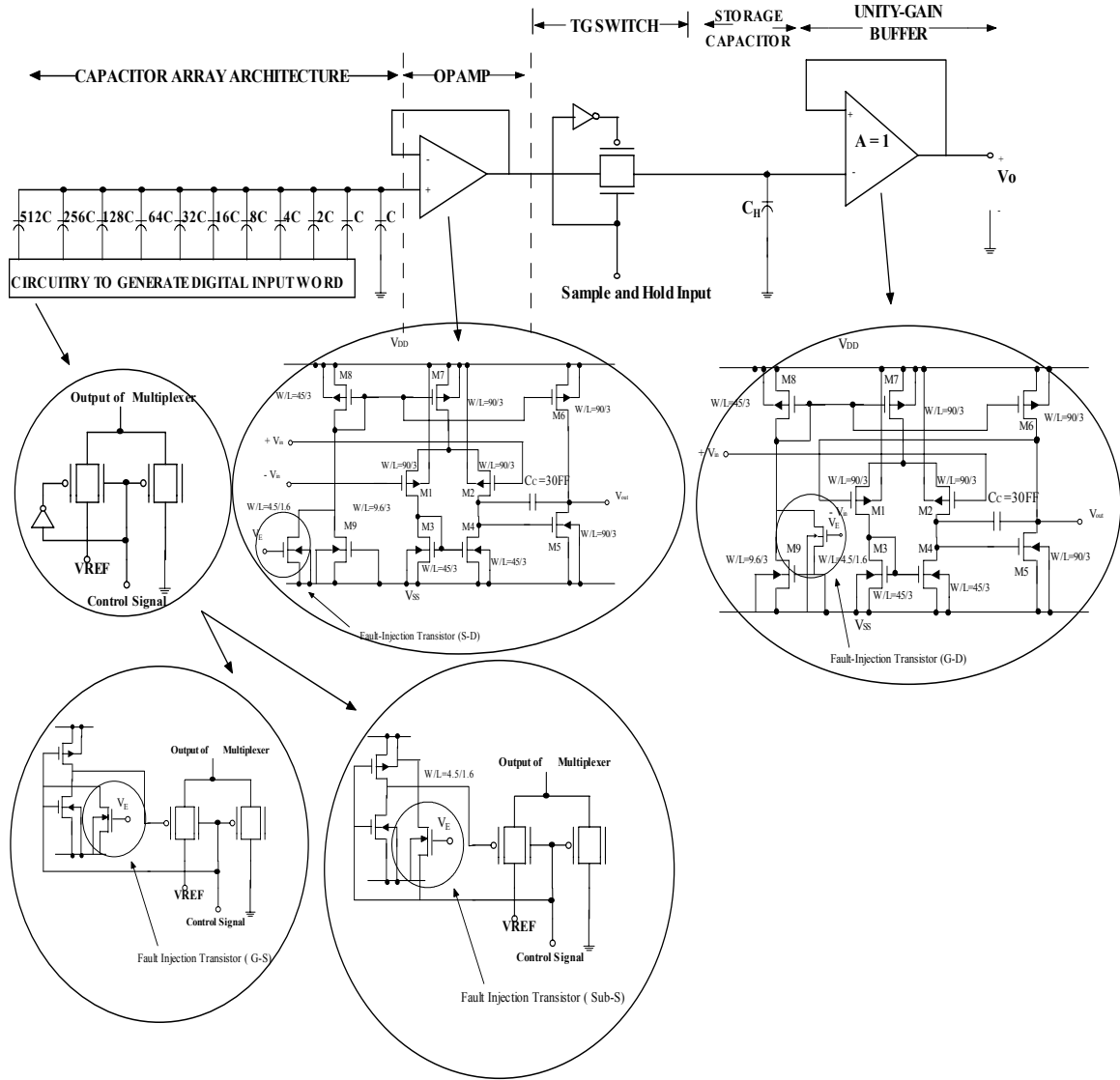


Figure 4.16: CMOS circuit diagram of 10-bit charge scaling DAC with four fault injection transistors distributed across different parts of the circuit.

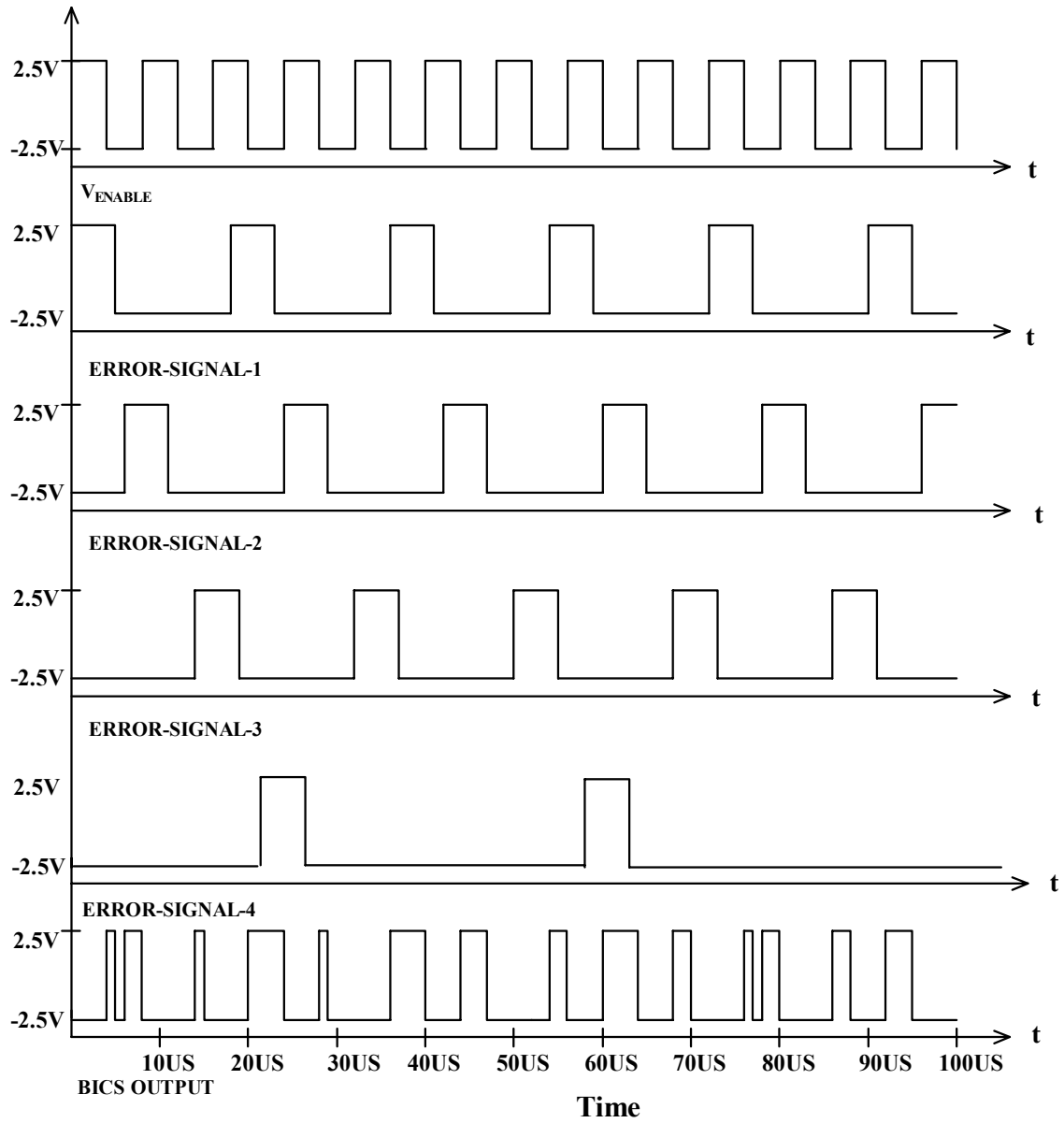


Figure 4.17: Simulated BICS output with defects induced using fault injection transistors.

BICS when four FIT's are activated. In Fig. 4.17, when the  $V_{ENABLE}$  is 'high' the BICS is disabled and when it is low the BICS is enabled. When the BICS is enabled and if there is any Error-Signal going 'high' the BICS detects the fault. Table-1 shows the faulty  $I_{DDQ}$  values obtained for the different kinds of faults are injected in the chip. Figure 4.18 shows the wave forms obtained from the logic Analyzer. The error signal is kept 'high' and the BICS is tested for its operation in the normal mode and test mode. When the  $V_{ENABLE}$  is 'low', the BICS is in the test mode and if the error signal is 'high', PASS/FAIL gives logic '1' and thus, it detects the fault induced. When the  $V_{ENABLE}$  is 'low', the BICS is in the normal mode, PASS/FAIL gives logic '0' thus, no fault is detected.

Table 4.1 summarizes calculated (simulated) and measured  $I_{DDQ}$  values corresponding to four different faults distributed across the chip. The reference current, is  $I_{REF}$  is 1mA. Table 4.1 shows that in the presence of faults  $I_{DDQ}$  reaches to 3mA. The calculated and measured  $I_{DDQ}$  values are in close agreement. Table 4.2 summarizes a comparative study of design of previously reported BICS with the present BICS design. Our BICS design uses only seven transistors and an inverter buffer. The BICS requires neither an external voltage source nor a current source. Further more, the BICS does not require clocks.



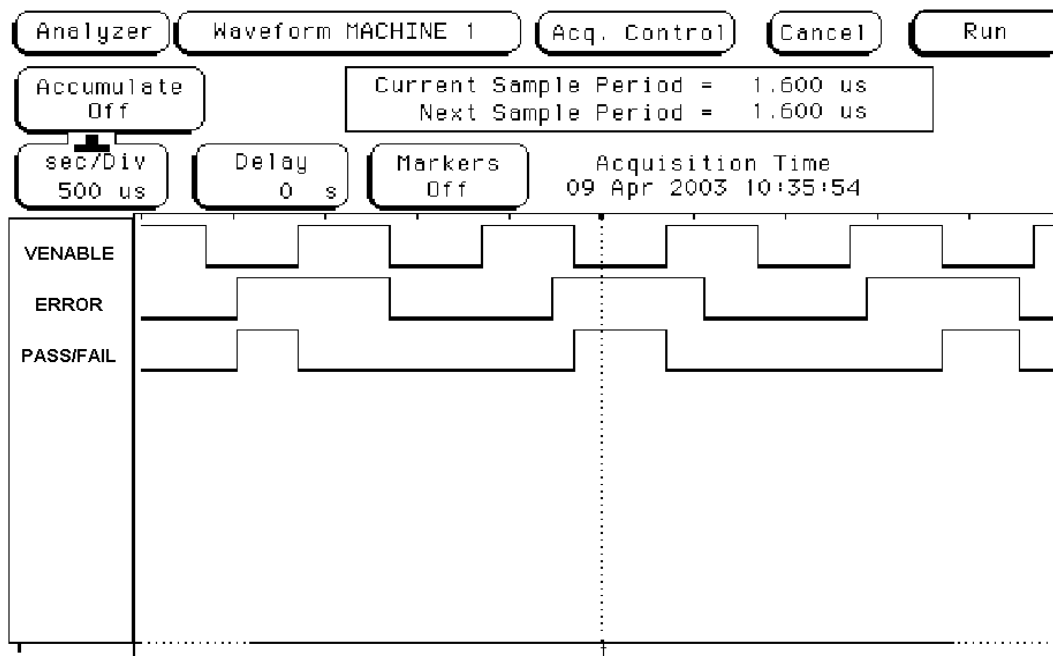


Figure 4.18: HP 1660CS logic analyzer test results on a fabricated CMOS 10-bit charge scaling DAC showing the performance of BICS in normal and test modes.

Table 4.1 Theoretical and measured  $I_{DDQ}$  for different fault types  
 Note: The reference current,  $I_{REF} = 1\text{mA}$

Defect	Faulty $I_{DDQ}$ (Sim) mA	Faulty $I_{DDQ}$ (Meas) mA
Source-Drain short	3.00 mA	2.8 mA
Gate-Drain short	2.8 mA	2.7 mA
Gate-Source short	2.7 mA	2.6 mA
Gate-oxide short	2.5 mA	2.2 mA

Table 4.2: Comparison of built-in-current sensors

	# Device	Clock Signal	Mode Select	Control Pin	Output Pin
Maly's Design[13]	TR: 10 Inv: 2 Nand: 1	Single Clock	Y	5	1
Miura's Design[15]	TR: 16 R: 1 C: 1	Not Used	Not Reported	3	1
Shen' Design[16]	TR: 13 Diode: 1	Two Phase Clock	N	3	2
Tang's Design[38]	TR: 24 R: 1	Single Clock	N	3	1
Favalli's Design[14]	TR: 2* $\text{gates}+1$	Not Used	Y	1	1
Nigh's Design[17]	TR: 13 Inv: 1	Two Phase Clock	Y	3	1
Proposed Design	TR: 7 Inv: 1	Not Used	Y	2	1

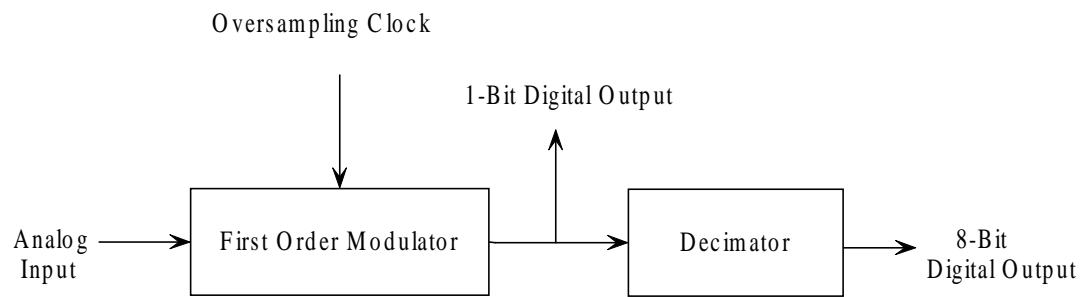
Note: Mode Select: Normal Mode / Test Mode, Control Pins:  $V_{\text{ENABLE}}$  and EXT.

## Chapter 5

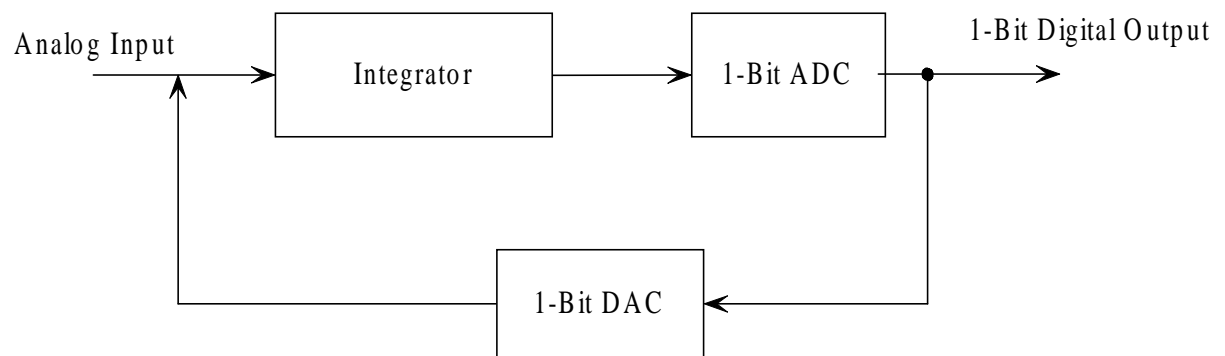
### Conclusion and Scope of Future Work

A 10-bit DAC using charge-scaling architecture is designed in standard 1.5  $\mu\text{m}$  n-well CMOS technology. The DAC is tested with all 1024 digital input word combinations. The unit step is about 1.9mV. DAC operates with  $\pm 2.5\text{V}$  supply voltages. The reference voltage used is 2V for a 'HIGH' and ground (0V) for a 'LOW'. The 10-bit DAC is used as a circuit under test (CUT). The CUT is tested with a novel built-in current sensor (BICS), which has a very negligible impact on the performance of the circuit under test.

The present BICS works in two-modes: normal mode and the test mode. In the normal mode, BICS is isolated from the CUT due to which there is no performance degradation of the circuit under test. In the testing mode, BICS detects the abnormal current caused by permanent manufacturing defects. The BICS requires neither an external voltage source nor a current source. The present BICS is designed with only seven transistors and an inverter buffer. The present BICS design which is based on current comparison, combined with the novel fault-injection technique, can be used for  $I_{DDQ}$  testing of other type of data converters of the type shown in Fig. 5.1 and is suggested for future work. The built-in current sensor of the present work requires less area and is more efficient than the conventional current sensors. It is shown that with the use of a novel fault injection technique, combined with a built-in current sensor design, has significantly improved the testing of mixed signal integrated circuits



(a)



(b)

Figure 5.1: Block diagram of a sigma-delta ADC

## Bibliography

- [1] R. Rajsuman, *I<sub>ddq</sub> Testing for CMOS VLSI*, Artech House, 1995.
- [2] C.Y. Chao, H. J. Lin and L. Milor, "Optimal testing of VLSI analog circuits," *IEEE. Tran. on Computer-Aided Design of Integrated Circuits and Systems*, vol.16, Jan. 1997. pp. 58-77.
- [3] C.Y. Pan and K.T. Cheng, "Pseudorandom testing for mixed-signal circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol 16, Oct.1997. pp. 1173-1185.
- [4] K. Arabi and B. Kaminska, "Design for testability of embedded integrated operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 33, April.1998. pp. 573-581.
- [5] K. Arabi and B. Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE. Trans. on Computer-Aided Design of Integrated Circuits and Systems*, July 1997, pp. 745-753.
- [6] B. Dufort and G. W Roberts, "On-chip analog signal generation for mixed-signal built in self-test," *IEEE J. Solid-State Circuits*, vol. 34, March 1999. pp. 318-330.
- [7] K. Arabi, B. Kaminska and J. Rzeszut, "A new built-in-self-test approach for digital-to-analog and analog-to-digital converters," *Proc. 12<sup>th</sup> Int. Conf. on Computer-Aided-Design*, Nov. 1994. pp. 491-494.
- [8] B.D. Brown. R.D. McLeod, "Built-in current mode circuits for I<sub>ddq</sub> monitoring," *Proc. 1993 IEEE Custom Integrated Circuit Conference*, 1993, pp. 30.6.1-4.
- [9] C.W. Hsue and C. J. Lin, "Built-in current sensor for I<sub>ddq</sub> test in CMOS," *Proc. Int. Test Conf.*, 1993, pp. 635-641.
- [10] S. Siskos, Th. Laopoulos, A. A. Hatzopoulos and M. Bafleur, "A current conveyor based BIC sensor for current monitoring in mixed-signal circuits," *Proc. ICECS*, 1996, pp. 1210-1212.
- [11] J.B. Kim, S. J. Hong, and J. Kim, "Design of built-in current sensor for I<sub>DDQ</sub> testing," *IEEE J. Solid-State Circuits*, vol. 33, Aug. 1998, pp. 1266-1272.
- [12] T.Y. Chang, C. C. Wang, and J. B. Hsu, "Two schemes for detecting CMOS analog faults," *IEEE J. Solid-State Circuits*, vol. 27, Feb. 1992. pp. 229-233.

- [13] W. Maly and M. Patyra, "Built-in current testing," *IEEE J. Solid-State Circuits*, vol. 27, May. 1992, pp. 425-428.
- [14] M. Favalli, P. Olivo, M. Damiani, and B. Ricco, "Novel design for testability schemes for CMOS IC's," *IEEE J. Solid-State Circuits*, vol. 25, Oct. 1990, pp. 1239-1246.
- [15] Y. Miura and K. Kinoshita, "Circuit design for built-in current testing," *Proc. Int. Test. Conf.*, Nov. 1992, pp. 873-881.
- [16] T.L. Shen, J. C. Daly, and J. C. Lo, "A 2-ns detecting time, 2- $\mu$ m CMOS built-in current sensing circuit," *IEEE J. Solid-State Circuits*, vol. 28, Jan. 1993. pp. 72-77.
- [17] P. Nigh and W. Maly, "A self-testing ALU using built-in current sensing," *Proc. 1989 IEEE Custom Integrated Circuit Conference*, 1989, pp. 22.1.1-22.1.4.
- [18] W. Maly and P. Nigh, "Built-in current testing-feasibility study," in *Proc. Int. Conf. Computer. -Aided Design*, Nov.1988, pp. 340-343.
- [19] A. Srivastava and S. Aluri, "A Novel Approach to  $I_{DDQ}$  testing of mixed-signal integrated circuits," *Proc. of 45<sup>th</sup> IEEE Int. Midwest Symposium on Circuits and Systems*, 2002, pp. II 270-273.
- [20] S.D. McEuen "I<sub>DDQ</sub> benefits", *Proc. of 1991 IEEE VLSI Test Symposium*, paper 14.1, 1991, pp. 285-290.
- [21] J. Argüelles, M. Martínez and S. Bracho, "Dynamic  $I_{DD}$  test circuit for mixed signal ICs," *Electronic Letters*, vol. 30, no. 6, 17<sup>th</sup> March 1994, pp. 485-486.
- [22] K. Arabi and B. Kaminska, "Design and realization of an accurate built-in current sensor for on-line power dissipation measurement and  $I_{DDQ}$  testing," *Proceedings International Test Conference*, 1997, pp. 578-586.
- [23] Y. Maidon, Y. Deval, P. Fouillat, J. Tomas, J. P. Dom; "On-chip  $I_{DDX}$  Sensor", *Proc. of IEEE  $I_{DDQ}$  Workshop*, 1996, pp. 64-67.
- [24] J. Segura, I.D. Paul, M. Roca, E. Isern, C.J. Hawkins, "Experimental analysis of transient current testing based on charge observation," *Electronics Letters*, vol. 35, no. 6, 18<sup>th</sup> March 1999, pp. 441-447.
- [25] I. Pecuh. M. Margala and V. Stopjakova, "1.5 Volts Iddq/Iddt current monitor," *Proc. of the 1999 IEEE Canadian Conference on Electrical and Computer Engineering*, May 9-12, 1999, pp. 472-476.

- [26] V. Stopjaková, H. Manhaeve and M. Sidiropulos, "On-chip transient current monitor for testing of low-voltage CMOS IC," *Proc. Design, Automation and Test conference and exhibition in Europe*, March 1999, pp. 538-542.
- [27] R.J. Baker, H.W. Li, D.E. Boyce, *CMOS Circuit Design Layout and Simulation*, IEEE Press 1998.
- [28] R.L. Geiger, P.E. Allen, N.R. Strader *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill, 1990.
- [29] P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, Second Edition, Oxford University Press, 2002.
- [30] R.T. Howe and C.G. Sodini *Microelectronics: A Integrated Approach*, Prentice Hall, NJ, 1997.
- [31] Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Technology*, McGraw-Hill, 1996.
- [32] J.P. UYEMURA, *Fundamentals of MOS Digital Integrated Circuits*, Addison-Wesley, 1988.
- [33] J.M. Soden, C.F. Hawkins, R.K. Gulati and W. Mao "IDDQ testing: a review," *Journal of Electronic Testing: Theory And Applications*, vol.3, 1992, pp. 291-303.
- [34] P. Nigh, W. Maly, "Test generation for current testing," *IEEE Design and Test of Computers*, Feb. 1990, pp. 26-38.
- [35] S.D. McEuen, "Reliability benefits of IDDQ," *J. of Electronic Testing: Theory and Application*, Vol.3, 1992, pp-904-910.
- [36] A. Rubio, J. Figueras and J. Segura, "Quiescent current sensor circuits in digital VLSI CMOS testing," *Electronics Letters*, vol. 26, No.15, 19<sup>th</sup> July 1990, pp. 1204-1205.
- [37] J.A. Segura, V.H. Champac, R.R. Montanes, J. Figueras and J.A. Rubio, "Quiescent current analysis and experimentation of defective CMOS circuits," *J. of Electronic Testing: Theory and Applications*, Vol.3, 1992, pp. 337-346.
- [38] K.J. Lee and J.J. Tang, "A built-in current sensor based on current-mode design," *IEEE Transactions on Circuits and Systems-II Analog and Digital Signal Processing*, Vol. 45, No. 1, Jan.1998, pp. 133-137.
- [39] J. Rius and J. Figueras, "Proportional BIC sensor for current testing," *J. Electronic Testing: Theory and Applications*, Vol.3, 1992, pp. 387-396.



- [40] T.L. Shen, J. C. Daly, and J. C. Lo, "On Chip current sensing circuit for CMOS VLSI," *Proc. IEEE VLSI Test Symposium*, paper 16.2, 1992, pp. 309-314.
- [41] C. Hwang, M. Ismail, J.E. DeGroat, "On chip  $I_{DDQ}$  testability schemes for detecting multiple faults in CMOS IC's," *IEEE J. of Solid State Circuits*, vol. 31, No.5, May 1996, pp. 732-739.
- [42] [www.mosis.edu](http://www.mosis.edu).

## Appendix A

### SPICE LEVEL 3 MOS MODEL Parameters for standard n-well CMOS Technology [42]

#### (A) Model Parameters for n-MOS transistors.

```
. MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+TPG=1 VTO=0.687 DELTA=0.0000E+00 LD=1.0250E-07 KP=7.5564E-05
+UO=671.8 THETA=9.0430E-02 RSH=2.5430E+01 GAMMA=0.7822
+NSUB=2.3320E+16 NFS=5.9080E+11 VMAX=2.0730E+05 ETA=1.1260E-01
+KAPPA=3.1050E-01 CGDO=1.7294E-10 CGSO=1.7294E-10
+CGBO=5.1118E-10 CJ=2.8188E-04 MJ=5.2633E-01 CJSW=1.4770E-10
+MJSW=1.00000E-01 PB=9.9000E-01
```

#### (B) Model Parameters for p-MOS transistors.

```
. MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+TPG=-1 VTO=-0.7574 DELTA=2.9770E+00 LD=1.0540E-08 KP=2.1562E-05
+UO=191.7 THETA=1.2020E-01 RSH=3.5220E+00 GAMMA=0.4099
+NSUB=6.4040E+15 NFS=5.9090E+11 VMAX=1.6200E+05 ETA=1.4820E-01
+KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11
+CGBO=4.2580E-10 CJ=2.9596E-04 MJ=4.2988E-01 CJSW=1.8679E-10
+MJSW=1.5252E-01 PB=7.3574E-01
```

## Mosis Fabricated Chip Model Parameters (T1AZ)

### (A) Model Parameters for n-MOS transistors.

```
. MODEL CMOSN NMOS LEVEL=3 TOX=3.07E-8 NSUB=2.75325E15  
+GAMMA= 0.7620845 PHI=0.7 VTO=0.6298903 DELTA=0.8569392  
+UO=702.9336344 ETA=9.99916E-4 THETA=0.0734963 KP=7.195017E-5  
+VMAX=2.766785E5 KAPPA=0.5 RSH=0.0474566 NFS=6.567094E11 TPG=1  
+XJ=3E-7 LD=4.271014E-12 WD=7.34313E-7 CGDO=1.75E-10  
+CGSO=1.75E-10 CGBO=1E-10 CJ=2.944613E-4 PB=0.9048351 MJ=0.5  
+CJSW=1.236957E-10 MJSW =0.05
```

### (B) Model Parameters for p-MOS transistors.

```
. MODEL CMOSP PMOS LEVEL=3 TOX=3.07E-8 NSUB=1E17 GAMMA=0.4940829  
+PHI=0.7 VTO=-0.8615406 DELTA=0.5236605 UO=250 ETA=7.55184E-3  
+THETA=0.1344949 KP=2.438731E-5 VMAX=9.345228E5 KAPPA=200  
+RSH=36.5040447 NFS=5.518964E11 TPG=-1 XJ=2E-7 LD=9.684773E-12  
+WD=1E-6 CGDO=2.09E-10 CGSO=2.09E-10 CGBO=1E-10 CJ=2.965467E-4  
+PB=0.744678 MJ=0.4276703 CJSW=1.619193E-10 MJSW=0.1055522
```

## Appendix B

### Chip Testability

Figure B.1 shows the 10-bit DAC with BICS in 2.25 mm × 2.25 mm padframe. Figure B.2 shows the Microchip photograph of 10-bit DAC with BICS. The design includes individual sub-modules for testing the device.

#### B.1 Inverter Module and Testing.

PIN No.	Description
13	Input
14	Output

DC test was performed on the independent inverter module to test if the chip did not have fabrication problems. Logic ‘0’ is applied at the input pin #13 and output (logic ‘1’) is observed on pin #14. A logic ‘1’ is applied at the input pin #13 and output (logic ‘0’) is observed on pin #14.

#### B.2 Opamp Module and Testing

PIN No.	Description
8	Positive OPAMP
6	OPAMP Output
9	Negative OPAMP

The opamp is tested by giving a sine wave with 4V p-p to the positive input pin #8 and the output is observed at the output pin #6. The negative input pin is grounded.

### B.3 Sample and hold Circuit and Testability

PIN No.	Description
1	S/H Output
2	Control voltage
4	S/H Input

The sample and hold circuit is tested by giving 4V p-p sine wave. The control voltage of the sampling capacitor is a pulse of  $\pm 2.5V$ . When the pulse is HIGH, the input is sampled and when the pulse is LOW, the circuit is in the hold mode. The output is observed at pin #1.

### B.4 10-bit DAC with BICS and Testability

Table B.1 gives the pin numbers and their description to test 10-bit DAC

Pin No.	Description of PIN
1	S/H Output
2	Control Voltage
3	$V_{SS}$
4	S/H Input
5	$V_{DD}$ (corner pad)
6	OPAMP Output
7	$V_{DD}$
8	Positive Input (OPAMP)

<b>9</b>	<b>Negative Input (OPAMP)</b>
<b>10</b>	<b>V<sub>SS</sub></b>
<b>11</b>	<b>Input Bit (D<sub>10</sub>)</b>
<b>12</b>	<b>Input Bit (D<sub>9</sub>)</b>
<b>13</b>	<b>Input (Test Inverter)</b>
<b>14</b>	<b>Output (Test Inverter)</b>
<b>15</b>	<b>V<sub>DD</sub> (Corner Pad)</b>
<b>16</b>	<b>Input Bit (D<sub>8</sub>)</b>
<b>17</b>	<b>Input Bit (D<sub>7</sub>)</b>
<b>18</b>	<b>Input Bit (D<sub>6</sub>)</b>
<b>19</b>	<b>Input Bit (D<sub>5</sub>)</b>
<b>20</b>	<b>Input Bit (D<sub>4</sub>)</b>
<b>21</b>	<b>Input Bit (D<sub>3</sub>)</b>
<b>22</b>	<b>Input Bit (D<sub>2</sub>)</b>
<b>23</b>	<b>Input Bit (D<sub>1</sub>)</b>
<b>24</b>	<b>Error-Signal-2</b>
<b>25</b>	<b>V<sub>SS</sub> (Corner Pad)</b>
<b>26</b>	<b>Error-Signal-1</b>
<b>27</b>	<b>V<sub>CONTROL</sub></b>
<b>28</b>	<b>V<sub>ENABLE</sub></b>
<b>29</b>	<b>Error-Signal-3</b>
<b>30</b>	<b>V<sub>DD</sub></b>
<b>31</b>	<b>BICS Output</b>

<b>32</b>	<b>EXT</b>
<b>33</b>	<b>Error-Signal-4</b>
<b>34</b>	<b>BICS output for Test module</b>
<b>35</b>	<b>V<sub>SS</sub> (Corner Pad)</b>
<b>36</b>	<b>DAC output</b>
<b>37</b>	<b>V<sub>SS</sub></b>
<b>38</b>	<b>V<sub>GND</sub></b>
<b>39</b>	<b>V<sub>REF</sub></b>
<b>40</b>	<b>V<sub>DD</sub></b>

### **B.5 10-bit DAC Testing in Normal Mode**

1. Supply voltages of  $\pm 2.5\text{V}$  is given to the power supply pin numbers of the chip ( $V_{DD} = +2.5\text{V}$  and  $V_{SS} = -2.5\text{V}$ ).
2. The  $V_{ENABLE}$  pin (#28) is given a ‘high’ voltage ( $+2.5\text{V}$ ), which makes the BICS to function in the normal mode.
3. The EXT pin (#32) is connected to the  $V_{SS}$  ( $-2.5\text{V}$ ) when the BICS is in the normal mode. ( $V_{ENABLE} = '1' = +2.5\text{V}$ )
4. The fault-injection transistors must be de-activated by giving a ‘low’ voltage ( $-2.5\text{V}$ ) to the error-signals  $V_{E1}$ ,  $V_{E2}$ ,  $V_{E3}$  and  $V_{E4}$ .
5. The DAC is tested with giving various combinations of inputs to the digital input pins 11,12,16-23. (MSB – LSB).
6. The output of the DAC is observed at pin #36 on the oscilloscope.

## **B.6 I<sub>DDQ</sub> Testing of the 10-bit DAC in Test Mode**

1. The  $V_{ENABLE}$  is given a LOW voltage (-2.5V) to make BICS operate in the test mode.
2. The fault-injection n-MOS transistors are activated by connecting the error-signals  $V_{E1}$ ,  $V_{E2}$ ,  $V_{E3}$  and  $V_{E4}$  to a HIGH voltage (+2.5V)
3. The reference current generated on-chip is about 1mA.
4. When the error signals are activated, faults are injected into the chip and the faulty current shoots up to 3mA.
5. The PASS/FAIL output is observed. The output of the BICS shows a HIGH value (PASS/FAIL = '1' = +2.5V) when the faults are injected into the chip and when the BICS is in test mode. When the BICS is in the normal mode the output is LOW (PASS/FAIL = '0' = -2.5V).

## **B.7 Testing of 10-bit DAC using Logic Analyzer HP 1660CS**

1. The  $V_{ENABLE}$  is given a pulse input. When the pulse input is 'high' the BICS is in the normal mode and when the pulse input is low the BICS is in the test mode.
2. The Error Signal is given a high voltage (+2.5V).
3. The PASS/FAIL output is observed. The output of the BICS shows a HIGH value (PASS/FAIL = '1' = +2.5V) when the  $V_{ENABLE}$  is low and the Error Signal is high. The output of the BICS shows a low value (PASS/FAIL = '0' = -2.5V) when the  $V_{ENABLE}$  is high and the Error Signal is 'high' since the BICS is disabled.



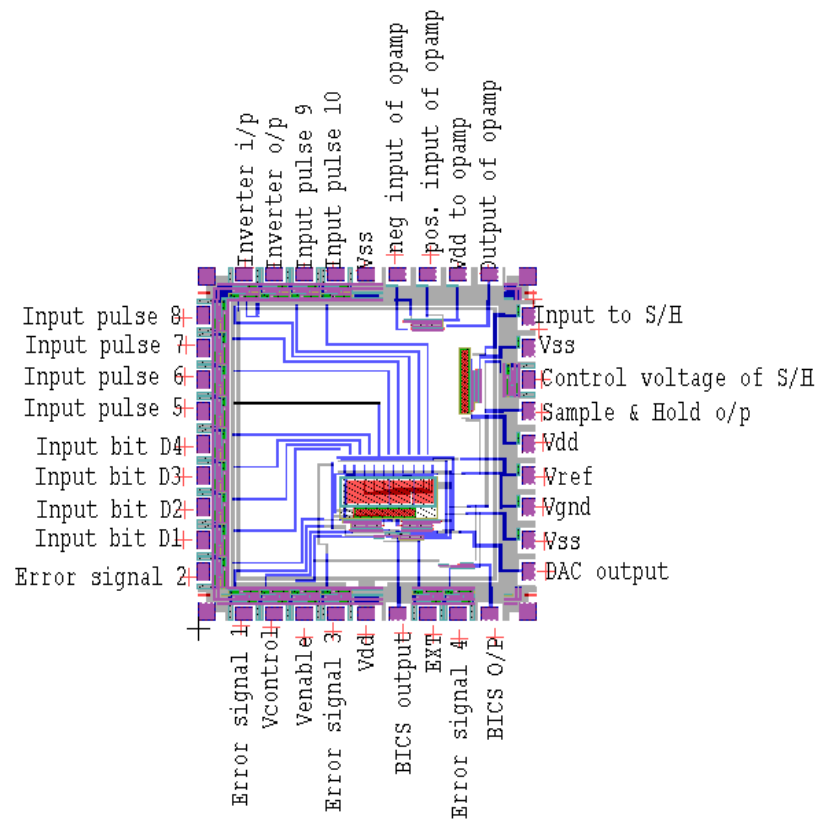


Figure: B.1 10-bit DAC with BICS in the 2.25 mm  $\times$  2.25 mm padframe.

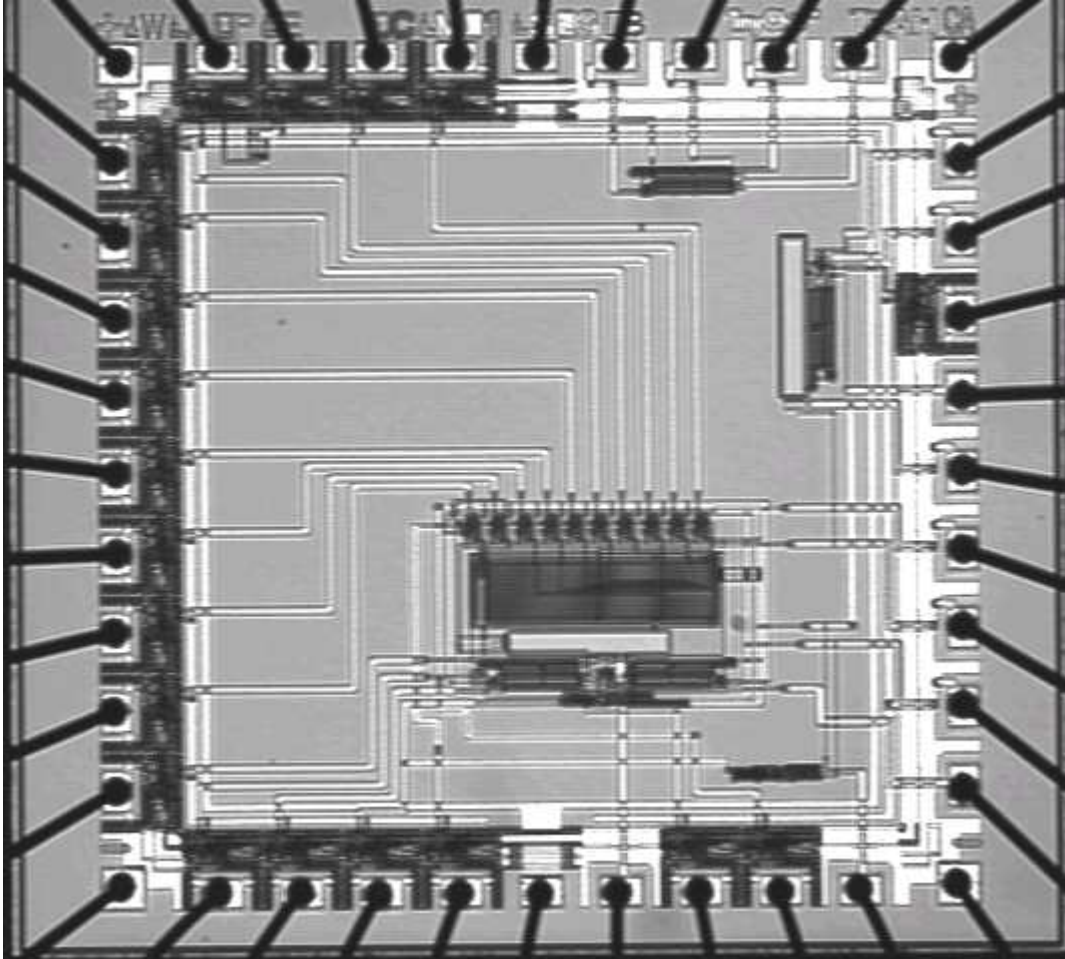


Figure B.2: Microchip photograph of 10-bit charge scaling DAC and BICS for  $I_{DDQ}$  testing.

## **Vita**

Srinivas Rao Aluri was born on June 20, 1978, in Hyderabad, India. He received his Bachelor of Engineering in Electronics and Communication Engineering degree from Osmania University, Hyderabad, India, in April, 2000. He was enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, to attend graduate school. He is presently working for Micron Technology Inc., Allen, Texas. His research interests include  $I_{DDQ}$  Testing of Mixed signal Integrated Circuits and Memory design.