High-frequency CMOS VLSI chip testability and on-chip interconnect modeling

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HIGH-FREQUENCY CMOS VLSI CHIP TESTABILITY AND ON-CHIP INTERCONNECT MODELING

A Thesis

Submitted to the Graduate Faculty of the Louisiana State University and Agricultural and Mechanical College in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

in

The Department of Electrical and Computer Engineering

by

Evan Ross Shultz
B.S.E.E., Tulane University, 2002
December 2005
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Abstract

As high-speed digital and radio-frequency mixed-signal integrated circuits become increasingly common in product designs in industry, it is important for VLSI designers to be familiar with the challenges of chip testing and the behavior of circuit elements, including on-chip interconnect, at high frequencies. Expensive, specialized test equipment and software simulation packages for high-frequency chip testing and design are not always accessible for student research. This thesis documents the setup and characterization of a best-possible environment for high-frequency chip testing and data acquisition using existing laboratory equipment and resources. Experimental methodologies and measurement results of on-chip interconnect signal integrity and delay, ring oscillator noise and timing jitter, and time-domain reflectometry (TDR) testing are presented. Methods of modeling on-chip interconnect at high frequencies using field solvers and equivalent circuits are discussed. Lastly, the designs of single-ended and differential ring oscillators, for use in future voltage-controlled oscillator (VCO) and phase-locked loop (PLL) test chip designs, are presented and analyzed.
Chapter 1

Introduction

A dominant trend in integrated circuit design is higher-speed, higher-frequency operation. High-performance computing systems require integrated circuit components that operate with high-frequency, fast-switching, stable clock signals and buses. Increasingly small, low-power wireless communication devices operating at gigahertz frequencies need radio-frequency (RF) mixed-signal integrated circuits and fast digital signal processors. Designing and testing these high-frequency devices is increasingly challenging for engineers.

To be prepared for these challenges in the workplace, it is important for today’s VLSI designers to gain a basic understanding of the challenges and methods of accurate signal measurement and chip testing at high frequencies. Most student chip designs are tested only at relatively low frequencies (i.e. kiloHertz range) and are not tested for high-speed performance or RF functionality. Higher-frequency chip testing requires more careful evaluation of the effects of the measurement system on the circuit under test, including instrument specifications (analog bandwidth, sample rate, rise time, input impedance) and parasitics (socket capacitances, probe loading, ground lead inductance, transmission line effects, interference). Expensive, specialized equipment for high-speed chip testing is not always available for research. Therefore, it is important to identify and understand the best-possible setup for high-frequency chip testing using existing laboratory equipment and resources.

When designing integrated circuits for high-frequency applications, it is necessary to take into account the effects of interconnect (both global and on-chip) on delay and signal integrity. As operating frequencies and speeds increase, signal delay and distortion due to interconnect lengths (signal flight times), parasitics (both capacitive and inductive), impedance mismatches,
transmission line effects, and crosstalk become more pronounced. Accurately modeling on-chip interconnect can be challenging, complex, and expensive. Experimentally measuring on-chip interconnect delay and impedance as well as learning basic techniques for approximating and simulating interconnect performance will improve future high-frequency designs.

The design and performance of CMOS ring oscillators used for on-chip signal generation in voltage-controlled oscillator (VCO) and phase-locked loop (PLL) devices can also affect the integrity of high-frequency designs. Ring oscillator architecture, ring length, and MOS channel dimensions greatly affect frequency, rise time, amplitude range, noise, and jitter, as well as chip footprint and power dissipation. It is necessary to understand the performance characteristics and tradeoffs associated with ring oscillator designs as well as accurate simulation techniques for robust high-frequency chip designs and good simulation-to-silicon accuracy.

This thesis documents the setup and characterization of the laboratory environment for high-frequency measurements using available instrumentation and resources, experimental test measurements of on-chip interconnect and ring oscillator performance, interconnect simulation techniques, and ring oscillator designs. Chapter 2 provides an evaluation of the functionality and specifications of available test instruments, particularly the Tektronix 11801A Digital Sampling Oscilloscope and the HP 8133A 3 GHz Pulse Generator, as well as an analysis of the effects of instrument performance on high-frequency measurement accuracy. It also documents the design and construction of a socket interface board, as well as the implementation of a data acquisition system developed using LabVIEW 7 Express and MATLAB 6.5 to acquire oscilloscope data via a GPIB interface. Chapter 3 presents experimental results from measurements enabled by this setup, including on-chip interconnect delay; ring oscillator frequency, noise, and jitter; and time-domain reflectometry (TDR) tests. Chapter 4 discusses on-chip interconnect SPICE simulation
models generated using field solvers and equivalent circuit approximations. Chapter 5 presents the designs and layouts of 0.5 µm CMOS process single-ended and differential ring oscillators, accurate SPICE simulation techniques and considerations, simulation results, and simulation-to-silicon correlation. Chapter 6 summarizes the results and conclusions.
Chapter 2

Measurement Environment Setup and Characterization

2.1 Overview

To define the best-possible high-frequency measurement environment, the performance specifications of all available laboratory instruments, particularly the Tektronix 11801A Digital Sampling Oscilloscope and the Hewlett-Packard 8133A 3 GHz Pulse Generator, were examined. The impact of specifications such as analog bandwidth and signal rise time on the accuracy and limitations of high-frequency digital signal measurements was analyzed, and the capabilities of the aforementioned test equipment were experimentally verified. An IC chip socket board was designed and constructed to provide the cleanest-possible interface between the device under test (DUT), the pulse generator, and the oscilloscope. To store, display, and analyze high-frequency signal waveforms from the 11801A oscilloscope on a PC, a custom LabVIEW driver application was developed to access and store data from the instrument via a GPIB bus interface. Finally, a MATLAB parsing script was written to import raw waveform data captured from the 11801A oscilloscope for flexible display and analysis.

2.2 Instrument Specifications and Performance Analysis

2.2.1 Tektronix 11801A Digital Sampling Oscilloscope

The Tektronix 11801A Digital Sampling Oscilloscope was the highest performance test instrument available for high-frequency, fast-rise, digital signal acquisition and measurement. Analog oscilloscopes, which directly apply the measured signal voltage to the vertical axis of the electron beam of a cathode-ray tube (CRT) display, are generally limited in bandwidth ($BW$) by CRT write speeds ($BW_{max} < 1$ GHz). Standard “real-time sampling” digital oscilloscopes, which
include digital storage (DSO) and digital phosphor (DPO) oscilloscopes, sample the input signal at a constant rate, with a fixed delay between samples, and simultaneously reconstruct the signal from the samples in the order they are taken (i.e. real-time). These oscilloscopes can reconstruct both transient and periodic signals, but their bandwidths are limited by practical analog-to-digital converter (ADC) sampling rates according to Nyquist’s theorem, which holds that

\[ BW \leq \frac{f_s}{2} \]  

(2.1)

where \( f_s \) is the ADC sampling frequency (\( BW_{max} < 7 \text{ GHz} \)). “Equivalent-time sampling” digital oscilloscopes like the 11801A, however, utilize sampling heads that accumulate samples taken over several periods of a periodic input signal. The samples are taken at slightly different time intervals so that, by piecing together samples taken over several periods, the sampling heads can reconstruct periodic signals with much higher “equivalent” sampling rates [1]. The oscilloscopes then poll the sampling heads at relatively low frequency to acquire the complete, high-resolution input signal captures. These oscilloscopes have “equivalent” periodic signal bandwidths up to an order of magnitude greater than those of other digital oscilloscopes (\( BW_{max} < 70+ \text{ GHz} \)), limited only by the timing precision of the sampling heads. However, since repetitive sampling is used, non-periodic events (e.g. transients, glitches) cannot be captured. Also, since neither attenuators nor protection diodes can be placed before the sampling heads, the dynamic range of most digital sampling oscilloscopes is limited to about 1 V\(_{p-p}\) (peak-to-peak) with a maximum safe peak input voltage of \( \pm 3 \text{ V} \), versus typically 100 V\(_{p-p}\) and \( \pm 500 \text{ V} \), respectively, for other oscilloscopes [2].

The Tektronix 11801A oscilloscope consists of a “mainframe” with a touch-sensitive display, button and knob controls, and four available compartments for interchangeable sampling heads. The only notable performance specification of the mainframe is its 200 kHz maximum sampling head polling rate [3]; the overall oscilloscope bandwidth, rise time, dynamic range,
maximum input voltage, input impedance, and other performance characteristics are determined by the installed sampling head(s). Four Tektronix sampling head models were available for use: model numbers SD-14, SD-22, SD-24, and SD-26. Table 2.1 on Page 7 summarizes the critical performance specifications and applications of each sampling head model [4-6]. The SD-14 and SD-24 sampling heads were used for all experimental measurements for maximum bandwidth, source and cabling impedance matching (50 Ω), and time-domain reflectometry (TDR) testing capability. With these sampling heads installed, the Tektronix 11801A vastly outperformed two other available digital oscilloscopes, the Tektronix TDS3052 DPO and the HP 54602B DSO, for high-frequency, fast-rise, low-voltage measurements. Table 2.2 on Page 8 summaries the performance specifications of these three oscilloscopes [3, 6-8].

One important disadvantage of the 11801A oscilloscope is its lack of an internal auto triggering source. The internal clock trigger of the 11801A is synchronized with its 100 kHz calibration signal and cannot be used for stable triggering of test measurements. An external triggering source synchronized with the measured signal must be supplied to the external trigger input on the 11801A mainframe. This input has a bandwidth of 2 GHz and maximum voltage limits of ± 1 V (or ± 5 V with X10 attenuation enabled). If the measured signal is produced by or synchronized with a function or pulse generator, the external trigger output of the generator can be connected directly to the trigger input on the 11801A to supply the triggering source. If the measured signal is generated on-chip or is otherwise unsynchronized to any existing external trigger source, the measured signal itself can be split and connected to the trigger input to supply its own triggering source.

Before each measurement task, the 11801A oscilloscope must be initialized to restore factory settings. Once the instrument has been turned on, it is initialized by pressing the Utility
Table 2.1: Sampling Head Performance Specifications

<table>
<thead>
<tr>
<th>Model #:</th>
<th>Analog Bandwidth</th>
<th>Rise Time 10-90%</th>
<th>Dynamic Range</th>
<th>Max Input Voltage</th>
<th>Input Impedance</th>
<th>Connector / Probe Type</th>
<th>TDR</th>
<th>Application</th>
</tr>
</thead>
</table>
| SD-14      | 3 GHz            | < 140 ps         | $7V_{p-p} < 570$ MHz  
1.33 $V_{p-p}$ @ 3 GHz | ± 15 V          | 100 kΩ || 0.475 pF | Handheld Probe  | No  | Low-frequency, slow-rise, high-voltage probing |
<p>| SD-22      | 12.5 GHz         | &lt; 28 ps          | 1 $V_{p-p}$    | ± 3 V            | 50 Ω Terminated  | SMA-f Coaxial          | No  | High-frequency, fast-rise, low-voltage load for 50 Ω source and interconnect |
| SD-24      | 20 GHz           | &lt; 17.5 ps        | 1 $V_{p-p}$    | ± 3 V            | 50 Ω Terminated  | SMA-f Coaxial          | Yes | Highest-frequency, fastest-rise, low-voltage load for 50 Ω source and cabling; TDR measurements |
| SD-26      | 20 GHz           | &lt; 17.5 ps        | 1 $V_{p-p}$    | ± 3 V            | 50 Ω Terminated  | SMA-f Coaxial          | No  | Highest-frequency, fast-rise, low-voltage load for 50 Ω source and cabling |</p>
<table>
<thead>
<tr>
<th>Model #</th>
<th>Type</th>
<th>Max Sampling Rate</th>
<th>Max Analog Bandwidth</th>
<th>Rise Time</th>
<th>Dynamic Range</th>
<th>Max Input Voltage</th>
<th>Input Impedance</th>
<th>Connector / Probe Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tektronix 11801A w/ SD-24</td>
<td>Digital Sampling</td>
<td>200 kSa/s</td>
<td>20 GHz</td>
<td>&lt; 17.5 ps</td>
<td>1 V&lt;sub&gt;p-p&lt;/sub&gt;</td>
<td>± 3 V</td>
<td>50 Ω Termination</td>
<td>SMA-f Coaxial</td>
</tr>
<tr>
<td>Tektronix TDS3052 DPO</td>
<td>Digital Phosphor</td>
<td>5 GSa/s</td>
<td>500 MHz</td>
<td>0.7 ns</td>
<td>80 V&lt;sub&gt;p-p&lt;/sub&gt; (into 1 MΩ)</td>
<td>± 400 V (into 1 MΩ)</td>
<td>Selectable: 1 MΩ</td>
<td></td>
</tr>
<tr>
<td>HP 54602B DSO</td>
<td>Digital Storage</td>
<td>20 MSa/s</td>
<td>150 MHz</td>
<td>&lt; 2.33 ns</td>
<td>64 V&lt;sub&gt;p-p&lt;/sub&gt;</td>
<td>± 400 V</td>
<td>1 MΩ</td>
<td></td>
</tr>
</tbody>
</table>
menu button, touching Initialize at the bottom-left corner of the display, and touching Initialize in the Verify Initialize pop-up menu, as outlined in Figure 2.1. Following initialization, signal waveforms are toggled on and off by pressing the Select Channel buttons on the fronts of the sampling heads for each active channel. On-screen cursors as well as the Cursors menu are invoked by touching the Cursors icon at the top of the display. Cursor position is adjusted with the control knobs, and cursor type is selected in the Cursors menu as shown in Figure 2.2. A multitude of waveform measurements in default Software Mode can be applied by pressing the Measure menu button, touching Measurements at the bottom of the display, and touching up to six measurements in the Measurements pop-up menu, as shown in Figure 2.3.

Advanced measurement capabilities of the Tektronix 11801A oscilloscope, including jitter, noise, and TDR measurements, are documented separately in Chapter 3. Details of the instrument’s programming interface and GPIB bus support, used for interfacing the oscilloscope with a PC for waveform acquisition and storage, are provided in Sections 2.4 and 2.5.

2.2.2 Hewlett-Packard 8133A 3 GHz Pulse Generator

The HP 8133A 3 GHz Pulse Generator was the most capable instrument available for the generation of high-frequency, fast-rise signals for test measurements. It can produce two complementary square wave and variable pulse width signals with a period range of 333 ps to 30.303 ns (clock frequency of 33.0 MHz to 3.0000 GHz) and fast rise times of < 100 ps (< 60 ps typical). Its 50 Ω source impedance outputs have a limited output voltage range of 0.30 V_p-p to 3.00 V_p-p within a - 2.00 V to + 4.00 V window into a 50 Ω load, though it is sufficient for high-frequency measurements with the 11801A oscilloscope. Its 50 Ω external trigger output is synchronized with the two signal outputs and features an output voltage range of 0.50 V_p-p to 1.80 V_p-p within a - 4.00 V to + 4.00 V window, which meets the requirements for direct
Figure 2.1: Tektronix 11801A Oscilloscope Initialization

<table>
<thead>
<tr>
<th>GPIB/RS232C</th>
<th>Identify</th>
<th>Color</th>
<th>Hardcopy</th>
<th>Main Size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bitmap Screen</td>
<td>Main Pos</td>
</tr>
<tr>
<td>Initialize</td>
<td>Instrument Options</td>
<td>Labeling</td>
<td>Page to Enhanced Accuracy</td>
<td>Remove/Clear Trace</td>
</tr>
<tr>
<td>Verify Initialize</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Initialize</td>
<td>Cancel</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 2.2: Tektronix 11801A Oscilloscope Cursor Controls
Figure 2.3: Tektronix 11801A Oscilloscope Software Mode Measurements

<table>
<thead>
<tr>
<th>Measurements</th>
<th>Main Size</th>
<th>Main Pos</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compare &amp; References</td>
<td>Remove/Clip</td>
<td>Pan/Zoom</td>
</tr>
<tr>
<td>Trace 1</td>
<td>Main</td>
<td>Off</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Amplitude</th>
<th>Timing</th>
<th>Area/Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>Mean</td>
<td>Rise</td>
</tr>
<tr>
<td>Mid</td>
<td>RMS</td>
<td>Frequency</td>
</tr>
<tr>
<td>Min</td>
<td>Over Shoot</td>
<td>PropDelay</td>
</tr>
<tr>
<td>Peak-Peak</td>
<td>Under Shoot</td>
<td>Width</td>
</tr>
<tr>
<td>Amplitude</td>
<td>Extinct Ratio</td>
<td>Phase</td>
</tr>
<tr>
<td>Noise</td>
<td>SNR</td>
<td>Spectral Mag</td>
</tr>
</tbody>
</table>

| Exit | Clear All | Default Parameters | THD |
connection to the 11801A oscilloscope’s 50 Ω external trigger input [9]. The HP 8133A far outperformed the other two available pulse generators, the Tektronix PG508 50 MHz Pulse Generator and the HP 33120A Function Generator, in clock period and rise time performance for high-frequency testing. Table 2.3 below highlights the performance differences [9-10].

Table 2.3: Pulse Generator Performance Comparison

<table>
<thead>
<tr>
<th>Model #</th>
<th>Max Clock Frequency</th>
<th>Min Rise Time</th>
<th>Max Voltage (into 50 Ω)</th>
<th>Coaxial Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP 8133A</td>
<td>3 GHz</td>
<td>&lt; 100 ps</td>
<td>3 V_{p-p}</td>
<td>SMA-f</td>
</tr>
<tr>
<td>Tektronix PG508</td>
<td>50 MHz</td>
<td>5 ns</td>
<td>10 V_{p-p}</td>
<td>BNC-f</td>
</tr>
<tr>
<td>HP 33120A</td>
<td>15 MHz</td>
<td>20 ns</td>
<td>10 V_{p-p}</td>
<td>BNC-f</td>
</tr>
</tbody>
</table>

When the HP 8133A is turned on, the signal outputs can be toggled between square wave (50% duty cycle) or variable-width pulse output by pressing the PULSE/SQUAR button on the PULSE front panel. The pulse width setting is accessed by pressing the WIDTH/DCYC button until the WIDTH option is selected. The output voltage range is set either by 1) defining the peak-to-peak amplitude plus offset, by pressing the AMPL/HIGH and OFFS/LOW buttons to select AMPL followed by OFFS; or 2) defining the exact high and low output voltages, by pressing the same buttons to select HIGH followed by LOW instead. Clock frequency and period are accessed by pressing the FREQ/PERIOD button on the TIMEBASE front panel to select and modify either option. When each setting is accessed and displayed on the instrument’s LCD, its value is modified using the Vernier buttons to adjust each digit individually.

2.2.3 Performance Specification Analysis and Evaluation

The most critical performance specifications affecting accurate high-frequency signal measurements are the interrelated analog bandwidth and rise time of the system. It is important not to confuse the analog bandwidth of an oscilloscope with the clock frequency of a measured
digital signal. Clock frequency is simply the number of low-to-high and high-to-low transitions per second and is not directly comparable to the analog bandwidth of the measurement system. For example, an oscilloscope with a bandwidth of 1 GHz cannot accurately display a 1 GHz square-wave digital clock signal. The analog bandwidth specifies the oscilloscope’s ability to measure the spectral frequency components of a digital signal, where the stated bandwidth is the -3 dB (50% power, 70% voltage) point of the oscilloscope’s frequency response curve. An ideal digital clock signal, modeled as a periodic square wave with a 50% duty cycle, is a superposition of an infinite number of sinusoidal functions with frequencies that are odd multiples above the fundamental clock frequency. The spectral frequency component coefficients are given by the Fourier series expansion

\[ f(t) = \frac{2}{\pi} \sum_{n=1,3,5 \ldots}^{\infty} \frac{1}{n} \sin(2\pi nf_0 t) \]  

(2.2)

where \( f_0 \) is the clock frequency [1]. A significant portion of the power spectral density extends to the fifth harmonic, i.e. five times the clock frequency. Thus, for example, an ideal 1 GHz digital clock signal would require an analog bandwidth of at least 5 GHz for reasonably accurate measurement. “Five times the clock frequency” is a commonly used rule of thumb for quickly estimating the capability of laboratory equipment for digital signal measurements [1].

Similarly, signal rise and fall times are directly related to system bandwidth. As signal transition times decrease (i.e. faster edge rates), the energy in higher spectral frequency components increases, and larger bandwidth is required to measure the signal accurately. An ideal pulse with zero rise time, modeled as a Dirac impulse delta function, has a flat frequency spectrum and would require infinite bandwidth. A simple, practical relationship between rise time and bandwidth can be derived from the step response of an ideal input signal into a network with an \( RC = \tau \) time constant, given by
\[ V = V_{input} (1 - e^{-t/\tau}) \]  

(2.3)

where \( V_{input} \) is the voltage of the input signal [1]. For \( V_{input} = 1 \) V, the 90\% rise time \((V = 0.9 \) V) from Equation 2.2 is

\[ t_{90\%} = (-\ln 0.1)\tau \approx 2.3\tau \]  

(2.4)

Similarly, the 10\% rise time \((V = 0.1 \) V) is

\[ t_{10\%} = (-\ln 0.9)\tau \approx 0.105\tau \]  

(2.5)

Thus, the standard 10\% to 90\% rise time is

\[ t_{rise} = t_{90\%} - t_{10\%} \approx (2.3 - 0.105)\tau = 2.195\tau \]  

(2.6)

The frequency response (i.e. bandwidth) of a simple \( RC \) network is given by

\[ BW = f_{3\,dB} = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau} \]  

(2.7)

Combining Equations 2.6 and 2.7 yields

\[ BW = \frac{2.195}{2\pi t_{rise}} \],

\[ BW = \frac{0.35}{t_{rise}}. \]  

(2.8)

Thus, for example, an oscilloscope with a 1 GHz bandwidth would display an ideal step function as a 350 ps rise time pulse. However, since a real step function will have finite edge rates depending on the generator instrument and interconnect, the signal source and the oscilloscope form a system with a degraded 10\%-90\% rise time of

\[ t_{system} = \sqrt{t_{signal}^2 + t_{oscilloscope}^2} \]  

(2.9)

which will appear slower than the rise times of both the measured signal and the oscilloscope [1]. For example, if a 350 ps rise-time signal is measured with a 350 ps rise-time (1 GHz bandwidth)
oscilloscope, the displayed waveform will have an apparent rise time of 495 ps. However, if an
clockscope with five times the bandwidth (5 GHz, 70 ps) is used, the apparent rise time is a
more accurate 357 ps. Thus, the same “five times” rule of thumb applies for quickly estimating
the rise time performance of laboratory instruments.

When a handheld probe is used for signal acquisition, the probe’s $RC$ network becomes
another part of the measurement system. The overall system rise time is further degraded to

$$t_{\text{system}} = \sqrt{t_{\text{signal}}^2 + t_{\text{probe}}^2 + t_{\text{oscilloscope}}^2}$$

(2.10)

which shows that the effective bandwidth of the combined probe and oscilloscope will be less
than the specified bandwidth of either component [1]. For example, a 1 GHz probe used with the
1 GHz oscilloscope will result in a combined effective bandwidth of only 707 MHz with a rise
time of 495 ps. Used to measure the original 350 ps rise-time signal, the combined system will
display a waveform with an apparent rise time of 606 ps. Another problem associated with the
use of handheld probes is the effect of ground lead inductance at high frequencies. Inductance in
the return path of a measured signal through a probe causes high-frequency ringing in the
displayed waveform, with a ring frequency of

$$f_{\text{ring}} = \frac{1}{2\pi \sqrt{LC}}$$

(2.11)

where $L$ is the sum of the source and ground lead inductances and $C$ is the input capacitance of
the probe [11]. A rule of thumb for approximating ground lead inductance is roughly 25 nH per
inch [11]. So, even a high-frequency, low-capacitance 50 $\Omega$ passive probe with a minimal 1 pF
input capacitance and one-inch ground lead will introduce an $f_{\text{ring}}$ of 1.01 GHz. Therefore, to
maximize bandwidth, minimize rise times and impedance discontinuities, and eliminate ground
lead inductance effects, all of the components of a high-frequency test measurement system
(signal generator, interface hardware, oscilloscope) should be directly connected using matched-impedance coaxial interconnect. High-frequency instruments such as the Tektronix 11801A and the HP 8133A specifically use SMA microwave coaxial connectors for their higher bandwidths (DC to 18 GHz) instead of the lower-bandwidth standard BNC connectors (DC to 4 GHz) [12].

To evaluate the practical maximum performance of the 8133A pulse generator and the 11801A oscilloscope, the two instruments were connected directly using Tektronix 174-1428-00 60-inch, low-capacitance, 50 Ω, SMA-male to SMA-male coaxial semi-rigid cables for test measurements. To compare rise-time performance, the Tektronix PG508 and HP 33120A signal generators were also tested with direct cable connections using available BNC-to-SMA adapters. Table 2.4 below summarizes the measurement results. The high-frequency HP 8133A achieved a superior practical minimum rise time of 50 ps, corresponding to a bandwidth of 7 GHz.

Table 2.4: Pulse Generator 10%-90% Rise Time (1 V_{p-p}) Measurement Results

<table>
<thead>
<tr>
<th>Model #</th>
<th>Rise Time Specification</th>
<th>Rise Time Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP 8133A</td>
<td>&lt; 100 ps</td>
<td>50 ps</td>
</tr>
<tr>
<td>Tektronix PG508</td>
<td>5 ns</td>
<td>5.5 ns</td>
</tr>
<tr>
<td>HP 33120A</td>
<td>20 ns</td>
<td>17 ns</td>
</tr>
</tbody>
</table>

Next, the practical bandwidth limitations of the 11801A oscilloscope were evaluated. Figure 2.4 shows 100 MHz, 1 GHz, 2 GHz, and 2.6 GHz pulse shapes captured with a direct cable connection from the 8133A to the oscilloscope. Minor overshoot and ringing due to slight impedance mismatches in the cable interface are evident above 1 GHz, but signal integrity is reasonable up to 2.5 GHz. However, the oscilloscope lost trigger stability at 2.6 GHz and above, likely caused by attenuation of the external trigger signal due to the trigger input’s 2 GHz limit.

In summary, the experimentally-verified performance limitations of the 11801A/8133A test measurement system include a 50 ps rise time, 7 GHz analog bandwidth, and 2.5 GHz clock
Figure 2.4: Measured Pulse Shapes  
(a) 100 MHz  
(b) 1 GHz  
(c) 2 GHz  
(d) 2.6 GHz
frequency. Performance in practical circuit measurements further depends on the parasitics and impedance mismatches present in the interface hardware used to connect the pulse generator and oscilloscope to the device under test.

2.3 DUT Interface Board Design

The quality of the hardware designed to interface the integrated circuit device under test (DUT) with the signal generator and oscilloscope is usually the limiting factor in the overall performance of the high-frequency measurement system. Parasitic capacitances and impedance discontinuities inherent in the physical geometries of connectors and cabling reduce bandwidth, slow signal edge rates, and cause voltage and current reflections. Unshielded components and wiring can inject significant RF noise and electromagnetic interference (EMI) into the signal path. Additively, these disturbances severely compromise signal integrity, which is critical for high-frequency accuracy.

Standard solderless socketed protoboards/breadboards with unshielded jumper wire were tested and found to support frequencies below 1 MHz only. An existing DUT interface box, comprised of BNC-female coaxial input/output connectors permanently wired to an IC socket inside a metal enclosure, was also tested and found to support frequencies only up to 10 MHz. For optimal signal integrity, custom printed circuit board (PCB) hardware with surface-mount connectors and components must be used. However, since PCBs are costly and complex to design, a PCB solution was not available for experimental measurements. Therefore, a socketed component interface board was carefully designed and constructed to achieve the best possible signal integrity and bandwidth with available resources.

The interface board top side and key design features are illustrated in Figure 2.5. Side and bottom views, showing solder joint locations, are also illustrated in Figure 2.6. The design
Figure 2.5: DUT Interface Board Top Side
Figure 2.6: DUT Interface Board  (a) Side View  (b) Bottom View
features a perforated component board with corner standoffs, 3.5 mm SMA-female coaxial surface-mount input/output connectors attached through custom-drilled pilot holes, a 40-pin DIP IC socket, and signal jumper sockets. Gold-plated SMA connectors and sockets were used to resist corrosion for maximum signal transfer. The bodies of the SMA connectors, which are tied to the signal generator or oscilloscope ground through the outer coaxial conductor, are connected for a common ground reference for input and output signals. To minimize RF noise, shielded 22-gauge solid-conductor cabling was obtained and used to make jumpers to connect the SMA inputs/outputs to the DUT socket. Each SMA connector has two signal sockets, each with a separate ground socket for connecting the drain wire of the cabling shield to ground. Additional sockets are provided for jumping supplies, ground, or low-frequency signals to the DUT socket. The layout of the board was designed to minimize jumper length to reduce transmission line effects, noise, and parasitics.

The ultimate performance of the DUT interface board is discussed with the experimental measurement results presented in Chapter 3.

2.4 LabVIEW and MATLAB Acquisition System

2.4.1 Overview

To store, analyze, and print high-frequency signal waveform captures from the Tektronix 11801A oscilloscope, which is not equipped with a floppy disk drive or other transferable media, an acquisition system was devised and implemented using the National Instruments LabVIEW 7 Express and MathWorks MATLAB 6.5 software packages. This system interfaces the 11801A with a Windows 2000 PC via a General Purpose Interface Bus (GPIB) network, acquires and converts raw waveform data for display using a custom-developed LabVIEW driver application, and stores waveform data for import into MATLAB for advanced analysis and printing.
Significant effort was required to install and configure LabVIEW 7 Express to work concurrently with the Agilent 82350B PCI GPIB card and HP VEE instrument control software previously installed on the laboratory PC. The available and thoroughly documented HP VEE software could not be used with the 11801A because it provided neither an existing instrument driver nor a capable custom development environment to enable the GPIB interface. Agilent and National Instruments hardware and software utilize “officially incompatible” implementations of the Virtual Instrument Software Architecture (VISA) language used to handle low-level function calls over the GPIB network. However, a successful installation method was found to allow for side-by-side installation of Agilent VISA and NI-VISA and to configure LabVIEW to pass its NI-VISA calls through Agilent VISA and the 82350B card’s I/O drivers. This method is listed in Appendix A.

2.4.2 LabVIEW 7 Express Development Environment

LabVIEW 7 Express is a powerful and versatile graphical programming development environment for a vast array of instrument control and data acquisition applications. LabVIEW allows for the creation of Virtual Instrument (VI) drivers and applications which enable user-friendly, graphical, interactive control of laboratory instruments from a PC via several interfaces and communication protocols. It also allows for advanced collection and processing of data acquired from measurement equipment. LabVIEW VIs are developed graphically by placing and interconnecting built-in or custom functional blocks which control various configurable data input, output, and mathematical operations. Each VI consists of two elements: 1) the “Front Panel,” which serves as the VI’s interactive interface, featuring realistic-looking buttons, gauges, displays, etc. to simulate real instrument controls; and 2) the “Block Diagram,” which contains the functional blocks that determine program execution, operate on Front Panel controls, and
return Front Panel display data. Front Panel and Block Diagram development is performed concurrently; for example, placing a Waveform Display graphic on the Front Panel automatically places a Waveform Display functional block in the Block Diagram, the input of which controls the Front Panel display. Figure 2.7 shows the Front Panel of one of the many built-in example VIs, and Figure 2.8 shows its corresponding Block Diagram. Figure 2.9 shows some of the built-in functional blocks used for easy drag-and-drop programming.

LabVIEW can interface with instruments via GPIB using either vendor-provided drivers or custom VIs utilizing the Instrument I/O Assistant functional block shown in Figure 2.10. The Instrument I/O Assistant automatically detects active GPIB-enabled instruments connected to the PC (designated “GPIB::x::INSTR,” where x is the instrument’s unique GPIB address) and allows individual text commands to be issued to those instruments. It then captures the raw data strings returned by the instruments and automatically parses the data into “tokens” (individual strings of similar data type) which can be output separately to other functional blocks. For example, if a “get waveform data” command is sent to an oscilloscope, the returned data string may contain several individual pieces of information (e.g. trace name, axis scales, sample values). The Instrument I/O Assistant converts the binary data string to ASCII text, identifies different pieces of colon- or comma-delimited data, and creates a separate functional block output for each piece in the correct data format (e.g. text for the trace name, decimal for the sample values). The block can be programmed to issue multiple text commands sequentially and repeatedly, enabling advanced automatic instrument control or real-time data feedback. Nearly all functions of GPIB-enabled instruments can be controlled through text commands. Programming reference manuals that list and describe supported commands are usually provided with GPIB-enabled instruments. Unfortunately, the command sets are not standardized and vary by manufacturer and instrument.
Figure 2.7: Example LabVIEW VI Front Panel
Figure 2.8: Example LabVIEW VI Block Diagram
Figure 2.9: LabVIEW Functional Blocks   (a) Root Menu   (b) Signal Analysis Menu
Figure 2.10: LabVIEW Instrument I/O Assistant   (a) Functional Block   (b) Settings Window
2.4.3 Virtual Instrument (VI) Design for the Tektronix 11801A Oscilloscope

A vendor-supplied driver for the 11801A oscilloscope was not available, so a custom VI was developed using the Instrument I/O Assistant to transfer waveform data to the PC. Two Block Diagrams were created: “Acquire (One Trace),” with Channel 1 enabled only, shown in Figure 2.11; and “Acquire (Two Traces),” with Channels 1 and 2 enabled, shown in Figure 2.12. The Front Panel, shown in Figure 2.13, is identical for the two Block Diagrams. The Instrument I/O Assistant block and settings previously shown in Figure 2.10 were taken from the “Acquire (One Trace)” VI. A sequence of three commands is issued to the 11801A to acquire trace data:

1. ABBwfmpre { ON | OFF }  (syntax: ABB ON)
2. OUTput <arg>              (syntax: OUT TRA1, OUT TRA2)
3. WAVfrm?                   (syntax: WAV?)

which abbreviates the preamble returned with each waveform query, selects the desired channel, and requests the trace preamble and data points [13]. Each unscaled trace is comprised of 512 data points, each with an unscaled integer value between ± 32767 (16-bit resolution). Four scaling factors are provided in the trace preamble: XZERO, which gives the time of the first data point in seconds; XINCR, which gives the time interval between data points in seconds; YZERO, which gives the amplitude of the median quantization level (i.e. unscaled integer value of zero) in volts; and YMULT, which gives the amplitude step between quantization levels in volts. The Instrument I/O Assistant automatically separates the data point values and scaling factors into five tokens. The unscaled data point token is fed to a Waveform Display functional block to enable real-time display of the waveform in the VI’s Front Panel. All five tokens are fed to a Write LabVIEW Measurement File functional block, which saves the currently displayed trace data as a comma-separated text file with a *.lvm file extension whenever the “Save to File” button on the Front Panel is pressed.
Figure 2.11: Acquire (One Trace) VI Block Diagram
Figure 2.12: Acquire (Two Traces) VI Block Diagram
Figure 2.13: Acquire VI Front Panel
The LabVIEW Application Builder feature was used to compile standalone Windows executable files from the developed VIs. The standalone applications enable full Front Panel functionality and faster execution while hiding the underlying Block Diagrams and development tools, and can be run on any PC with a minimal LabVIEW Runtime Library installed (the full LabVIEW package is not needed). This allows any user needing to capture and store waveforms from the 11801A oscilloscope to do so quickly and easily without any knowledge of LabVIEW. The user must simply set up the measurement on the oscilloscope, run the executable (which will automatically begin capturing data), and click “Save to File” to store the data.

Since the VI simply acquires data about the traces displayed on the 11801A and does not control the signal sampling or measurement in any way, the LabVIEW acquisition system does not affect the performance of the overall measurement system. Traces displayed on the VI Front Panel on the PC will be identical to those displayed on the 11801A’s screen.

2.4.4 MATLAB Parsing Script

To display, analyze, and print fully-scaled waveforms from the saved *.lvm files, a MATLAB function was written to parse, scale, and plot the waveform data automatically. The function prototype is

\[
[\text{TIME}, \text{TRA1}, \text{TRA2}] = \text{lvmconv}(\text{filename})
\]

where \text{filename} is the name of the *.lvm input file and \text{TIME}, \text{TRA1}, and \text{TRA2} are the arrays in which the data points are saved. The interconnect delay waveforms presented in Chapter 3 were generated using this single function call. The function source code is presented in Appendix B.
Chapter 3

Signal Integrity, Delay, Noise, Jitter, and TDR Measurements

3.1 Overview

Using the measurement environment defined in Chapter 2, several experimental test measurements related to high-frequency chip testability and circuit performance were collected. To characterize on-chip interconnect and their influence on signal integrity and timing accuracy, interconnect resistance and signal delay measurements were conducted using a 0.5 µm test chip. Single-ended ring oscillator frequency, noise, and jitter measurements were made for a 1.2 µm test chip to study on-chip signal generation performance. Time-domain reflectometry (TDR) measurement techniques were utilized to illustrate and understand the effects of impedance discontinuities on signal integrity within the measurement environment and interface hardware. The following sections document measurement methodologies, results, and analyses.

3.2 On-Chip Interconnect Resistance, Signal Integrity, and Delay

An interconnect test chip, fabricated using the AMIS C5F/N 0.5 µm process through the MOSIS fabrication service (Run # T37D), was obtained and used for experimental testing of on-chip interconnect characteristics. The layout of this chip is shown in Figure 3.1. The test chip features several long interconnect (three in each of its three metal layers and one polysilicon layer) each directly connecting a pair of input/output (I/O) pads. Each interconnect is 1.8 µm wide over the majority of its length, and parallel interconnect are separated horizontally by a minimum of 0.9 µm except at one crossover point at the center of the chip.

First, the total resistance of each interconnect was found by applying a 4 V DC supply across each I/O pair, measuring the supply current, and calculating resistance from Ohm’s Law. The sheet resistance of each metal and polysilicon layer was then estimated by calculating the
Figure 3.1: Interconnect Test Chip Layout
approximate number of square segments in one interconnect in each layer from the layout design file and dividing the total resistance by the number of segments. The estimated sheet resistances were then compared to the values given in the parametric test results for the T37D run provided by MOSIS [14]. Table 3.1 below lists the total resistances found for all of the interconnect.

Table 3.1: Measured On-Chip Interconnect Resistances

<table>
<thead>
<tr>
<th>I/O Pin Pair</th>
<th>Layer</th>
<th>Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-18</td>
<td>Metal-1</td>
<td>56.4</td>
</tr>
<tr>
<td>19-39</td>
<td>Metal-1</td>
<td>59.9</td>
</tr>
<tr>
<td>20-38</td>
<td>Metal-1</td>
<td>59.9</td>
</tr>
<tr>
<td>15-29</td>
<td>Metal-2</td>
<td>60.8</td>
</tr>
<tr>
<td>14-30</td>
<td>Metal-2</td>
<td>56.2</td>
</tr>
<tr>
<td>13-31</td>
<td>Metal-2</td>
<td>55.9</td>
</tr>
<tr>
<td>22-37</td>
<td>Metal-3</td>
<td>50.5</td>
</tr>
<tr>
<td>27-36</td>
<td>Metal-3</td>
<td>60.2</td>
</tr>
<tr>
<td>28-35</td>
<td>Metal-3</td>
<td>60.8</td>
</tr>
<tr>
<td>12-32</td>
<td>Poly</td>
<td>9.8 K</td>
</tr>
<tr>
<td>10-33</td>
<td>Poly</td>
<td>10.8 K</td>
</tr>
<tr>
<td>9-34</td>
<td>Poly</td>
<td>12.5 K</td>
</tr>
</tbody>
</table>

Table 3.2 below shows the estimated sheet resistances for each interconnect layer.

Table 3.2: Estimated On-Chip Interconnect Layer Sheet Resistances

<table>
<thead>
<tr>
<th>I/O Pin Pair</th>
<th>Layer</th>
<th># Square Segments</th>
<th>Experimental Sheet Resistance (Ω/□)</th>
<th>MOSIS-Provided Sheet Resistance (Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-18</td>
<td>Metal-1</td>
<td>612</td>
<td>0.092</td>
<td>0.09</td>
</tr>
<tr>
<td>15-29</td>
<td>Metal-2</td>
<td>630</td>
<td>0.097</td>
<td>N/A</td>
</tr>
<tr>
<td>22-37</td>
<td>Metal-3</td>
<td>779</td>
<td>0.065</td>
<td>N/A</td>
</tr>
<tr>
<td>12-32</td>
<td>Poly</td>
<td>493</td>
<td>19.87</td>
<td>22.4</td>
</tr>
</tbody>
</table>

The calculated sheet resistances align well with the MOSIS-provided parametric data. Since interconnect resistance causes signal attenuation and $RC$ delay, interconnect used to route high-frequency signals should usually be kept as short and wide as layout constraints allow, and their effects on signal timing in high-speed digital logic must be modeled accurately.
Next, an experiment to measure and observe propagation delay, bandwidth, and integrity of high-frequency signals transmitted through the various on-chip interconnect was devised and performed. Figure 3.2 diagrams the experimental setup. The general methodology used in this experiment was to measure the voltage and timing offset of a generated pulse simultaneously at the input pin and output pin of a selected I/O pair internally interconnected within the test chip. While the primary goal in determining the experimental setup was to measure the pulse as close as possible to the I/O pins to isolate the contribution of the on-chip interconnect to the measured propagation delay, it was also critical to match source and load impedances and minimize parasitics throughout the signal path to minimize reflections, delay, and bandwidth limitations caused by the measurement system. For these reasons, the 20 GHz SD-24 sampling head with 50 Ω coaxial cabling was used with the Tektronix 11801A oscilloscope for this experiment instead of the 3 GHz SD-14 sampling head with 100 kΩ handheld probes. Although this setup required less precise jumpering to and from the test chip I/O pins, the parasitics of the SD-14’s handheld probe tips placed directly at the I/O pins were found to make accurate, undistorted measurements impossible. To minimize inaccuracies in the measured propagation delays due to skew between oscilloscope channels, the lengths of cables from the test chip to the two sampling head channel inputs were closely matched. A nominal 50 Ω environment was maintained from source to load. A direct coaxial cable connection from the pulse generator’s trigger output to the oscilloscope’s trigger input was used to provide the triggering source.

A 1 V\(_{\text{p-p}}\) signal amplitude was selected to meet the dynamic range requirements of the SD-24 sampling head. Due to voltage division between the ~60 Ω metal layer interconnect and the 50 Ω load termination, the actual voltage of the test signal measured at the output pin is about half of that measured at the input pin, as shown in Figure 3.3. However, to illustrate propagation
Figure 3.2: Interconnect Delay Experimental Setup
Figure 3.3: Test Pulse Voltage Levels  (a) Actual   (b) Scaled
delay and signal distortion more clearly, the amplitude scale (V/div) of the output pin channel was doubled so that the measured input and output voltages appeared equal.

Measurements were recorded for 15, 35, 40, 50, 60, 75, 90, 100, and 200 MHz square wave test signals generated with the Tektronix PG508 and HP 8133A pulse generators and transmitted through metal-1 (pins 1-18) and metal-3 (pins 22-37) on-chip interconnect. The waveforms captured across the metal-1 interconnect are shown in Figures 3.4 through 3.12, with the input pin signals in blue and the output pin signals in red. The metal-3 waveforms, which are nearly identical, are included in Appendix C. Table 3.3 below presents the time delays ($TD$) measured at the zero-crossing (50% transition) point across the metal-1 interconnect.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Time Delay ($TD$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 MHz</td>
<td>0.96 ns</td>
</tr>
<tr>
<td>35 MHz</td>
<td>0.74 ns</td>
</tr>
<tr>
<td>40 MHz</td>
<td>0.72 ns</td>
</tr>
<tr>
<td>50 MHz</td>
<td>0.72 ns</td>
</tr>
<tr>
<td>60 MHz</td>
<td>0.70 ns</td>
</tr>
<tr>
<td>75 MHz</td>
<td>0.64 ns</td>
</tr>
<tr>
<td>90 MHz</td>
<td>0.70 ns</td>
</tr>
<tr>
<td>100 MHz</td>
<td>0.70 ns</td>
</tr>
</tbody>
</table>

The experimental setup in Figure 3.2 shows that the difference in signal path length between the input pin and output pin measurement channels includes the length of the on-chip interconnect plus approximately 2.9 cm in jumper length. From the test chip layout, the length of the tested metal-1 interconnect is approximately 1.6 mm pad-to-pad. Assuming similar signal propagation velocities through the jumpers and the interconnect, the $TD$ at 100 MHz of the on-chip interconnect alone is approximately the proportion $(0.70 \text{ ns})(1.6 \text{ mm})/(1.6 \text{ mm} + 2.9 \text{ cm})$, or 36.6 ps. The measured propagation delay ($PD$) is then $(36.6 \text{ ps})(1.6 \text{ mm})$, or 22.9 ps/mm.
Figure 3.4: Metal-1 Interconnect 15 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure 3.5: Metal-1 Interconnect 35 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure 3.6: Metal-1 Interconnect 40 MHz Pulse   (a) Pulse Shape   (b) Rising Edge
Figure 3.7: Metal-1 Interconnect 50 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure 3.8: Metal-1 Interconnect 60 MHz Pulse  
(a) Pulse Shape  
(b) Rising Edge
Figure 3.9: Metal-1 Interconnect 75 MHz Pulse   (a) Pulse Shape   (b) Rising Edge
Figure 3.10: Metal-1 Interconnect 90 MHz Pulse   (a) Pulse Shape   (b) Rising Edge
Figure 3.11: Metal-1 Interconnect 100 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure 3.12: Metal-1 Interconnect 200 MHz Pulse
The measured PD of 22.9 ps/mm equates to a signal propagation velocity \( (v = 1/PD) \) of approximately 0.15 \( c \), where \( c \) is the speed of light in a vacuum \( (3 \times 10^8 \text{ m/s}) \). The electrical signal propagation velocity through an ideal lossless interconnect depends on the surrounding dielectric constant according to the relationship

\[
v = \frac{c}{\sqrt{\varepsilon_r}}
\]

(3.1)

where \( \varepsilon_r \) is the dielectric constant \([1]\). For a silicon dioxide (SiO\(_2\)) dielectric constant of 3.9 for on-chip interconnect, the ideal propagation velocity is approximately 0.5 \( c \). The differences between ideal and measured velocities are attributable to RC delay caused by lossy interconnect, discussed further in Chapter 4, and DUT socket parasitics.

In terms of signal integrity and bandwidth, the measurements indicate significant edge degradation, ringing, and noise, which become more pronounced at higher frequencies, also primarily due to socket parasitics on the DUT interface board. The fastest measured rising signal edges exhibited maximum slew rates of approximately 0.57 V/ns, equating to 10%-90% signal rise times of approximately 1.4 ns for a 1 V\(_{\text{p-p}}\) voltage transition. Applying Equation 2.8, a rise time of 1.4 ns corresponds to an analog bandwidth of approximately 250 MHz. This result is supported by the 200 MHz waveforms in Figure 3.12. At 200 MHz, the bandwidth-limited, lowpass-filtered square-wave signals become nearly sinusoidal, and rolloff attenuation is clearly evident in the waveform at the output pin. The fact that the input pin and output pin waveforms exhibit similar filtering indicates that the socket parasitics on the DUT interface board, not the on-chip interconnect under test, are the limiting factor for bandwidth performance.

Although these limitations prevent precise high-frequency characterization of on-chip interconnect, the measurement results clearly define the practical limitations for high-frequency CMOS chip testability with the best-possible experimental measurement environment defined in
Chapter 2. Specifically, the practical analog bandwidth within the measurement environment is \(\leq 250\) MHz, which, according to the “five times” rule of thumb discussed in Chapter 2, suggests that clock frequencies for digital circuits should be \(\leq 50\) MHz. However, based on the measured waveforms and depending on design sensitivity, performance may still be acceptable for clock frequencies of 100 MHz and higher.

3.3 Single-Ended Ring Oscillator Performance, Noise, and Jitter

An experimental methodology was developed to enable the measurement of the critical performance characteristics of high-frequency on-chip signal generators, including the oscillation frequency, noise, and timing jitter. Timing or clock jitter refers to cycle-to-cycle variations of the oscillation or clock period, while noise refers to random voltage aberrations in the oscillator waveform. A powerful feature of the Tektronix 11801A oscilloscope is its built-in noise and jitter measurement capability, enabled when the instrument is configured for Statistics Mode measurement calculations. The oscilloscope quantifies jitter as the root-mean-square (RMS) average variation of repetitive periodic signals across the x-axis (time scale). Similarly, it quantifies noise as the RMS average variation over the y-axis (amplitude scale). Statistics Mode is enabled on the 11801A oscilloscope by first enabling the color graded display mode, done by pressing the Display Modes menu button, touching Persist/Histogram at the bottom-left corner of the display, and touching Color Grading in the Persistence/Histogram pop-up menu, as outlined in Figure 3.13. Statistics Mode is then enabled by pressing the Measure menu button, touching Measurements at the bottom of the display, and touching Statistics Mode at the top of the Measurements pop-up menu, as shown in Figure 3.14. The Jitter and Noise measurement options, disabled under the default Software Mode, are then enabled and will return accurate results after several seconds of signal acquisition.
Figure 3.13: Tektronix 11801A Oscilloscope Color Grading Display Mode
Figure 3.14: Tektronix 11801A Oscilloscope Statistics Mode
Since the 11801A oscilloscope requires an external triggering source synchronized with the measured periodic signal, the output of on-chip signal sources must be split and connected to both the oscilloscope trigger input and the sampling head channel input as shown in Figure 3.15 for both SD-14 (handheld probe) and SD-24 (coaxial cabling) sampling head configurations. It is important to ensure that the amplitude of the on-chip generated signal does not exceed the maximum safe input voltage specifications of both the trigger input and the sampling head input.

To test this experimental methodology, and to obtain experimental performance data for a practical ring oscillator designed as discussed in Chapter 5, an existing 1.2 µm CMOS test chip containing a 27-stage single-ended ring oscillator was obtained and tested. To safely measure the ring oscillator’s 5 V_{p-p} amplitude range, the SD-14 sampling head’s 100 kΩ handheld probe was used for signal acquisition, and X10 attenuation was enabled on the 11801A’s trigger input by pressing the Trigger menu button and touching External Attenuate at the bottom of the display. The ring oscillator output waveform captured with the LabVIEW/MATLAB acquisition system is shown in Figure 3.16, while a screenshot of the color-graded output on the 11801A used for noise and jitter measurements is shown in Figure 3.17 (the LabVIEW/MATLAB system cannot store color-graded persistence). Table 3.4 below summarizes the results of experimental measurements. The 11801A oscilloscope was found to be capable of picosecond (ps) and microvolt (µV) resolution for jitter and noise measurements, respectively.

Table 3.4: 1.2 µm Single-Ended Ring Oscillator Measurement Results

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude</td>
<td>5.0 V_{p-p}</td>
</tr>
<tr>
<td>Frequency</td>
<td>44.05 MHz</td>
</tr>
<tr>
<td>Rise Time</td>
<td>6.8 ns</td>
</tr>
<tr>
<td>RMS Noise</td>
<td>43.178 mV</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>166.94 ps</td>
</tr>
</tbody>
</table>
Figure 3.15: On-Chip Generated Signal Measurement Setup  (a) SD-14  (b) SD-24
Figure 3.16: 1.2 \( \mu \text{m} \) Single-Ended Ring Oscillator Output Waveform

1.2 um Single-Ended Ring Oscillator @ VDD = 5 V

Amplitude (Vcts)

Time (Nanoseconds)
Figure 3.17: 1.2 µm Single-Ended Ring Oscillator Output Color-Graded Waveform
3.4 Time-Domain Reflectometry (TDR) Testing

Additional experimental testing was performed to evaluate the SD-24 sampling head’s time-domain reflectometry (TDR) measurement capabilities. Time-domain reflectometry is a testing technique used to identify, measure, and calculate impedance discontinuities, propagation velocities, and characteristic impedances of interconnect transmission lines. TDR measurements involve driving step function signals into the interconnect network under test and measuring the reflections transmitted back to the driver against a standard reference impedance. According to transmission line theory, energy transmitted through any impedance discontinuity will result in energy being reflected back, the magnitude of which is a function of both the transmitted energy and the magnitude of the impedance discontinuity. The time delay between transmitted and reflected energy is a function of transmission line length and signal propagation velocity [1]. Impedances can be calculated from the measured reflection profile using the formula

\[ Z = Z_o \frac{1 + \rho}{1 - \rho} \]  

(3.2)

where \( Z_o \) is the known reference output impedance of the TDR driver (in this case, the 11801A oscilloscope’s SD-24 sampling head), \( \rho \) is the reflection coefficient equal to

\[ \rho = \frac{V_{\text{reflected}}}{V_{\text{incident}}} = \frac{Z - Z_o}{Z + Z_o} \]  

(3.3)

and \( Z \) is the impedance of the interconnect under test [1]. Low-impedance voltage droops in the reflection profile indicate capacitive loading discontinuities, while high-impedance voltage peaks indicate inductive loading discontinuities [1]. TDR techniques are used to test both terminated interconnect (to validate driver/load impedance matching along a signal path, with ideally zero reflected energy, i.e. \( \rho = 0 \)) and single-ended open interconnect (to measure interconnect length, propagation velocity, and signal integrity and to calibrate timing measurements, with ideally all
transmitted energy reflected back, i.e. $\rho = 1$). Although typically used to measure printed circuit board (PCB) trace characteristic impedances, TDR experimental measurements were collected to identify the sources of impedance discontinuities and parasitics in the DUT interface hardware used for high-frequency measurements.

TDR measurements are enabled on the 11801A oscilloscope with the SD-24 sampling head installed by pressing the Waveform menu button, touching Sampling Head Fnc’s in the bottom-left corner of the display, touching TDR/TDT in the Head Type: SD-24 box in the Sampling Head Functions pop-up menu, and touching TDR Preset in the same menu, as shown in Figure 3.18. To select the unit of the x-axis in the reflection profile to measure propagation velocity (seconds) or interconnect/cable length (meters, feet, or inches), touch Graticules at the bottom of the display and then touch the desired unit under X Units in the Graticules pop-up menu, as shown in Figure 3.19. When a unit of length is selected, the oscilloscope calculates the x-axis scale using the Propagation Velocity (coefficient of $c$) setting in the Graticules pop-up menu, which must be set to the known or assumed $v$ of the interconnect under test.

Experimental TDR measurements of the lengths and propagation velocities of coaxial cabling used in the DUT interface were first collected. Two pairs of low-capacitance SMA coaxial cables of known lengths were used: Tektronix part numbers 174-1428-00 (60 inches) and 174-1120-00 (8.5 inches). The reflection profile of the 60-inch cable with one end connected to the SD-24 sampling head, shown in Figure 3.20, illustrates the reflection of the TDR pulse from the open end of the cable back to the sampling head. As expected, the reflection profile is nearly ideal (i.e. sharp edges with minimal aberrations) since the cable’s nominal 50 $\Omega$ impedance is consistent throughout the length of cable and matches the 50 $\Omega$ impedance of the sampling head, and cable parasitics are small. Cable length and propagation time/velocity are determined from
Figure 3.18: Tektronix 11801A Oscilloscope TDR Activation
Figure 3.19: Tektronix 11801A Oscilloscope TDR Unit Selection
Figure 3.20: SMA Cable Reflection Profile
the length of the profile’s “shelf” along the x-axis (bounded by vertical cursor bars in Figure 3.20) divided in half, since the shelf represents the round-trip path of the TDR pulse from the sampling head to the end of the cable and back. Table 3.5 below summarizes the measurement and calculation results of cable length, propagation delay and velocity, and dielectric constant (from Equation 3.1).

<table>
<thead>
<tr>
<th>Cable Part #</th>
<th>Nominal Length</th>
<th>TDR Length (assumed ( v = 0.7 , c ))</th>
<th>Propagation Velocity (Actual)</th>
<th>Propagation Delay (Actual)</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>174-1428-00</td>
<td>60.0 in.</td>
<td>66.1 in.</td>
<td>0.64 ( c )</td>
<td>52.1 ps/cm</td>
<td>2.4</td>
</tr>
<tr>
<td>174-1120-00</td>
<td>8.5 in.</td>
<td>10.7 in.</td>
<td>0.56 ( c )</td>
<td>59.6 ps/cm</td>
<td>3.2</td>
</tr>
</tbody>
</table>

Next, experimental TDR measurements of the DUT interface hardware and on-chip interconnect were collected to identify the influence of each hardware component on the overall high-frequency measurement bandwidth and signal integrity limitations. Figure 3.20 previously illustrated the reflection profile of the SMA coaxial cable prior to connection to the DUT board. Figure 3.21 shows the reflection profile with the cable connected to an SMA connector on the DUT interface board, extending the open end of the signal path to the socket tied to the SMA connector as shown in Figures 2.4-2.5. The path to this point is still free of major impedance discontinuities, since the 50 \( \Omega \) TDR driver, cable, and connector are properly matched. The connection of a 2 cm shielded jumper to the socket introduces an inductive discontinuity as suggested by the peak/overshoot in the reflection profile shown in Figure 3.22. With the open end of the jumper then connected to the empty DUT socket, the resultant reflection profile shown in Figure 3.23 indicates the introduction of parasitic capacitance into the signal path. Finally, with the interconnect test chip inserted into the DUT socket, extending the signal path through a metal-1 on-chip interconnect to an open output pin, the reflection profile shown in Figure 3.24
Figure 3.21: Path Through SMA Connector  (a) Connection  (b) Reflection Profile
Figure 3.22: Path Through Socket Jumper  
(a) Connection  
(b) Reflection Profile
Figure 3.23: Path Through DUT Socket Reflection Profile
Figure 3.24: Path Through On-Chip Interconnect  (a) Connection  (b) Reflection Profile
illustrates the complex series of impedance variations encountered in the DUT interface affecting high-frequency signal integrity, bandwidth, and settling time.

Finally, experimental TDR measurements of the existing BNC-based DUT interface box, previously evaluated and found to be severely bandwidth-limited as discussed in Section 2.3, were collected to compare its characteristics to those of the SMA-based high-frequency DUT interface board. The reflection profile shown in Figure 3.25 for a BNC coaxial cable prior to connection to the interface box suggests negligible differences between standalone BNC and SMA cabling performance. However, with the BNC cable connected to a BNC connector on the interface box, extending the signal path through internal wiring directly to the DUT socket, the reflection profile shown in Figure 3.26 clearly shows major capacitive and inductive parasitic impedances responsible for the limited analog bandwidth of the box. Comparing Figures 3.23 and 3.26, which show the reflection profiles of the signal paths to the DUT sockets of the high-frequency SMA interface board and the existing BNC box, respectively, the newly designed and constructed SMA-based board clearly provides a cleaner interface between test equipment and the DUT, resulting in a 25x improvement in analog bandwidth.
Figure 3.25: BNC Cable Reflection Profile
Figure 3.26: Path Through BNC Connector  (a) Connection  (b) Reflection Profile
Chapter 4

On-Chip Interconnect Modeling and Simulation Techniques

4.1 Overview

To simulate and verify the results of the on-chip interconnect impedance and propagation delay measurements presented in Chapter 3, basic equivalent-circuit interconnect models were developed. Physical modeling techniques and SPICE implementations were also examined. The models can be incorporated into full-chip SPICE simulations of high-frequency, mixed-signal integrated circuit designs for more accurate analysis of signal integrity and timing specifications.

Although the physical characteristics, parasitics, and interactions of on-chip interconnect can typically be neglected in simple, low-frequency digital CMOS VLSI designs, these elements significantly impact the functionality and performance of complex, high-speed digital integrated circuits. Each non-ideal conductive path introduces resistance, capacitance, and inductance into the circuit design. Furthermore, at high frequencies, these interconnect parasitics behave not as discrete lumped circuit elements but rather as a series of smaller elements distributed over the length of the interconnect. Under such conditions, on-chip interconnect can no longer be considered ideal conductors or lumped elements, but instead must be modeled as transmission lines. This becomes necessary when the physical length of the interconnect approaches the wavelength of the highest frequency component in signals transmitted over the interconnect [1].

As discussed in Chapter 2, the rise time or edge rate of a digital signal determines the maximum frequency component present in the signal, approximated according to Equation 2.8. The length a digital signal with a fixed edge rate travels during a transition through an ideal, lossless on-chip interconnect depends on the signal propagation velocity through the surrounding dielectric, given by Equation 3.1. As stated in Chapter 3, the on-chip signal propagation velocity along a lossless
interconnect through silicon dioxide dielectric material is approximately 0.5 \( c \). As a general rule, an interconnect of a length greater than or equal to \( 1/10 \)th of the length traveled by a digital signal during an edge transition will exhibit transmission line behavior and must be modeled as such for signal integrity and timing accuracy [1]. Thus, for example, a 1 GHz digital clock signal with a fifth harmonic frequency component of 5 GHz (as discussed in Chapter 2), equivalent to a rise time of 70 ps, travels approximately

\[
(0.5c)(70 \times 10^{-12}) \approx 1 \text{ cm}
\]
during an edge transition, and any on-chip interconnect of length \( \geq 1/10 \) cm (1 mm) carrying this signal must be modeled as a transmission line.

While signal propagation velocity places a lower bound on interconnect delay relatively independent of frequency, practical lossy on-chip interconnect introduce \( RC \) and \( RLC \) delay that limits analog bandwidth and increases effective digital signal transition times. Each distributed segment of an interconnect transmission line propagating in transverse electromagnetic (TEM) mode is modeled as an \( RLCG \) (resistance, inductance, capacitance, conductance) circuit, as shown in Figure 4.1 [1]. Interconnect resistance, dependent primarily only on metal conductor resistivity (\( \rho \)) and dimensions, is given by

\[
R = \frac{\rho L}{A} = \frac{\rho}{t} \frac{L}{W} = R_\square \frac{L}{W}
\]

where \( A \) is the conductor cross-sectional area, \( L \) is the length, \( W \) is the width, \( t \) is the thickness, and \( R_\square \) is the sheet resistance [1]. The capacitance of a given interconnect segment, however, is layout-dependent and consists of several components, including line-to-ground capacitance and line-to-line coupling capacitance [15]. Nevertheless, since interconnect parasitic capacitances are limited to short-range, nearest-neighbor electric field interactions, they can be calculated deterministically for a given layout. On the other hand, interconnect parasitic inductances are
Figure 4.1: Distributed Interconnect Segment *RLCG* Equivalent Circuit Model
dependent on long-range magnetic field interactions with multiple neighboring and distant lines, and determining current loops and return paths for accurate inductance modeling is significantly more challenging [16]. Interconnect conductance can typically be neglected [1].

The parasitic resistances, capacitances, and inductances of lossy interconnect relate to signal propagation and \( RLC \) delay according to the Telegrapher’s equation [17]

\[
\frac{\partial^2 V}{\partial x^2} = RC \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2}
\] (4.2)

where \( x \) is the interconnect length, \( t \) is time, and \( V \) is signal voltage [17]. Intuitively, the \( RC \) term is dominant at low frequencies, causing signals to propagate slowly by diffusion, increasing delay and limiting bandwidth. At multi-GHz frequencies, however, interconnect inductance dominates resistance, causing the interconnect to propagate signals as a waveguide [17]. Though analog bandwidth increases, parasitic inductances also cause delay, crosstalk, power grid noise, overshoot, and other signal integrity problems [18].

On-chip interconnect delay and other parasitic effects become more pronounced as chip feature sizes shrink. Process technology improvements and feature size reductions decrease the intrinsic MOSFET switching delay, improving performance; however, since interconnect widths and thicknesses decrease, increasing resistance per unit length, while capacitance remains fairly constant, on-chip interconnect \( RC \) delay actually increases for a given length. Table 4.1 on the next page summarizes the 1999 International Technology Roadmap for Semiconductors (ITRS) projections for typical MOSFET and interconnect delays in present and future deep submicron process generations, clearly predicting that traditional metal layer interconnect limitations will surpass transistor performance as the dominant cause of signal path latency [19]. Furthermore, as clock frequencies, circuit densities, and the number of metal interconnect layers all increase, signal integrity problems due to capacitive and inductive crosstalk between random signal lines
increase exponentially. Although process material improvements such as lower-resistivity copper (instead of aluminum) metal layers and low-K dielectrics will improve performance, modeling on-chip interconnect parasitics will be critical for accurate design simulations.

Table 4.1: Submicron Technology MOSFET and Interconnect Delay Projections

<table>
<thead>
<tr>
<th></th>
<th>1.0 µm</th>
<th>100 nm</th>
<th>35 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET Switching Delay (ps)</td>
<td>~20</td>
<td>~5</td>
<td>~2.5</td>
</tr>
<tr>
<td>(L = 1 mm) Interconnect RC Delay (ps)</td>
<td>~1</td>
<td>~30</td>
<td>~250</td>
</tr>
</tbody>
</table>

Accurate layout extraction and high-frequency modeling of lossy on-chip interconnect parasitic inductances and capacitances can be a complex and computationally intensive process. To model effective interconnect inductances without a priori predetermination of current loops and return paths, most current analysis methodologies rely on the Partial Element Equivalent Circuit (PEEC) method, in which partial self and mutual inductances are defined for each individual segment of the distributed transmission line interconnect model [18]. The resistance and self and mutual capacitances of each segment are incorporated into the PEEC model to form a complete RLC model for SPICE simulation. Electrostatic (2D) or full-wave (3D) field solvers, which solve Maxwell’s equations for electromagnetic interactions in arbitrary geometries, are used for accurate calculation of these inductances and capacitances from geometric descriptions of physical circuit layouts [1]. However, these tools are often very difficult to use and require extensive processing time (hours or days) for complete parasitic extraction from complex circuit layouts [1]. Also, the resultant dense RLC circuit matrices obtained from field solvers require extremely long SPICE processing times and require sparsification (simplification or elimination of negligible terms) to improve simulation efficiency.

A literature review of current research in high-frequency on-chip interconnect modeling and simulation was first conducted. Several recent publications, such as [16], propose optimized
methods for calculating partial inductances for \( RLC \) interconnect models valid up to 100 GHz. Others, such as [17], propose design techniques for exploiting on-chip interconnect inductances to improve high-frequency signal propagation. However, little documentation was found on the implementation of on-chip interconnect models in SPICE. The bandwidth of the measurement environment evaluated in Chapter 2 was insufficient for experimental verification of the high-frequency inductance models proposed in [16] and others. Also, costly commercial field solvers and physical layout modeling tools were unavailable for research. Therefore, the following work focuses on the basic physical modeling of the test chip interconnect described in Chapter 3, the comparison of theoretical and experimental interconnect impedance and delay results, and the implementation and simulation of equivalent circuit models in Cadence PSpice 10.0.

### 4.2 Physical Interconnect Model – FastCap and FastHenry

Recalling the experimental results from Chapter 3, the tested metal-1 (aluminum) layer interconnect exhibited a propagation delay \((PD)\) of 22.9 ps/mm, a propagation velocity \((v)\) of 0.15 \(c\), and a sheet resistance of 0.09 \(\Omega/\square\). The width \((W)\) of each interconnect was 1.8 \(\mu\)m from the layout file, but the layer thickness was unknown. From Equation 4.1, with \(\rho = 2.7\times10^{-8} \Omega\cdot m\) for aluminum, the approximate layer thickness is calculated to be

\[
t = \frac{\rho}{R_w} = \frac{2.7\times10^{-8} \Omega\cdot m}{0.09 \Omega/\square} = 0.3 \mu m
\]

and the resistance of a 1 mm interconnect segment is

\[
R = R_w \frac{L}{W} = (0.09 \Omega/\square) \frac{1\times10^{-3} m}{1.8\times10^{-6} m} = 50 \Omega.
\]

To calculate the effective capacitance and inductance of the 1 mm interconnect segment, two powerful, free 3D field solver tools developed at M.I.T., FastCap and FastHenry, were used. FastCap is a 3D capacitance extraction program that computes self and mutual capacitances for
ideal conductors of arbitrary shape, orientation, and size, embedded in arbitrary dielectric regions [20]. The input to this program is a manually-generated 3D geometric description of the system of conductors, each defined as a set of adjoining rectangular panels. Each panel is specified with a conductor number followed by the \([x \ y \ z]\) coordinates of the vertices of the panel, in the form:

\[
Q \ 1 \ 0.0 \ 0.0 \ 0.0 \ 1.0 \ 0.0 \ 0.0 \ 1.0 \ 1.0 \ 0.0 \ 0.0 \ 1.0 \ 0.0
\]

To increase extraction accuracy and speed, long or complex conductors must be discretized into multiple smaller uniform segments. The output of the program is a standard capacitance matrix \(C\), in which \(C_{NN}\) is the total capacitance seen by line \(N\), and \(C_{MN}\) is the mutual capacitance between lines \(M\) and \(N\) [1].

Three parallel metal-1 layer interconnect segments in the test chip, shown in Figure 4.2 from the layout file, with \(L = 1.0\) mm, \(W = 1.8\) µm, \(t = 0.3\) µm, and 0.9 µm line spacing, were modeled for capacitance extraction in FastCap. Each conductor was discretized into ten 0.1 mm segments. Figure 4.3 shows a 3D model of the parallel conductors generated from the input file by the FastModel viewer packaged with FastCap and FastHenry. For a silicon dioxide dielectric \((\varepsilon_r = 3.9)\), the following capacitance matrix was found:

\[
C = \begin{pmatrix}
88.5 & -57.31 & -17.38 \\
-57.31 & 123 & -57.22 \\
-17.38 & -57.22 & 88.77
\end{pmatrix} \times 10^{-15} \text{ F}
\]

FastHenry is a 3D inductance extraction program that computes frequency-dependent self and mutual inductances and resistances of conductors of arbitrary shape and conductance [21]. Instead of rectangular panels, conductor geometries are defined as linear segments connecting end point nodes. Nodes and segments are defined in the input file in the general form:

\[
\begin{align*}
N1 & \ x=0 \ y=0 \ z=0 \\
N2 & \ x=1 \ y=0 \ z=0 \\
E1 N1 N2 & \ w=0.2 \ h=0.1
\end{align*}
\]
Figure 4.2: Metal-1 Parallel Interconnect Layout
Figure 4.3: Metal-1 Parallel Interconnect 3D Model
which defines the [x y z] coordinates of two nodes, \( N1 \) and \( N2 \), and then defines a segment from \( N1 \) to \( N2 \) with a rectangular cross-section defined by \( w \) and \( h \). Each segment can be discretized non-uniformly to model skin effects at high frequencies. The output of the program is a standard complex impedance \((R + jL)\) matrix \( Z \), in which \( Z_{NN} \) is the resistance and self inductance of line \( N \), and \( Z_{MN} \) is the resistance and mutual inductance between lines \( M \) and \( N \).

An equivalent FastHenry-compatible model of the same three parallel interconnect lines with a conductivity \((\sigma = 1/\rho)\) of \( 3.7 \times 10^{-7} \, \Omega^{-1}/\text{m} \) was created for inductance extraction. Impedance matrices were computed for \( f = 100 \, \text{MHz} \) and \( f = 1 \, \text{GHz} \), though inductances were identical at both frequencies. The following \( f = 100 \, \text{MHz} \) impedance matrix was found:

\[
Z = \begin{pmatrix}
50.05 + 1.47 \times 10^{-9} & 0 + 1.13 \times 10^{-9} & -1.04 \times 10^{-17} + 9.86 \times 10^{-10} \\
-1.73 \times 10^{-18} + 1.13 \times 10^{-9} & 50.05 + 1.47 \times 10^{-9} & 0 + 1.13 \times 10^{-9} \\
-6.94 \times 10^{-18} + 9.86 \times 10^{-10} & 3.47 \times 10^{-18} + 1.13 \times 10^{-9} & 50.05 + 1.47 \times 10^{-9}
\end{pmatrix}
\]

The FastCap and FastHenry input files are presented in Appendix D.

The \( N = 1 \) conductor in the above matrices corresponds to the experimentally tested metal-1 interconnect. The \( RLC \) model derived from the field solver results for this conductor has \( R = 50.05 \, \Omega \), \( C = 88.5 \, \text{fF} \), and \( L = 1.47 \, \text{nH per 1 mm segment} \). The \( 50 \, \Omega \) resistance calculated from the FastHenry model precisely matches the value of \( R \) previously calculated using the experimentally determined sheet resistance. The time delay across an ideal 1 mm interconnect (neglecting resistance and \( RC \) delay) is given by

\[
TD = \sqrt{LC}
\]

which for the above \( L \) and \( C \) values yields

\[
TD = \sqrt{(1.47 \times 10^{-9} \, \text{H})(88.5 \times 10^{-15} \, \text{F})} = 11.4 \, \text{ps}
\]

equal to a propagation delay \( PD = 11.4 \, \text{ps/mm} \) and a propagation velocity \( v = 1/\text{PD} = 0.29 \, c \).
This value is less than the theoretical maximum propagation velocity in silicon dioxide (~ 0.5 \( c \)) because the conductor was modeled with a non-ideal conductivity, but it is greater than the experimentally determined value of 0.15 \( c \) because the measured time delay used to calculate this value included \( RC \) delay.

The final parameter of interest, useful for SPICE implementation, is the characteristic impedance \((Z_o)\) of the 1 mm interconnect segment. The complete frequency-dependent equation for characteristic impedance is

\[
Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{4.4}
\]

where \( R, L, C, \) and \( G \) are per unit length values and \( \omega = 2\pi f [1] \). For ideal lossless interconnect (neglecting resistance), or for lossy interconnect at multi-GHz frequencies at which \( L \) dominates \( R \), this expression simplifies to

\[
Z_o = \sqrt{\frac{L}{C}} \tag{4.5}
\]

which is essentially frequency-independent. For lossy interconnect at lower frequencies, though, resistance cannot be neglected, as the characteristic impedance becomes approximately

\[
Z_o = \sqrt{\frac{R}{j\omega C}} \tag{4.6}
\]

which is highly frequency-dependent and generally much larger than the \( Z_o \) value calculated with Equation 4.5. For the \( RLC \) values from the field solver results (neglecting \( G \)),

\[
Z_{o \text{ ideal}} = \sqrt{\frac{L}{C}} = \sqrt{\frac{1.47 \times 10^{-9} \text{ H}}{88.5 \times 10^{-15} \text{ C}}} = 129 \Omega
\]

\[
Z_{o \ 1 \text{ MHz}} = \sqrt{\frac{50 + j2\pi(10^6)(1.47 \times 10^{-9})}{j2\pi(10^6)(88.5 \times 10^{-15})}} = 9482 \Omega
\]
These results clearly highlight the frequency dependence in accurately modeling characteristic impedance for SPICE on-chip interconnect transmission line simulation.

4.3 Equivalent Circuit Model and SPICE Implementations

From the calculated $R$, $L$, $C$, $\nu$, $Z_o$, and $PD$ values, on-chip interconnect equivalent circuit models can be formed and implemented in SPICE. Basic equivalent distributed circuit models consist of multiple RLC segments (neglecting $G$), previously shown in Figure 4.1, in series. Recalling the rule that any interconnect $\geq 1/10^{th}$ the length traveled by the highest frequency component of a digital signal during an edge transition will exhibit transmission line effects, the minimum number of segments required for accurate simulation is

\[
\text{segments} \geq 10 \left( \frac{X}{T_e \nu} \right) \quad (4.7)
\]

where $X$ is the interconnect length, $T_e$ is the edge rate of the highest frequency component in the signal, and $\nu$ is the propagation velocity [1]. Thus, for example, a 1 GHz clock frequency with a fifth harmonic 5 GHz bandwidth requirement transmitted across the 1 mm interconnect with the previously calculated propagation velocity of 0.29 $c$ would require

\[
\text{segments} \geq 10 \left( \frac{10^{-3}}{(7 \times 10^{11}) (0.29 \times 3 \times 10^8)} \right) = 1.64 \rightarrow 2
\]

in the model for accurate simulation. The values of $R$, $L$, and $C$ per segment are simply:
\[ R_{\text{segment}} = \frac{R_{\text{total}}}{\text{segments}} \]  
\[ L_{\text{segment}} = \frac{L_{\text{total}}}{\text{segments}} \]  
\[ C_{\text{segment}} = \frac{C_{\text{total}}}{\text{segments}} \]  

where \( R_{\text{total}}, L_{\text{total}}, \) and \( C_{\text{total}} \) are the values from the field solver results over the full length of the interconnect [1]. If the length of an interconnect is doubled while its cross-sectional area and line spacing is constant, its \( R_{\text{total}} \) and \( C_{\text{total}} \) are effectively doubled, and the known values from the shorter interconnect can be used to generate a new equivalent circuit. However, \( L_{\text{total}} \) increases nonlinearly with parallel interconnect length, so the field solver model must be edited and rerun.

To implement on-chip interconnect distributed equivalent circuit models in SPICE, the only stable and accurate method found was to manually define each discrete \( R, L, \) and \( C \) element in every segment. A complete segment is defined using the syntax and node connections:

\[
\begin{align*}
&\text{R <name> N1 N2 <value>} \\
&\text{L<name> N2 N3 <value>} \\
&\text{C<name> N3 0 <value>}
\end{align*}
\]

Defining multiple segments with this method can be tedious and error-prone. Attempts were made to implement the equivalent circuit models using the built-in transmission line elements in Cadence PSpice 10.0, which include both a lossless model, defined in the general form

\[
\begin{align*}
&\text{T <name> <A port (+) node> <A port (-) node> } \\
&\quad + \text{<B port (+) node> <B port (-) node>} \\
&\quad + \text{ZO=<value> TD=<value>}
\end{align*}
\]

where \( A \) and \( B \) are the input and output ports, \( TD \) is the time delay, and \( ZO \) is the characteristic impedance of the line [22]; and a lossy model, defined in the general form

\[
\begin{align*}
&\text{T <name> <A port (+) node> <A port (-) node> } \\
&\quad + \text{<B port (+) node> <B port (-) node>} \\
&\quad + \text{LEN=<value> R=<value> L=<value>} \\
&\quad + \text{G=<value> C=<value>}
\end{align*}
\]
where \( \text{LEN} \) is the interconnect length and \( R, L, G, \) and \( C \) are per-\( \text{LEN} \) values [22]. This lossy model automatically distributes the per-length \( RLC \) values continuously over the line length, eliminating the need to manually calculate the frequency-specific number of required segments and define extensive netlists of discrete components [22]. Unfortunately, the simulation results from these models were unstable due to the inaccuracies of the built-in transmission line models with large \( R/L \) ratios and extremely small time delays. Therefore, use of the built-in models must be limited to board-level and cabling interconnect models.

### 4.4 Example Simulation Results

Using the derived on-chip interconnect equivalent circuit models, SPICE simulations to model the interconnect delay measurement experiment from Chapter 3 as well as gate-to-gate interconnect delay in high-frequency designs were performed. First, the 1.6 mm metal-1 layer test chip interconnect was modeled using the \( R_{\text{total}} \) measured experimentally for the interconnect plus the \( LC \) values calculated above for the 1 mm conductor, divided proportionally into three segments with \( R_{\text{segment}} = 18.8 \, \Omega, L_{\text{segment}} = 0.735 \, \text{nH}, \) and \( C_{\text{segment}} = 0.4425 \, \text{fF} \). The setup shown in Figure 3.2 was simulated with a 100 MHz pulse signal, lossless transmission line models for the 2.5 cm shielded jumpers, and a 50 \( \Omega \) oscilloscope sampling head input impedance. Figure 4.4 shows the simulated pulse waveforms at the input (in blue) and output (in red) connectors of the DUT interface board as measured in Chapter 3. These waveforms exhibit the same general delay, input overshoot, and output undershoot characteristics as the experimentally measured 100 MHz waveforms shown in Figure 3.11.

Next, to illustrate the effects of on-chip interconnect propagation and \( RC \) delay on gate-to-gate timing in high-speed digital circuit designs, a long 5 mm clock distribution interconnect between two CMOS inverters was modeled and incorporated into circuit simulations. The \( RC \)
Figure 4.4: Test Chip Interconnect Delay Simulation
values calculated for the 1 mm conductor model were multiplied by five to find $R_{\text{total}} = 250 \ \Omega$
and $C_{\text{total}} = 0.4425 \ \text{pF}$ for the 5 mm conductor. FastHenry was used to calculate $L_{\text{total}} = 8.97 \ \text{nH}$.
For a maximum clock frequency of 1 GHz, the number of distributed segments required in the
equivalent circuit model is calculated as:

$$BW = 5 \times f = 5 \times 10^9 \ \text{Hz}$$

$$T_r = \frac{0.35}{BW} = \frac{0.35}{5 \times 10^9} = 70 \ \text{ps}$$

$$PD = \frac{\sqrt{LC}}{X} = \frac{\sqrt{(8.97 \times 10^{-9} \ \text{H})(4.425 \times 10^{-13} \ \text{F})}}{5 \times 10^{-3} \ \text{m}} = 12.6 \ \text{ns/m}$$

$$v = \frac{1}{PD} \approx 0.26 \ c$$

$$\text{segments} \geq 10 \left( \frac{X}{T_r v} \right) = 10 \left( \frac{5 \times 10^{-3} \ \text{m}}{(7 \times 10^{-11} \ \text{s})(0.26 \times 3 \times 10^8 \ \text{m/s})} \right) = 9.16 \rightarrow 10.$$ 

For 10 uniform $RLC$ segments, the per-segment element values are then $R_{\text{segment}} = 25 \ \Omega$, $L_{\text{segment}} = 0.897 \ \text{nH}$, and $C_{\text{segment}} = 44.25 \ \text{fF}$. A CMOS inverter layout with fast-switching, wide-channel
nMOS and pMOS devices ($W/L = 20.1/0.6 \ \mu\text{m}$) was created using the MOSIS scalable CMOS
submicron (SCmos_SUBM) design rules for the AMIS C5F/N 0.5 \ \mu\text{m} process and simulated
using typical-corner SPICE BSIM3v3 model parameters provided by MOSIS [23]. Figure 4.5
shows a diagram of the complete circuit, which was simulated for clock frequencies of 500 MHz
(140 ps edge rate) and 1 GHz (70 ps edge rate). Figure 4.6 shows the voltage transition at the
gate of the second inverter (in red) for an ideal step input to the gate of the first inverter (in blue)
with (a) an ideal zero-delay interconnect (common SPICE netlist node) and (b) the ten-segment
equivalent circuit model connecting the two devices. For the ideal case seen in Figure 4.6 (a),
the second inverter sees the voltage transition instantaneously, indicating zero propagation delay,
Figure 4.5: Gate-To-Gate Delay Simulation Circuit Diagram
Figure 4.6: Voltage Transition Delay  (a) Ideal Model  (b) Equivalent Circuit Model
while the 120 ps overall transition delay at $V_{DD}/2 = 2.5$ V is due exclusively to the intrinsic switching delay of the first inverter. For the equivalent circuit model case seen in Figure 4.6 (b), there is an initial 60 ps propagation delay as predicted from the $PD$ value calculated previously:

$$X \cdot PD = (5 \times 10^{-3} \text{ m})(12.6 \text{ ns/m}) = 63 \text{ ps}.$$ 

The larger 380 ps overall transition delay at $V_{DD}/2$ is a combination of the propagation delay, inverter switching delay, and the $RC$ delay of the interconnect.

Figures 4.7 and 4.8 show the voltage waveform at the input of the first inverter (in blue) and the input and output of the second inverter (in red), respectively, for (a) an ideal zero-delay interconnect and (b) the ten-segment equivalent circuit model at a clock frequency of 500 MHz. Figures 4.9 and 4.10 show the same waveforms at a higher clock frequency of 1 GHz. Timing delay imposed by the long clock distribution line is evident at both frequencies. Furthermore, at 1 GHz, the bandwidth and edge rate limitations imposed by the distributed $RLC$ parasitics nearly causes the waveform at the input of the second inverter to fail to reach the $V_{DD}/2$ threshold, as seen in Figure 4.9 (b). Clearly, accurate modeling of on-chip interconnect and clock distribution lines is critical for simulating both timing and functionality of complex high-speed digital circuit designs. The physical and equivalent circuit modeling techniques presented here align well with theoretical and experimental interconnect characterization.

The SPICE netlists and input files for these simulations are presented in Appendix E.
Figure 4.7: 500 MHz Input-Input Delay  
(a) Ideal Model   (b) Equivalent Circuit Model
Figure 4.8: 500 MHz Input-Output Delay   (a) Ideal Model   (b) Equivalent Circuit Model
Figure 4.9: 1 GHz Input-Input Delay  
(a) Ideal Model   (b) Equivalent Circuit Model
Figure 4.10: 1 GHz Input-Output Delay  (a) Ideal Model   (b) Equivalent Circuit Model
Chapter 5

Ring Oscillator Designs and Simulation Techniques

5.1 Overview

In addition to the evaluation and modeling of the performance and parasitic effects of the instrumentation, interface hardware, and global and on-chip interconnect used to transmit and measure high-frequency signals, the design and behavior of circuit devices used for on-chip high-frequency signal and clock generation were also studied. Two particular CMOS structures were examined: the single-ended ring oscillator, comprised of a series of cascaded standard complementary inverters; and the differential ring oscillator, comprised of a series of cascaded differential inverters. Each design has advantages and disadvantages in terms of output performance, footprint, power dissipation, jitter, and noise sensitivity. Device characteristics are highly dependent on process technology, feature sizes, supply voltage, and other design criteria.

Example designs and layouts of each structure were completed and simulated in SPICE using AMI Semiconductor (AMIS) 0.5 µm (λ = 0.3 µm) Scalable CMOS Submicron (SCMOS_SUBM) process design rules for the MOSIS foundry. The intended application of these designs was their inclusion into future voltage-controlled oscillator (VCO) and phase-locked loop (PLL) device designs and layouts.

5.2 Layout and Simulation Tools and Methods

The layouts and SPICE simulations were completed and executed using the Tanner EDA L-Edit Pro v8.3/v10.2 and Cadence PSD v15.0 (PSpice v10.0 with BSIM3v3.2 MOSFET SPICE model support) software packages for Windows, respectively. Layout-to-netlist extraction was performed using the Tanner Tools Setups for MOSIS AMI (0.5 µm) Submicron Process Revision 1.0 package. It is important to note that, in the default Extract definition file for this
package (mAMIs05.ext), for the Drain and Source entries under the nMOS and pMOS transistor definitions, the “WIDTH” arguments must be changed to “AREA, PERIMETER” to enable extraction of the drain area (AD), source area (AS), drain perimeter (PD), and source perimeter (PS) model parameters. The values of these parameters must be explicitly defined together with the channel length (L) and channel width (W) of each nMOS and pMOS device in the netlist to simulate drain and source parasitic capacitances in the BSIM3v3.2 (Level 7) model in Cadence PSpice. For Synopsis/Star-HSPICE this step is not needed if the ACM parameter is used to specify an automatic calculation method for the areas and perimeters [24]; however, in PSpice these values will default to zero and generate a simulation warning if not specified explicitly. Accounting for these parasitic capacitances is critical to the analog accuracy of the oscillator design simulations. Similar modifications must be made to the other device definitions in the Extract definition file (e.g. nMOS capacitor, Poly resistor) if used in future layouts for extraction and simulation in PSpice.

BSIM3v3 (HSPICE Level 49) MOSFET model parameters provided by MOSIS for the AMIS C5 (0.5 µm) process with nMOS-typical, pMOS-typical (tt) corner skew were used for all SPICE simulations except where noted [23]. To enable simulations using these parameters in Cadence PSpice, the HSPICE-aware “Level = 49” argument must be changed to “Level = 7” to apply the equivalent BSIM3v3 model in PSpice. Additional notes regarding HSPICE/PSpice model compatibility are also provided by MOSIS [24].

All circuits were simulated for \( V_{DD} = 5.0 \) V and \( V_{SS} = 0 \) V (ground) at 27°C (room temperature). Initial condition (.IC) statements were used as needed in SPICE input files to force voltages on output nodes to initiate steady-state oscillation. SPICE simulation model parameters and input netlist files used in the following sections are presented in Appendices F and G.
5.3 Single-Ended Ring Oscillator Design and Analysis

The single-ended ring oscillator is comprised of a series of standard complementary inverters (consisting of one pMOS pull-up device and one nMOS pull-down device) in which the output of each inverter stage is fed into the input of the successive stage, and the output of the final stage is fed back to the input of the first stage, as illustrated in Figure 5.1. To create and maintain oscillation, the inverter chain must contain an odd number of stages, with a minimum of three stages. Oscillation will self-start in fabricated devices due to the amplification and inversion of transient thermal noise. The single-ended ring oscillator is capable of full $V_{DD}$ to $V_{SS}$ voltage output swing, provided the voltage rise and fall times are sufficiently small relative to the switching frequency. The delay of each stage, $t_D$, is most readily calculated with the formula

$$t_D = \frac{1}{2Nf_N}$$  \hspace{1cm} (5.1)

where $N$ is the total number of stages and $f_N$ is the observed frequency of operation of an $N$-stage ring oscillator [25]. The average power dissipation of an $N$-stage single-ended ring oscillator can be approximated by

$$P_{RMS} \approx Nq_{max}V_{DD}f_N$$  \hspace{1cm} (5.2)

assuming the load capacitance of each stage is charged to $q_{max}$ and discharged during each oscillation period [25].

A standard complementary inverter cell layout with the design-rule-minimum MOS channel dimensions ($W/L = 0.9/0.6$ µm), shown in Figure 5.2, was created and instanced to create single-ended ring oscillator layouts for several values of $N$. An example 3-stage structure is shown in Figure 5.3; however, because the maximum simulated output voltage for $N = 3$ was less than $V_{DD}$, the fewest number of stages considered for analysis was $N = 5$. Single-ended ring
Figure 5.1: Single-Ended Ring Oscillator Block Diagram
Figure 5.2: Complementary Inverter Layout ($W/L = 0.9/0.6 \mu m$)
Figure 5.3: 3-Stage Single-Ended Ring Oscillator Layout
oscillators with $N = 5, 15, 25,$ and $31$ were simulated to observe trends in output frequency ($f_N$), delay per stage ($t_d$), signal 10%-90% rise time ($t_r$), signal 90%-10% fall time ($t_f$), and RMS power dissipation ($P_{RMS}$) versus the number of inverter stages. Sample output waveforms for the $N = 5$ and $N = 31$ structures are shown in Figure 5.4. Analyzing the simulation results and applying Equations 5.1 and 5.2 yielded the data in Table 5.1 below.

### Table 5.1: Single-Ended Ring Oscillator ($W/L = 0.9/0.6 \mu m$) Simulation Results

<table>
<thead>
<tr>
<th>N</th>
<th>$f_N$</th>
<th>$t_D$</th>
<th>$t_R$</th>
<th>$t_F$</th>
<th>$P_{RMS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>163.3 MHz</td>
<td>0.612 ns</td>
<td>1.43 ns</td>
<td>0.99 ns</td>
<td>375.0 µW</td>
</tr>
<tr>
<td>15</td>
<td>54.8 MHz</td>
<td>0.608 ns</td>
<td>1.76 ns</td>
<td>1.19 ns</td>
<td>375.0 µW</td>
</tr>
<tr>
<td>25</td>
<td>33.0 MHz</td>
<td>0.606 ns</td>
<td>2.16 ns</td>
<td>1.36 ns</td>
<td>375.0 µW</td>
</tr>
<tr>
<td>31</td>
<td>26.6 MHz</td>
<td>0.605 ns</td>
<td>2.39 ns</td>
<td>1.59 ns</td>
<td>375.0 µW</td>
</tr>
</tbody>
</table>

Several conclusions about the characteristics and interrelationships of the single-ended oscillator specifications are supported by the simulation results. The time delay per stage is a factor of the inverter design, specifically the $W/L$ ratios that determine transconductance ($g_m$), hence $t_d$ is independent of $N$. Since power in complementary inverters is dissipated essentially only when switching (neglecting leakage), and since the inverters within the delay chain switch sequentially at a constant propagation rate determined by $t_D$ and independent of $N$, it follows that average power dissipation is also independent of the length of the delay chain. Then, to satisfy Equations 5.1 and 5.2 for a constant $V_{DD}$ and $q_{max}$ fixed for the nMOS and pMOS dimensions, the product of the number of stages and the corresponding output frequency must be constant, i.e. $N$ and $f_N$ are inversely proportional. The oscillation period ($t_N = 1/f_N$) is equal to $2Nt_D$ since both the rising and falling edges of the ring oscillator’s output signal propagate through the entire delay chain sequentially during each cycle. Lastly, for equivalent channel dimensions, the lower impedance nMOS pull-down devices produce falling edge rates that are faster than the rising edge rates produced by the higher impedance pMOS pull-up devices.
Figure 5.4: Single-Ended Ring Oscillator Output Waveforms  
(a) $N = 5$  
(b) $N = 31$
5.4 MOS Channel Sizing and Simulation-To-Silicon Accuracy

Although devices with the design-rule-minimum MOS channel width of 0.9 µm ($3\lambda$) will be functional, MOSIS recommends a wider minimum of 3.0 µm ($10\lambda$) in analog designs for the AMIS 0.5 µm process, claiming that the electrical characteristics of narrower devices are neither scalable nor accurately predictable with MOSIS-provided SPICE parameters [26]. For each process run, MOSIS embeds a standard 31-stage single-ended ring oscillator designed with their recommended-minimum MOS channel dimensions ($W/L = 3.0/0.6$ µm) into each wafer of the lot. The average measured oscillation frequency at $V_{DD} = 5.0$ V is reported in the parametric test results of each lot, along with lot-specific SPICE BSIM3v3 parameters. To evaluate the effects of MOS channel dimensions on oscillator performance as well as simulation-to-silicon accuracy, a second complementary inverter cell layout with $W/L = 3.0/0.6$ µm, shown in Figure 5.5, was created and instanced to create new 5-stage and 31-stage single-ended ring oscillator layouts. The additional active contacts were added to the wider drains and sources to reduce resistance.

First, to compare the performance of single-ended ring oscillators with different MOS channel widths, the new designs were simulated using the same typical corner SPICE BSIM3v3 parameters used in the previous section. The simulation results are shown in Table 5.2 below.

<table>
<thead>
<tr>
<th>N</th>
<th>$f_N$</th>
<th>$t_D$</th>
<th>$t_R$</th>
<th>$t_F$</th>
<th>$P_{RMS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>593.9 MHz</td>
<td>0.168 ns</td>
<td>0.40 ns</td>
<td>0.24 ns</td>
<td>2.98 mW</td>
</tr>
<tr>
<td>31</td>
<td>95.6 MHz</td>
<td>0.169 ns</td>
<td>0.60 ns</td>
<td>0.38 ns</td>
<td>3.00 mW</td>
</tr>
</tbody>
</table>

Clearly, increasing MOS channel widths, thereby raising $g_m$ and lowering impedances, increases switching speed and reduces delay through each inverter stage, resulting in higher frequencies for the same number of stages. However, since $f_N$ increases for a given $N$, and $q_{max}$ increases due
Figure 5.5: Complementary Inverter Layout ($W/L = 3.0/0.6 \, \mu m$)
to the larger input capacitances of the wider gates, average power dissipation greatly increases as predicted by Equation 5.2. Thus, there is a tradeoff between footprint and power dissipation when designing for a particular output frequency.

Next, to evaluate simulation-to-silicon accuracy, the 31-stage single-ended ring oscillator ($W/L = 3.0/0.6 \ \mu m$) was re-simulated with lot-specific SPICE BSIM3v3 parameters obtained from MOSIS for two selected AMIS 0.5 \ \mu m runs (T36S and T39U), and the frequencies and power dissipation (reported per MHz per gate) obtained from the simulations and the fabrication parametric test results of each run were compared [27-28]. Table 5.3 summarizes the results, which show that simulated output frequencies correlate with test measurements with less than 10.7\% difference, and power dissipation likewise correlates with less than 8.2\% difference. The differences may be attributed to both fundamental inaccuracies in the SPICE model parameters and PSpice’s incomplete support for the HSPICE-targeted MOSIS BSIM3v3 parameters.

<table>
<thead>
<tr>
<th>Run/Lot #</th>
<th>Simulation</th>
<th>Fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$f_N$</td>
<td>$P_{RMS}$</td>
</tr>
<tr>
<td>T36S</td>
<td>105.0 MHz</td>
<td>0.51 uW/MHz/gate</td>
</tr>
<tr>
<td>T39U</td>
<td>105.4 MHz</td>
<td>0.51 uW/MHz/gate</td>
</tr>
</tbody>
</table>

5.5 Differential Ring Oscillator Design and Analysis

The differential ring oscillator is comprised of a series of differential inverters of the form shown in Figure 5.6, consisting of two symmetric nMOS driver transistors ($N_1$ and $N_2$) and load resistors ($R_L$) with a common constant tail current source ($I_{tail}$) [15]. In an ideal differential inverter stage, when the input voltages $V_{in1}$ and $V_{in2}$ are both equal to the same voltage $V_{quiescent}$, the $V_{gs}$ of each nMOS transistor is equal to $V_{quiescent} - V_{tail}$, where $V_{tail}$ is the voltage across the constant current source. The $I_{ds}$ of each transistor is equal to $I_{tail}/2$, and the output voltages $V_{out1}$
Figure 5.6: Ideal Differential Inverter Schematic
and $V_{out2}$ are equal [15]. If $V_{in1}$ and $V_{in2}$ increase or decrease equally, then $V_{tail}$ rises or falls respectively to maintain the same constant current through the tail source. The $I_{ds}$ of each transistor remains equal to $I_{tail}/2$, and the output voltage levels, dictated by the $I_{tail}R_{L}/2$ voltage drop across each load resistor, do not change. Therefore, the ideal Common Mode Gain of the differential inverter is zero. However, if $V_{in1}$ increases by $\delta V$, and $V_{in2}$ decreases by the same $\delta V$, then the $I_{ds}$ of $N_1$ will increase by $\delta I$, and the $I_{ds}$ of $N_2$ will decrease by $\delta I$. Inversely, $V_{out1}$ will decrease by $\delta IR_L$, and $V_{out2}$ will increase by $\delta IR_L$ [15]. Since $\delta I/\delta V$ is the $g_m$ of the nMOS driver, the ideal Differential Gain of the differential inverter is found to be

$$A_{\text{diff}} = -\frac{2\delta IR_L}{2\delta V} = -\frac{\delta IR_L}{\delta V} = -g_m R_L.$$  \hspace{1cm} (5.3)

The Common Mode Rejection Ratio (CMRR), defined as

$$CMRR = \frac{\text{Differential Gain}}{\text{Common Mode Gain}},$$  \hspace{1cm} (5.4)

is infinite for an ideal differential inverter; however, it will be limited for practical devices due to non-ideal constant current sources, lack of symmetry in the nMOS drivers and load resistors, etc. Unlike that of the complementary inverter, the maximum output voltage swing of the differential inverter is typically less than the full $V_{DD}$ to $V_{SS}$ range due to the positive biasing requirement of the constant tail current source. Assuming there is sufficient gain to drive the output voltages to rail, the output voltage swing limitations will be

$$V_{out_{\text{max}}} = V_{DD} \hspace{1cm} (5.5)$$

$$V_{out_{\text{min}}} = V_{DD} - I_{tail}R_L \hspace{1cm} (5.6)$$

with the stipulation that $V_{out_{\text{min}}}$ must be large enough to provide the minimum $V_{tail}$ required to meet the biasing requirement of the given constant tail current source design.

The differential ring oscillator can consist of three or more differential inverter delay
stages with inputs and outputs connected as shown in Figure 5.7 for both even and odd numbers of stages. The gain of each stage, $g_m R_L$, must be great enough to drive the output voltages to rail faster than the switching frequency, which is higher with fewer stages, to sustain oscillation. In fabricated devices oscillation will self-start due to the amplification of differential transient thermal noise across inputs. As with the single-ended ring oscillator, the time delay of a single differential delay stage is equal to

$$t_D = \frac{1}{2Nf_N}$$

(5.7)
given that $f_N$ is the observed output frequency of an $N$-stage differential ring oscillator. Unlike the single-ended ring oscillator, the power dissipation of an $N$-stage differential ring oscillator, given by the formula

$$P = NI_{tail}V_{DD}$$

(5.8)
is independent of frequency and time delay and increases linearly with the number of stages. There are a number of tradeoffs in terms of differential ring oscillator performance and power dissipation involved in the selection of load resistance, tail current, and nMOS channel width values. Table 5.4 summaries these tradeoffs [15].

<table>
<thead>
<tr>
<th>Design Component</th>
<th>Smaller Values</th>
<th>Larger Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Resistance ($R$)</td>
<td>+ high bandwidth</td>
<td>+ large gain</td>
</tr>
<tr>
<td></td>
<td>- small gain</td>
<td>- low bandwidth</td>
</tr>
<tr>
<td>Constant Current Source ($I_{tail}$)</td>
<td>+ small power dissipation</td>
<td>+ high bandwidth</td>
</tr>
<tr>
<td></td>
<td>- low bandwidth</td>
<td>- larger power dissipation</td>
</tr>
<tr>
<td>nMOS channel width ($W_N$)</td>
<td>+ small parasitic capacitance</td>
<td>+ large gain</td>
</tr>
<tr>
<td></td>
<td>- small gain</td>
<td>- large parasitic capacitance</td>
</tr>
</tbody>
</table>

Single-ended ring oscillators do have several advantages over differential ring oscillators. For the same $N$ and $f_N$, the single-ended variety typically has a smaller footprint, consumes less
Figure 5.7: Differential Ring Oscillator Block Diagrams  (a) Odd $N$  (b) Even $N$
power, exhibits less jitter and phase noise, is capable of greater output voltage swing if needed, and is simpler to design than the differential variety [25]. However, the primary advantages of the differential ring oscillator – its lower sensitivity to substrate and supply noise, and its lower noise injection into other circuits on the same chip – make it more attractive for designs targeted for noisy operating conditions [25]. It also automatically produces dual in-phase complementary outputs (inverted and non-inverted), and the small output voltage swing is useful for certain applications.

To implement the differential delay stage in CMOS, an nMOS current source is used in place of the ideal constant tail current source, and pMOS transistors are used to implement the large load resistances, as shown in Figure 5.8 [15]. To function as a pseudo-constant current source, the nMOS device must be biased to operate in the saturation region of the I-V curve shown in Figure 5.9. In this region the current through the nMOS device is nearly constant (except for channel length modulation effects) at a fixed $V_{gs}$ for any $V_{ds} > V_{gs} - V_{m}$, where $V_{m}$ is the threshold voltage of the nMOS device. For the differential delay stage, $V_{gs}$ is set by applying a fixed $V_{bias}$ on the nMOS gate, and $V_{ds}$ is equivalent to $V_{tail}$ which depends on the output voltage swing determined by $I_{tail}R$ (larger swing results in a smaller $V_{tail,min}$). Thus, for the nMOS to operate in the saturation region over the full output swing, $V_{bias}$ must be chosen to satisfy

$$V_{tail,min} > V_{bias} - V_{m}.$$  

(5.9)

The nMOS channel dimensions must be chosen to provide the desired $I_{tail}$ while keeping $V_{bias}$ sufficiently low (wider devices produce higher currents for lower bias voltages). Inversely, to function as pseudo-linear resistors, the pMOS devices must be biased to operate in the linear region, which is maintained for $V_{sd} < V_{sg} - V_{tp}$ and results in near-linear changes in the current through the device for changes in $V_{sd}$. This is satisfied simply by connecting the pMOS gates to
Figure 5.8: CMOS Differential Inverter Schematic
Figure 5.9: nMOS $I-V$ Curve

\[ V_{DS} = V_{GS} - V_T \]
$V_{SS}$ (ground), which sets $V_{sg}$ equal to $V_{DD}$ while $V_{sd}$ is limited to the output voltage swing ($V_{DD} - V_{out\text{min}}$). The pMOS channel dimensions then determine the load resistance (longer devices produce higher resistances).

To demonstrate the design process for a practical differential inverter and ring oscillator, the design, layout, and simulation of a differential inverter delay stage with an output voltage swing of 1.0 $V_{p-p}$ was completed and used to create differential ring oscillator layouts for several values of $N$. The 1.0 $V_{p-p}$ swing was chosen since it can be generated with minimal distortion for small transistor sizes, provides good margin for properly biasing the nMOS current source, and is practical for RF and communication signals (e.g. composite video) and test measurements. The MOSIS-recommended-minimum MOS channel dimensions ($W/L = 3.0/0.6 \ \mu m$) were used as the starting point for determining optimal transistor sizes.

First, to determine the values of $R_L$ and $I_{tail}$ needed to control the output swing with sufficient gain, a differential ring oscillator composed of delay stages with minimum-sized nMOS drivers and ideal resistor and current source models was simulated. Design choices to satisfy minimum gain requirements were made empirically from simulation results: to maintain oscillation with minimum-width nMOS drivers, a minimum $N = 8$ delay stages were used; for the best balance of gain and signal edge rolloff, nMOS driver dimensions of $W/L = 3.0/1.5 \ \mu m$ were chosen; a relatively small $R_L$ of 15 k$\Omega$ was found to provide sufficient differential gain to maintain oscillation given the nMOS driver size. From Equations 5.5 and 5.6:

$$V_{out\text{max}} = V_{DD} = 5 \ \text{V}$$

$$V_{out\text{min}} = V_{out\text{max}} - 1 = 4 \ \text{V}$$

$$I_{tail} = \frac{V_{DD} - V_{out\text{min}}}{R_L} = \frac{5 \ \text{V} - 4 \ \text{V}}{15 \ \text{k}\Omega} = 66.67 \ \text{mA}$$
Figure 5.10 shows $V_{out1}$, $V_{out2}$, and $V_{tail}$ waveforms for this design. Since $V_{tail\text{min}} \approx 3$ V, and assuming $V_{in} \approx 1$ V, the upper limit on $V_{bias}$ for the nMOS current source from Equation 5.9 is

$$V_{bias} < V_{tail\text{min}} + V_{in} \approx 4$$ V.

Next, the nMOS current source and pMOS load resistors were designed to match the ideal $I_{tail}$, $V_{bias}$, and $R_L$ values. DC sweeps of the gate voltage in SPICE were used to predict $I_{tail}$ across $V_{bias}$ for various nMOS channel dimensions. The previously chosen nMOS driver size ($W_n/L_n = 3.0/1.5 \ \mu$m) was found to produce an $I_{tail}$ of 66.67 mA at a satisfactory $V_{bias} \approx 1.75$ V with $V_{ds} = V_{tail\text{min}} = 3$ V as shown in Figure 5.11, so the same size was chosen for the nMOS current source. Similarly, DC sweeps of $V_{sd}$ in SPICE were used to predict the effective $R_L$ across the output voltage swing for various pMOS channel dimensions. A pMOS size of $W_p/L_p = 3.0/3.0 \ \mu$m was found to have a satisfactory effective $R_L$ range of 13-15 kΩ across a $V_{out}$ range of 4-5 V with the gate grounded as shown in Figure 5.12, so this size was chosen for the pMOS load resistors.

Finally, the differential inverter layout shown in Figure 5.13 was created with the chosen MOS dimensions and instanced to create differential ring oscillator layouts of various lengths. The example 3-stage and 4-stage structures shown in Figures 5.14 and 5.15 illustrate the routing differences for odd and even $N$. Differential ring oscillators with $N = 8$, 16, and 31 were simulated, and applying Equations 5.7 and 5.8 to the results yielded the data in Table 5.5 below. Sample output waveforms for the $N = 8$ and $N = 31$ structures are shown in Figure 5.16. Actual $I_{tail}$ and $V_{tail}$ levels for a single stage of the $N = 8$ structure are shown in Figure 5.17.

**Table 5.5: Differential Ring Oscillator Simulation Results**

<table>
<thead>
<tr>
<th>N</th>
<th>$f_N$</th>
<th>$t_D$</th>
<th>$t_R$</th>
<th>$t_F$</th>
<th>$P_{RMS}$</th>
<th>$1 \ V_{pp}$</th>
<th>$V_{bias}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>94.9 MHz</td>
<td>0.659 ns</td>
<td>3.20 ns</td>
<td>2.93 ns</td>
<td>2.78 mW</td>
<td>1.78 V</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>47.9 MHz</td>
<td>0.652 ns</td>
<td>3.69 ns</td>
<td>3.92 ns</td>
<td>5.42 mW</td>
<td>1.77 V</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>24.2 MHz</td>
<td>0.667 ns</td>
<td>5.62 ns</td>
<td>6.29 ns</td>
<td>10.4 mW</td>
<td>1.76 V</td>
<td></td>
</tr>
</tbody>
</table>
Figure 5.10: Ideal $N = 8$ Differential Ring Oscillator Output Waveforms
Figure 5.11: nMOS Current Source $I_{tail}$ vs. $V_{bias}$

$I_{tail} = 66.67$ mA
$V_{bias} = 1.75$ V
Figure 5.12: pMOS Load Effective $R_L$ vs. $V_{out}$
Figure 5.13: Differential Inverter Layout
Figure 5.14: 3-Stage Differential Ring Oscillator Layout
Figure 5.15: 4-Stage Differential Ring Oscillator Layout

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Figure 5.16: Differential Ring Oscillator Output Waveforms  
(a) $N = 8$  (b) $N = 31$
Figure 5.17: $N = 8$ Differential Ring Oscillator Current Source Biasing  
(a) $I_{\text{tail}}$  
(b) $V_{\text{tail}}$
5.6 Experimental Results, Conclusion, and Future Improvements

Experimental measurements of oscillation frequency, noise, and jitter for a single-ended ring oscillator were previously presented in Chapter 3. Experimental testing of a 0.5 μm test chip containing a differential ring oscillator was attempted. However, the oscillator was found to be non-functional, likely due to functionality problems or limitations experienced with the I/O pads in the layout for the 0.5 μm process.

Research and simulation results show that single-ended ring oscillators offer faster performance, lower power dissipation, and simpler design for high-frequency on-chip signal generation, while differential ring oscillators offer more robust and adjustable performance for strict design requirements. MOS channel dimensions significantly affect the speed performance, power requirements, and footprint of both single-ended and differential ring oscillator designs. Simulation-to-silicon accuracy is good for devices designed with the MOSIS-recommended minimum channel width.

These designs can be incorporated into future VCO and PLL test chip designs. The current differential ring oscillator design requires an external $V_{bias}$ source to control the tail current source and output voltage swing. If an external constant current source is available, a current mirror can also be used to set $V_{bias}$. Future improvements may include a closed-loop biasing circuit requiring no additional external sources.
Chapter 6

Summary and Conclusions

A best-possible high-frequency CMOS VLSI chip testing environment using available laboratory resources, the Tektronix 11801A Digital Sampling Oscilloscope, the Hewlett-Packard 8133A 3 GHz Pulse Generator, and a custom-built DUT socket interface board has been defined, documented, and tested. A LabVIEW and MATLAB-based software solution for waveform data acquisition from the 11801A oscilloscope via GPIB and advanced numerical analysis capabilities has been implemented. The enabling of the utilization of these high-speed testing instruments with the improved DUT interface hardware has led to a minimum 25x improvement in overall measurement system bandwidth over previously used interface hardware and configurations, with a maximum analog bandwidth of approximately 250 MHz. Advanced signal measurements, including noise, jitter, and TDR, have been enabled, documented, and conducted with this testing environment. The limiting factor for high-frequency testability in this setup is the use of jumper wire and sockets on the interface board to connect the DUT to the test equipment. A properly designed custom interface PCB used with surface-mount devices would significantly increase overall system bandwidth and signal integrity, likely enabling accurate measurement and testing above 1 GHz with the same test equipment.

Experimental on-chip metal-layer interconnect impedance, signal integrity, and delay measurements have been collected using the high-frequency testing environment. The sheet resistance values calculated from the interconnect resistance measurements match those provided by MOSIS for the test chip’s process run. Although the precision and integrity of the I/O delay measurements were limited by the design of the DUT interface board, a reasonable estimate of 22.9 ps/mm has been derived from the measurement results.
Theoretical analysis, physical and equivalent-circuit modeling, parasitic extraction tools, and SPICE implementation techniques for on-chip interconnect simulation at high frequencies have been documented, developed, and applied to model the metal-layer interconnect of the test chip. The field solver and SPICE simulation results closely match theoretical calculations and experimental measurement data. The freely available FastCap and FastHenry 3D field solvers have been shown to be powerful and accurate tools for on-chip interconnect parasitic extraction, modeling, and simulation. However, since no non-commercial graphical modeling or layout extraction interface to these programs is currently available, and input model files must be generated numerically and manually, their application is limited to simple layouts and structures.

Lastly, the characteristics, design, layout, and simulation of single-ended and differential CMOS ring oscillators used for on-chip high-frequency signal generation have been presented and completed. Guidelines for accurate high-frequency simulation of submicron devices using MOSIS design rules in Cadence PSpice 10.0 have been specified. Oscillation frequency and power dissipation simulation results for a 31-stage single-ended ring oscillator layout designed for a 0.5 μm process agree with experimental data for 0.5 μm process runs provided by MOSIS. The differential ring oscillator designs and layouts can be incorporated into future VCO and PLL designs for test chips to be validated in the high-frequency measurement environment.
References


Appendix A: LabVIEW Agilent-Compatible Installation Method

To use an Agilent GPIB card with LabVIEW and NI-VISA, complete the following installation procedure. Reboot the PC when prompted.

1. Uninstall all previous Agilent IO Libraries, NI-VISA, and LabVIEW installations.
2. Uninstall the Agilent GPIB card from the PC, if currently installed.
3. Install NI-VISA (version 2.5 or later).
4. Install the Agilent GPIB card in the PC.
5. Install the Agilent IO Libraries (version J.01.00 or later) and choose the “SICL and side-by-side Agilent VISA Installation” option.
6. Configure the Agilent GPIB card using the Agilent IO Config program.
7. Open the NI Measurement and Automation Explorer (MAX) program.
8. From the menu bar, select “Tools > NI-VISA > Passport Editor”.
9. Check the box next to “NIVisaTulip.dll – VISA Library Passport for Tulip”.
10. Close the MAX program.
11. The Agilent GPIB card should now be accessible through NI-VISA.
function [TIME, TRA1, TRA2] = lvmconv(filename)

DATA = csvread(filename);

for i = 1:512,
    TIME(i) = DATA(1,4) * DATA(i,1) * 1e9;
    TRA1(i) = DATA(1,5) + DATA(1,6) * DATA(i,2);
    TRA2(i) = DATA(1,10) + DATA(1,11) * DATA(i,7) * 2;
end

figure
hold on
xlim([TIME(1) TIME(512)]);
ylim([-0.55,0.55]);
xlabel('Time (Nanoseconds)');
ylabel('Amplitude (Volts)');
title(filename([1:(length(filename)-4)]));
plot(TIME, TRA1, 'b')
plot(TIME, TRA2, 'r')
Appendix C: Metal-3 Interconnect Waveforms

Figure C.1: Metal-3 Interconnect 15 MHz Pulse  (a) Pulse Shape   (b) Rising Edge
Figure C.2: Metal-3 Interconnect 35 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure C.3: Metal-3 Interconnect 40 MHz Pulse  
(a) Pulse Shape  
(b) Rising Edge
Figure C.4: Metal-3 Interconnect 50 MHz Pulse   (a) Pulse Shape   (b) Rising Edge
Figure C.5: Metal-3 Interconnect 60 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure C.6: Metal-3 Interconnect 75 MHz Pulse  
(a) Pulse Shape  
(b) Rising Edge
Figure C.7: Metal-3 Interconnect 90 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
Figure C.8: Metal-3 Interconnect 100 MHz Pulse  (a) Pulse Shape   (b) Rising Edge
Figure C.9: Metal-3 Interconnect 200 MHz Pulse  (a) Pulse Shape  (b) Rising Edge
## Appendix D: FastCap and FastHenry Input Model Files

### D.1 FastCap Input File

0 Three Parallel Interconnect (WxDxL = 1.8u x 1.8u x 1m, Spacing = 0.9u)

| Q 1 | 0.0e-6 | 0.0e-6 | 0.0e-4 | 1.8e-6 | 0.0e-6 | 0.0e-4 | 1.8e-6 | 0.3e-6 | 0.0e-4 | 0.0e-6 | 0.3e-6 | 0.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 0.0e-4 | 1.8e-6 | 0.0e-6 | 1.0e-4 | 1.8e-6 | 0.3e-6 | 1.0e-4 | 1.8e-6 | 0.3e-6 | 0.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 0.0e-4 | 1.8e-6 | 0.0e-6 | 1.0e-4 | 0.0e-6 | 0.0e-6 | 1.0e-4 | 0.0e-6 | 0.0e-6 | 0.0e-4 |
| Q 1 | 0.0e-6 | 0.0e-6 | 0.0e-4 | 0.0e-6 | 0.3e-6 | 0.0e-4 | 0.0e-6 | 0.3e-6 | 1.0e-4 | 0.0e-6 | 0.3e-6 | 1.0e-4 |
| Q 1 | 1.8e-6 | 0.3e-6 | 0.0e-4 | 1.8e-6 | 0.3e-6 | 1.0e-4 | 0.0e-6 | 0.3e-6 | 1.0e-4 | 0.0e-6 | 0.3e-6 | 0.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 1.0e-4 | 1.8e-6 | 0.3e-6 | 1.0e-4 | 0.0e-6 | 0.3e-6 | 1.0e-4 | 0.0e-6 | 0.3e-6 | 1.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 1.0e-4 | 1.8e-6 | 0.3e-6 | 2.0e-4 | 1.8e-6 | 0.3e-6 | 2.0e-4 | 1.8e-6 | 0.3e-6 | 1.0e-4 |
| Q 1 | 0.0e-6 | 0.0e-6 | 1.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 1.8e-6 | 0.3e-6 | 1.0e-4 | 1.8e-6 | 0.3e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 2.0e-4 | 1.8e-6 | 0.3e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 2.0e-4 | 1.8e-6 | 0.3e-6 | 3.0e-4 | 1.8e-6 | 0.3e-6 | 3.0e-4 | 1.8e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 0.0e-6 | 0.0e-6 | 2.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 |
| Q 1 | 1.8e-6 | 0.3e-6 | 2.0e-4 | 1.8e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 3.0e-4 | 1.8e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 0.0e-6 | 0.0e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 | 0.0e-6 | 0.3e-6 | 2.0e-4 |
| Q 1 | 1.8e-6 | 0.3e-6 | 3.0e-4 | 1.8e-6 | 0.3e-6 | 4.0e-4 | 1.8e-6 | 0.3e-6 | 4.0e-4 | 1.8e-6 | 0.3e-6 | 3.0e-4 |
| Q 1 | 1.8e-6 | 0.0e-6 | 4.0e-4 | 1.8e-6 | 0.3e-6 | 4.0e-4 | 0.0e-6 | 0.3e-6 | 4.0e-4 | 0.0e-6 | 0.3e-6 | 3.0e-4 |

0 Total capacitance of capacitors: 1.5pF, 2pF, 2pF
<table>
<thead>
<tr>
<th>Q 3</th>
<th>7.2e-6</th>
<th>0.0e-6</th>
<th>1.0e-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q 3</td>
<td>4.5e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
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<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
<tr>
<td>Q 3</td>
<td>2.7e-6</td>
<td>0.3e-6</td>
<td>2.0e-4</td>
</tr>
</tbody>
</table>

Q 2
| 4.5e-6 | 0.0e-6 | 1.0e-4 |
| 4.5e-6 | 0.0e-6 | 2.0e-4 |
| 4.5e-6 | 0.0e-6 | 3.0e-4 |
| 4.5e-6 | 0.0e-6 | 4.0e-4 |
| 4.5e-6 | 0.0e-6 | 5.0e-4 |
| 4.5e-6 | 0.0e-6 | 6.0e-4 |
| 4.5e-6 | 0.0e-6 | 7.0e-4 |
| 4.5e-6 | 0.0e-6 | 8.0e-4 |
| 4.5e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |

Q 2
| 2.7e-6 | 0.0e-6 | 1.0e-4 |
| 2.7e-6 | 0.0e-6 | 2.0e-4 |
| 2.7e-6 | 0.0e-6 | 3.0e-4 |
| 2.7e-6 | 0.0e-6 | 4.0e-4 |
| 2.7e-6 | 0.0e-6 | 5.0e-4 |
| 2.7e-6 | 0.0e-6 | 6.0e-4 |
| 2.7e-6 | 0.0e-6 | 7.0e-4 |
| 2.7e-6 | 0.0e-6 | 8.0e-4 |
| 2.7e-6 | 0.0e-6 | 9.0e-4 |


D.2 FastHenry Input File

* Three Parallel Interconnect (WxDxL = 1.8u x 1.8u x 1m, Spacing = 0.9u)

* Values in millimeters
. Units mm

* Conductivity of Aluminum (Al) Interconnect
. Default sigma=3.7e4

N1 x=0 y=0 z=0
N2 x=0 y=0 z=1
N3 x=0.0027 y=0 z=0
N4 x=0.0027 y=0 z=1
N5 x=0.0054 y=0 z=0
N6 x=0.0054 y=0 z=1
E1 N1 N2 w=0.0018 h=0.0003
E2 N3 N4 w=0.0018 h=0.0003
E3 N5 N6 w=0.0018 h=0.0003

.extern N1 N2
.extern N3 N4
.extern N5 N6

.freq fmin=1e8 fmax=1e9 ndec=1

.end
Appendix E: SPICE Interconnect Simulation Netlists and Input Files

E.1 Measurement Environment Model

* Measurement Environment Model

VP 9 0 PULSE(0 1 0 1n 1n 4n 10n)

R1 1 2 18.8
L1 2 3 0.735e-9
C1 3 0 4.425e-14
R2 3 4 18.8
L2 4 5 0.735e-9
C2 5 0 4.425e-14
R3 5 6 18.8
L3 6 7 0.735e-9
C3 7 0 4.425e-14

T1 9 0 1 0 ZO=50 TD=332p
T2 7 0 8 0 ZO=20 TD=332p

RT 8 0 50

.TRAN 1p 50n
.PROBE
.END

E.2 Inverter-Inverter Interconnect Delay

* Inverter-Inverter Delay Line

.include mamis05.md

* NODE NAME ALIASES
*  1 = VOUT (159,29.5)
*  2 = VDD (83,56)
*  3 = B (86,29.5)
*  4 = VSS (83,3)
*  5 = A (74,29.5)
*  6 = VIN (1,29.5)

* Parasitic Drain/Source Capacitances
Cpar1 1 0 76.56264f
Cpar2 2 0 160.79568f
Cpar3 4 0 140.33916f
Cpar4 5 0 76.56264f

M4 1 3 4 4 NMOS L=600n W=20.1u AD=36.18p PD=43.8u AS=36.18p PS=43.8u
M3 4 6 5 4 NMOS L=600n W=20.1u AD=36.18p PD=43.8u AS=36.18p PS=43.8u
M2 1 3 2 2 PMOS L=600n W=20.1u AD=36.18p PD=43.8u AS=36.18p PS=43.8u
M1 5 6 2 2 PMOS L=600n W=20.1u AD=36.18p PD=43.8u AS=36.18p PS=43.8u

* Ideal Zero-Delay Interconnect
R1 5 3 1
* Distributed Delay Line Interconnect
R01 5 7 25
L01 7 8 0.897e-9
C01 8 0 4.425e-14
R02 8 9 25
L02 9 10 0.897e-9
C02 10 0 4.425e-14
R03 10 11 25
L03 11 12 0.897e-9
C03 12 0 4.425e-14
R04 12 13 25
L04 13 14 0.897e-9
C04 14 0 4.425e-14
R05 14 15 25
L05 15 16 0.897e-9
C05 16 0 4.425e-14
R06 16 17 25
L06 17 18 0.897e-9
C06 18 0 4.425e-14
R07 18 19 25
L07 19 20 0.897e-9
C07 20 0 4.425e-14
R08 20 21 25
L08 21 22 0.897e-9
C08 22 0 4.425e-14
R09 22 23 25
L09 23 24 0.897e-9
C09 24 0 4.425e-14
R10 24 25 25
L10 25 3 0.897e-9
C10 3 0 4.425e-14

VDD 2 0 DC 5
VSS 4 0 DC 0

* 1 GHz Clock Frequency
* VIN 6 0 PULSE(0 5 0 70p 70p 430p 1n)

* 500 MHz Clock Frequency
* VIN 6 0 PULSE(0 5 0 140p 140p 860p 2n)

* Step Response
* VIN 6 0 PWL(0 5 1n 5 1.001n 0)

.TRAN 1p 3n
.PROBE
.END
Appendix F: SPICE BSIM3v3 MOSFET Model Parameters

F.1 AMIS C5 (0.5 µm) nMOS/pMOS Typical (tt) Corner Parameters

```
.MODEL NMOS NMOS (LEVEL = 7
+VERSION = 3.1 TNOM = 27 TOX = 1.39E-8
+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.6696061
+K1 = 0.8351612 K2 = -0.0839158 K3 = 23.1023856
+K3B = -7.6841108 W0 = 1E-8 NLX = 1E-9
+DVTOW = 0 DVTIW = 0 DVT2W = 0
+DVT0 = 2.9047241 DVT1 = 0.4302695 DVT2 = -0.134857
+U0 = 458.439679 UA = 1E-13 UB = 1.485499E-18
+UC = 1.629939E-11 VSAT = 1.643993E5 A0 = 0.6103537
+AGS = 0.1194608 B0 = 2.674756E-6 B1 = 5E-6
+KETA = -2.640681E-3 A1 = 8.219585E-5 A2 = 0.3564792
+RDSW = 1.387108E3 PRWB = 0.0363981 DROUT = 0.7283566
+WR = 1 WINT = 2.472348E-7 LINT = 3.597605E-8
+XL = 0 WX = 0 DWG = -1.287163E-8
+DWB = 5.306586E-8 VOFF = 0 NFACTOR = 0.8365585
+CT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.0246738 ETAB = -1.406123E-3
+DSUB = 0.2543458 PCLM = 2.5945188 PDIBLC1 = -0.4282336
+PSCBE1 = 5.598623E8 PSCBE2 = 5.461645E-5 PVAG = 0
+DELTA = 0.01 RSH = 81.8 MOBMOD = 1
+PRT = 8.621 UTE = -1 KTI = -0.2501
+KT1L = -2.58E-9 KT2 = 0 UA1 = 5.4E-10
+UB1 = -4.8E-19 UC1 = -7.5E-11 AT = 1E5
+WL = 0 WL = 0 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 LINT = 3.597605E-8 XPART = 0.5
+CGDO = 2E-10 CGSO = 2E-10 CGBS = 1E-9
+CBS = 0.4197772E-4 PB = 0.99 MJ = 0.4515044
+CSBS = 3.242724E-10 PBSW = 0.1 MJSW = 0.1153991
+CSBSW = 1.64E-10 PBSWG = 0.1 MJSWG = 0.1153991
+CF = 0 PVTH0 = 0.0585501 FRDSW = 133.285505
+PK2 = -0.0299638 WKETA = -0.0248758 LKETA = 1.173187E-3
+AF = 1 KF = 0)

.MODEL PMOS PMOS (LEVEL = 7
+VERSION = 3.1 TNOM = 27 TOX = 1.39E-8
+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9214347
+K1 = 0.5553722 K2 = 8.763328E-3 K3 = 6.3063558
+K3B = -6.4873626 W0 = 1.280703E-8 NLX = 2.593997E-8
+DVTOW = 0 DVTIW = 0 DVT2W = 0
+DVT0 = 2.5131165 DVT1 = 0.5480536 DVT2 = -0.1186489
+U0 = 212.016613 UA = 2.807115E-9 UB = 1E-21
+UC = -5.82128E-11 VSAT = 1.713601E5 A0 = 0.8430019
+AGS = 0.1328608 B0 = 7.117912E-7 B1 = 5E-6
+KETA = -3.674859E-3 A1 = 4.77502E-5 A2 = 0.3
+RDSW = 2.837206E3 PRWG = -0.0363908 PRWB = -1.016722E-5
+WR = 1 WINT = 2.838038E-7 LINT = 5.528807E-8
+XL = 0 WX = 0 DWG = -1.606385E-8
+DWB = 2.266386E-8 VOFF = -0.0558512 NFACTOR = 0.9342488
```
F.2 MOSIS AMIS C5 (0.5 µm) Lot T36S Parameters

```
+MODEL NMOS NMOS (LEVEL = 7
+VERSION = 3.1
+TNOM = 27
+TOX = 1.41E-8
+PB = 0.9527355
+MJSW = 0.2958392
+PVTH0 = 0.1375778
+PRDSW = -174.8924404
```

```
F.3 MOSIS AMIS C5 (0.5 µm) Lot T39U Parameters

```plaintext
"MODEL NMG NMG (                                 LEVEL = 7
+VERSION = 3.1  TNOM = 27  TOX = 1.41E-8
+XJ = 1.5E-7  NCH = 1.7E17  VTH0 = 0.6047705
+K1 = 0.880153  K2 = -0.0936139  K3 = 26.1987415
+K3B = -7.3719352  W0 = 1E-8  NLX = 1E-9
+DVTOW = 0  DVT1W = 0  DVT2W = 0
+DVT0 = 3.9068989  DVT1 = 0.4061088  DVT2 = -0.078731
+U0 = 450.4728054  UA = 1E-13  UB = 1.464343E-18
+UC = 8.129968E-12  VSAT = 1.891853E5  A0 = 0.6020701
+AGS = 0.1210159  B0 = 2.588908E-6  B1 = 5E-6
+K ETA = -1.406419E-3  A1 = 6.379672E-4  A2 = 0.3077349
+RDSW = 1.007762E3  PRWG = 0.1270801  PRWB = 0.0539514
+WR = 1  WINT = 2.126498E-7  LINT = 5.643293E-8
+XL = 0  XW = 0  DWG = -1.414012E-9
+DWB = 6.03672E-8  VOFF = -5.104575E-5  NFACTOR = 0.7913376
)```

145
+CIT = 0  CDSC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 2.265836E-3  ETAB = -1.432795E-4
+DSUB = 0.0644669  PCLM = 2.5170771  PDIBLC1 = 0.938898
+PDIBLC2 = 2.121911E-3  PDIBLCB = 0  DROUT = 0.9200824
+PSCBE1 = 6.514708E8  PSCBE2 = 2.827643E-4  PVAG = 0
+DELT A = 0.01  RSH = 82.4  MOBMOD = 1
+PRT = 0  UTE = -1.5  KT1 = -0.11
+KT1L = 0  KT2 = 0.022  UA1 = 4.31E-9
+UB1 = -7.61E-18  UC1 = -5.6E-11  AT = 3.3E4
+WL = 0  WLN = 1  WW = 0
+WLN = 1  LW = 0  LWN = 1
+LWL = 0  CAPMOD = 2  XPART = 0.5
+CGDO = 2.04E-10  CGSO = 2.04E-10  CGBO = 1E-9
+CJ = 4.337161E-4  PB = 0.9412671  MJ = 0.4343185
+CJSW = 2.77139E-10  PBSW = 0.8  MJSW = 0.1696042
+CJSWG = 1.64E-10  PBSWG = 0.8  MJSWG = 0.1696042
+CF = 0  FVT0H = 0.0993944  PRDSW = 198.3850006
+PK2 = -0.0162644  WKET A = -0.0223371  LKETA = 3.49952E-3

) .MODEL PMOS PMOS ( LEVEL = 7
+VERSION = 3.1  TNOM = 27  TOX = 1.41E-8
+XJ = 1.5E-7  NCH = 1.7E17  VTH0 = -0.9264447
+K1 = 0.5167172  K2 = 0.0147998  K3 = 6.2190887
+K3B = -0.861117  W0 = 1E-8  NLX = 1E-9
+DVTOW = 0  DVT1W = 0  DVT2W = 0
+DVT0 = 2.4669501  DVT1 = 0.4454744  DVT2 = -0.077516
+U0 = 207.8178568  UA = 2.831663E-9  UB = 1.360669E-21
+UC = -6.18304E-11  VSAT = 2E5  A0 = 0.8698195
+AGS = 0.1440491  B0 = 1.311386E-6  B1 = 4.898717E-6
+KETA = -1.696864E-3  A1 = 0  A2 = 0.3
+RDSW = 2.150935E3  PRWG = 1.088595E-3  PRWB = -0.074831
+WR = 1  WINT = 3.230059E-7  LINT = 6.843022E-8
+XL = 0  XW = 0  DWG = -2.508317E-8
+DWB = 1.475942E-8  VOFF = -0.0371851  NFACTOR = 0.6968013
+CIT = 0  CDSC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 0.1879247  ETAB = -0.1362702
+DSUB = 1  PCLM = 2.1403084  PDIBLC1 = 0.1057656
+PDIBLC2 = 4.390793E-3  PDIBLCB = -0.0477652  DROUT = 0.2875568
+PSCBE1 = 5.096006E9  PSCBE2 = 5.009254E-10  PVAG = 0.0150529
+DELT A = 0.01  RSH = 104.7  MOBMOD = 1
+PRT = 0  UTE = -1.5  KT1 = -0.11
+KT1L = 0  KT2 = 0.022  UA1 = 4.31E-9
+UB1 = -7.61E-18  UC1 = -5.6E-11  AT = 3.3E4
+WL = 0  WLN = 1  WW = 0
+WLN = 1  LW = 0  LWN = 1
+LWL = 0  CAPMOD = 2  XPART = 0.5
+CGDO = 2.74E-10  CGSO = 2.74E-10  CGBO = 1E-9
+CJ = 7.118124E-4  PB = 0.9813695  MJ = 0.4991914
+CJSW = 2.713496E-10  PBSW = 0.99  MJSW = 0.2824528
+CJSWG = 6.4E-11  PBSWG = 0.99  MJSWG = 0.2824528
+CF = 0  FVT0H = 5.98016E-3  PRDSW = 14.8598424
+PK2 = 3.73981E-3  WKET A = 6.200933E-3  LKETA = -8.125108E-3

)
Appendix G: SPICE Ring Oscillator Simulation Netlists and Input Files

G.1 Single-Ended Ring Oscillator, $N = 5$ ($W/L = 0.9/0.6 \text{ µm}$)

* Inverter (Minimum Size) Ring Oscillator -- 05-Stage

```
.include typical.md
* NODE NAME ALIASES
* 1 = VOUT (69,29.5)
* 2 = VSS (72,3)
* 3 = VDD (72,56)

Cpar1 1 0 13.92132f
Cpar2 2 0 39.2736f
Cpar3 3 0 46.74618f
Cpar4 4 0 9.60432f
Cpar5 5 0 9.60432f
Cpar6 6 0 9.60432f
Cpar7 7 0 9.60432f

M10 2 5 4 2 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M9 2 4 6 2 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M8 2 7 1 2 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M7 2 6 7 2 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M6 2 1 5 2 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M5 4 5 3 3 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M4 6 4 3 3 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M3 1 7 3 3 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M2 7 6 3 3 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M1 5 1 3 3 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u

VDD 3 0 DC 5
VSS 2 0 DC 0

.IC V(1)=0

.TRAN 1n 100n
.PROBE
.END
```

G.2 Single-Ended Ring Oscillator, $N = 15$ ($W/L = 0.9/0.6 \text{ µm}$)

* Inverter (Minimum Size) Ring Oscillator -- 15-Stage

```
.include typical.md
* NODE NAME ALIASES
* 7 = VOUT (199,29.5)
* 15 = VDD (202,56)
* 17 = VSS (202,3)

Cpar1 1 0 9.60432f
Cpar2 2 0 9.60432f
```
M30 17 1 7 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M29 17 2 1 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M28 17 4 3 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M27 17 3 5 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M26 17 5 2 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M25 17 8 16 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M24 17 16 6 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M23 17 6 4 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M22 7 1 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M21 1 2 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M20 3 4 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M19 5 3 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M18 2 5 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M17 16 8 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M16 6 15 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M15 4 6 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M14 17 10 9 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M13 17 9 11 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M12 17 11 8 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M11 17 13 12 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M10 17 12 14 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M9 17 14 10 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M8 17 7 13 17 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M7 9 10 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M6 11 9 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M5 8 11 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M4 12 13 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M3 14 12 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M2 10 14 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M1 13 7 15 15 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u

VDD 15 0 DC 5
VSS 17 0 DC 0

.IC V(7)=5
.TRAN 1n 50n
.PROBE
.END
G.3 Single-Ended Ring Oscillator, \( N = 25 \) (\( W/L = 0.9/0.6 \) \( \mu m \))

* Inverter (Minimum Size) Ring Oscillator -- 25-Stage

.include typical.md

* NODE NAME ALIASES
*     17 = VOUT (329,29.5)
*     25 = VDD (332,56)
*     27 = VSS (332,3)

Cpar1 1 0 9.60432f
Cpar2 2 0 9.60432f
Cpar3 3 0 9.60432f
Cpar4 4 0 9.60432f
Cpar5 5 0 9.60432f
Cpar6 6 0 9.60432f
Cpar7 7 0 9.60432f
Cpar8 8 0 9.60432f
Cpar9 9 0 9.60432f
Cpar10 10 0 9.60432f
Cpar11 11 0 9.60432f
Cpar12 12 0 9.60432f
Cpar13 13 0 9.60432f
Cpar14 14 0 9.60432f
Cpar15 15 0 9.60432f
Cpar16 16 0 9.60432f
Cpar17 17 0 27.10332f
Cpar18 18 0 9.60432f
Cpar19 19 0 9.60432f
Cpar20 20 0 9.60432f
Cpar21 21 0 9.60432f
Cpar22 22 0 9.60432f
Cpar23 23 0 9.60432f
Cpar24 24 0 9.60432f
Cpar25 25 0 231.07218f
Cpar26 26 0 9.60432f
Cpar27 27 0 195.42f

M50 27 2 1 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M49 27 1 17 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M48 1 2 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M47 17 1 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M46 27 4 3 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M45 27 3 5 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M44 2 5 27 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M43 27 7 6 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M42 27 6 8 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M41 27 8 4 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M40 27 10 9 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M39 27 9 7 27 NMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M38 3 4 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M37 5 3 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M36 2 5 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M35 6 7 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
M34 8 6 25 25 PMOS L=600n W=900n AD=2.52p PD=6.6u AS=2.52p PS=6.6u
G.4 Single-Ended Ring Oscillator, \( N = 31 \) (\( W/L = 0.9/0.6 \) µm)

* Inverter (Minimum Size) Ring Oscillator -- 31-Stage

.include typical.md

* NODE NAME ALIASES
* 23 = VOUT (407,29.5)
* 31 = VDD (410,56)
* 33 = VSS (410,3)

Cpar1 1 0 9.60432f
Cpar2 2 0 9.60432f
**G.5 Single-Ended Ring Oscillator, \( N = 5 \) (\( W/L = 3.0/0.6 \mu\text{m} \))**

* Inverter (MOSIS Size) Ring Oscillator -- 05-Stage
* include typical.md

* NODE NAME ALIASES
* \( 1 = \text{VOUT (94,29.5)} \)
* \( 3 = \text{VSS (97,3)} \)
G.6 Single-Ended Ring Oscillator, $N = 31$ ($W/L = 3.0/0.6 \mu m$)

* Inverter Ring Oscillator -- 31-Stage

.include typical.md

* NODE NAME ALIASES
* 25 = VOUT (562,29.5)
* 27 = VDD (565,56)
* 29 = VSS (565,3)

Cpar1 1 0 15.45276f
Cpar2 2 0 15.45276f
Cpar3 3 0 15.45276f
Cpar4 4 0 15.45276f
Cpar5 5 0 15.45276f
Cpar6 6 0 15.45276f
Cpar7 7 0 15.45276f
Cpar8 8 0 15.45276f
Cpar9 9 0 15.45276f
Cpar10 10 0 15.45276f
Cpar11 11 0 15.45276f
Cpar12 12 0 15.45276f
Cpar13 13 0 15.45276f
Cpar14 14 0 15.45276f
Cpar15 15 0 15.45276f
<table>
<thead>
<tr>
<th>Cpar16</th>
<th>16</th>
<th>0</th>
<th>15.45276f</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cpar17</td>
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M2 32 33 27 27 PMOS L=600n W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
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VSS 29 0 DC 0

.IC V(25)=5
.TRAN 1n 11n
.PROBE
.END

G.7 Ideal Differential Ring Oscillator, N = 8

* 8-Stage Differential Ring Oscillator Model

.include typical.md

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R3 1 4 15K
R4 1 5 15K
R5 1 6 15K
R6 1 7 15K
R7 1 8 15K
R8 1 9 15K
R9 1 10 15K
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R12 1 13 15K
R13 1 14 15K
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I1 18 0 DC 66.67u
I2 19 0 DC 66.67u
I3 20 0 DC 66.67u
I4 21 0 DC 66.67u
I5 22 0 DC 66.67u
I6 23 0 DC 66.67u
I7 24 0 DC 66.67u
I8 25 0 DC 66.67u

.IC V(8)=5
.IC V(9)=4

.TRAN 1n 20n
.PROBE
.END

**G.8 DC Sweep of $I_{tail}$ vs. $V_{bias}$**

* NMOS Constant Current Source

.include typical.md

M1 1 2 0 0 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u

VD 1 0 DC 3
VG 2 0 DC 0

.DC VG 0.8 2 0.1
.PROBE
.END

**G.9 DC Sweep of $R_L$ vs. $V_{sd}$**

* PMOS Load Resistance

.include typical.md
M1 2 3 1 1 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
VD 1 0 DC 5
VS 2 0 DC 4
VG 3 0 DC 0
.DC VS 4 5 0.1
.PROBE
.END

G.10 Differential Ring Oscillator, \(N = 8\)

* Differential Inverter Ring Oscillator -- 08-Stage

.include typical.md

* NODE NAME ALIASES
* 6 = VSS (359,9)
* 9 = VPB (359,85)
* 21 = VOR (367,48)
* 22 = VOL (369,39)
* 23 = VDD (359,88)
* 25 = VNB (359,12)

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Cpar2 2 0 18.3195f
Cpar3 3 0 18.3195f
Cpar4 4 0 17.6016f
Cpar5 5 0 19.5462f
Cpar6 6 0 127.5072f
Cpar7 7 0 17.6016f
Cpar8 8 0 19.5462f
Cpar9 9 0 56.7336f
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Cpar11 11 0 18.3195f
Cpar12 12 0 18.3195f
Cpar13 13 0 18.3195f
Cpar14 14 0 17.6016f
Cpar15 15 0 19.5462f
Cpar16 16 0 17.6016f
Cpar17 17 0 19.5462f
Cpar18 18 0 19.5462f
Cpar19 19 0 18.3195f
Cpar20 20 0 18.3195f
Cpar21 21 0 47.9565f
Cpar22 22 0 43.4631f
Cpar23 23 0 261.41652f
Cpar24 24 0 17.6016f
Cpar25 25 0 29.5938f
Cpar26 26 0 17.6016f
Cpar27 27 0 19.5462f
Cpar28 28 0 19.5462f

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M41 6 25 1 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M39 22 9 23 23 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M38 21 9 23 23 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M37 5 10 4 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M36 5 3 2 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M35 6 25 5 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M34 8 7 10 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M33 8 11 3 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M32 6 25 8 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M31 15 14 7 6 NMOS L=1.5u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
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M26 3 9 23 23 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
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M13 14 9 23 23 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M12 13 9 23 23 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
M11 16 9 23 23 PMOS L=3u W=3u AD=5.4p PD=9.6u AS=5.4p PS=9.6u
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VNB 25 0 DC 1.78
VPB 9 0 DC 0

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.IC V(22)=4

.TRAN 1n 40n
.PROBE
.END

G.11 Differential Ring Oscillator, \( N = 16 \)

* Differential Inverter Ring Oscillator -- 16-Stage

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| Cpar25 25  0  18.3195f    |
| Cpar26 26  0  17.6016f    |
| Cpar27 27  0  17.6016f    |
| Cpar28 28  0  19.5462f    |
| Cpar29 29  0  19.5462f    |
| Cpar30 30  0  18.3195f    |
| Cpar31 31  0  18.3195f    |
| Cpar32 32  0  17.6016f    |
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| Cpar35 35  0  19.5462f    |
| Cpar36 36  0  17.6016f    |
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| Cpar38 38  0  18.3195f    |
| Cpar39 39  0  18.3195f    |
| Cpar40 40  0  17.6016f    |
| Cpar41 41  0  19.5462f    |
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G.12 Differential Ring Oscillator, \( N = 31 \)

* Differential Inverter Ring Oscillator -- 31-Stage

.include typical.md

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*  22 = VSS (1371,9)
*  61 = VNB (1371,12)
*  91 = VOL (1381,39)
*  92 = VDD (1371,88)
*  97 = VOR (1379,48)

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Vita

Evan Ross Shultz was born on November 16, 1979, in Metairie, Louisiana. He was graduated summa cum laude from Jesuit High School in New Orleans, Louisiana, in May 1998. He was graduated magna cum laude from Tulane University in New Orleans in May 2002 with the degree of Bachelor of Science in Electrical Engineering. He earned a Louisiana Board of Regents Dean’s Fellowship to pursue graduate study at Louisiana State University in Baton Rouge, where he is a candidate for the degree of Master of Science in Electrical Engineering. Evan is currently employed by Intel Corporation in Folsom, California, as a design validation engineer for flash memory products.