A programmable CMOS decimator for sigma-delta analog-to-digital converter and charge pump circuits

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A PROGRAMMABLE CMOS DECIMATOR FOR SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER AND CHARGE PUMP CIRCUITS

A Thesis

Submitted to the Graduate Faculty of the Louisiana State University and Agricultural and Mechanical College in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

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by
Raghavendra Reddy Anantha
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Abstract

Programmable Decimator for Sigma-Delta Analog-to-Digital Converter

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16.

Charge Pump Circuits

The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V – 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.
Chapter 1

Introduction

Advances in the integrated circuit (IC) technology have paved way for more compact and efficient implementation of digital logic on silicon chip. This indeed moved many types of signal processing to the digital domain. One of the major applications of this phenomenon is in sigma-delta analog to digital converter (ADC). Sigma-delta ADC is a low-cost, low-bandwidth, low-power, high-resolution ADC and has varied applications in data acquisition, communications, signal processing and instrumentation. A sigma-delta ADC comprises of a modulator, which is analog in implementation and a digital decimator stage. The decimator which is a crucial part of a sigma-delta ADC, relaxes the requirement for high precision analog circuits required for the modulator stage and also increases the final output resolution of the ADC. This work focuses mainly on the design and implementation of the decimator.

In modern integrated circuit (IC) technology, the current trend is toward decreasing device dimensions for operating at reduced supply voltages. However, circuits are needed which require operating voltages greater than the supply voltage. Higher operating voltages are required for EEPROM and flash memories. Single power EEPROM needs voltages in the range of 10-20 V. To drive LCD screens, LCD driver circuits are used to generate voltages in the range of two to four times the supply voltage. Bio-medical devices performing Functional Neuromuscular Stimulation (FNS) require high voltage electrical signals for treating neurological disorders in a human body. In this work, new charge pump circuits are proposed based on a simple and new proposed technique of internal clock voltage boosting. The developed technique has also been applied in Bio-implantable Electrical Stimulation System (BESS) used for FNS.
The thesis is organized into two parts. Part I presents the programmable decimator design for sigma-delta analog-to-digital converter and part II discusses about the new charge pump circuits and also a chip designed for BESS.

1.1 Motivation for Programmable Decimator for Sigma-Delta ADC (Part I)

In sigma-delta analog-to-digital converter (ADC), which is known as high resolution ADCs, the requirement for precise and complex analog circuitry has been relaxed by using dedicated digital signal processing techniques [1, 2]. Integrating an analog modulator with a digital decimator forms a sigma-delta ADC. The digital signal processing is done at the decimator stage, which is a decimation filter that performs the operation of down sampling a high frequency, low-resolution digital output of the modulator to nyquist rate, high-resolution digital output [3, 4]. The decimation stage which is responsible for achieving higher resolution and able to program a decimator offers further advantage of operating the ADC at different input channel bandwidths and with different oversampling ratios [5].

The output resolution of the ADC depends directly on the oversampling ratio. Increase in oversampling ratio increases the output resolution. But digital signal processing of oversampled signals requires large silicon area due to the requirement for more memory circuits and also incurs higher power dissipation as it places a requirement for fast switching circuits [5, 6]. Hence it is of significant advantage to have a single decimator that can be programmed to generate different resolutions for different oversampling ratios. Decimators have been implemented in any one of the following three ways: hard-wired, programmable read only memory (ROM) [7, 8] and field programmable gate arrays (FPGA) [9, 10]. The later two implementations require a programmable ROM to provide the filter coefficients for performing the decimation and thus making it difficult to build a stand-alone sigma-delta ADC. The motivation behind the present
work to design and implement a programmable CMOS ADC, with a focus on decimator design is to achieve two different resolutions for two different oversampling frequencies. An external sampling clock is used to operate both the modulator and the decimator stage, which will provide the flexibility to operate the ADC with different input signal bandwidths. The research goals are summarized below.

- Achieve an area efficient decimator design so as to form a stand-alone sigma-delta ADC by integrating the decimator with the existing modulator.

- Design a programmable decimator that can be programmed to generate a 10-bit and a 7-bit digital output depending upon the oversampling ratio of 64 and 16, respectively, set at the modulator stage.

- Develop circuitry that enables the programmability of the decimator and also design an internal clock divider circuit, which generates two down sampling clock signals for achieving two different resolutions.

- Design the decimator for operating from 0 to 5 V to integrate with modulator design operated from -2.5 V to +2.5 V.

1.2 Motivation for New Charge Pump Circuits (Part II)

Charge pump circuits are widely used for applications in integrated circuits [11, 12, 13], MEMS [14] and bio-medical applications [15] to generate higher output DC voltages. A charge pump is a DC-to-DC converter, which provides an output voltage higher than the supply voltage. A charge pump circuit can be designed using capacitors or inductors. But since the fabrication of an efficient inductor in IC technology is cumbersome, charge pump circuits based on capacitors are widely designed and used. In this work, capacitor based charge pump designs are discussed. Increased output voltages are obtained in a charge pump as a result of transferring charges to a capacitive load in alternate clock cycles [16]. In literature, different charge pump architectures have been presented starting with the Dickson charge pump design [16] to charge pump circuit with charge transfer switches [17] to voltage doublers [18] to the area efficient cross coupled
structures [12]. Dickson charge pump design is the simplest charge pump design to achieve higher output voltages and many reported designs use this technique. The charge pump designs [12, 17, 18, 19] have specifically concentrated on removing the threshold voltage drop existed in the Dickson design. But in this work, focus is on designing charge pump circuits which target the amplitude of the complementary clocks required for the charge pumping operation, so that higher DC output voltages can be achieved.

The research goals of the charge pump circuits are as follows:

- Develop a technique of internal clock voltage boosting.
- Design a four-stage and a six-stage charge pump circuits to generate higher output voltages compared to the reported charge pump design output voltages.
- Achieve an area efficient circuit with simple architecture.
- Generate higher clock voltages using the designed charge pump circuits.
- Design a circuit for generating higher clock voltages based on the developed technique of internal clock voltage boosting.

The other motivation to develop the proposed technique of internal clock voltage boosting is to overcome the charge leakage problem associated with the Bio-implantable Electrical Stimulation System (BESS) chip [15]. A modified BESS chip has been designed which uses a technique of internal clock voltage boosting to generate pulses of amplitude 10 V from a 3.7 V battery. There is also a requirement to design a battery switching circuit to alternate the power supply connection between the two batteries used by the previous BESS chip [15] and design a dual polarity pacing circuit to alternatively trigger the two connected electrodes. The later two circuits have to be designed to complement the BESS chip for full functionality.

The thesis is organized into two parts as mentioned above. Part I discusses the programmable CMOS decimator for a sigma-delta ADC. This part consists of five chapters (2 –
Chapter 2 introduces sigma-delta ADC operation, Chapter 3 presents with the decimation theory. Chapter 4 discusses the design, layout and simulation results of the decimator and also discusses the feature of programmability inside the decimator. Experimental results of the sigma-delta ADC are presented in Chapter 5 followed by the conclusion in Chapter 6. Part II discusses the new charge pump circuits and the redesigned BESS chip in Chapters 7 and 8, respectively. Chapter 7 gives an overview on the charge pump circuits reported in literature, presents with the proposed charge pump designs, their layout and simulation results. The experimental results and charge pump conclusion are presented in the later part of Chapter 7. Chapter 8 discusses the problems existed in the older BESS chip and the modified BESS chip designed to overcome problems associated with the older chip. The chapter also discusses the design, layout, simulation and experimental results of the redesigned BESS chip and conclusion of the BESS chip is presented at the later part of the chapter. Finally, Chapter 9 presents with the summary of the complete thesis work. Appendix-A summaries SPICE3 MOS model parameters used in circuit simulation. The pin diagrams of the decimator IC, modified BESS IC and the IC containing charge pump circuits are presented in Appendix-B.
PART–I: Programmable Decimator for Sigma-Delta ADC
Chapter 2

Sigma-Delta ADC Overview

2.4.1 Sigma-Delta ADC

Analog-to-digital converters can be categorized into two types depending upon the sampling rate [20]. The first kind samples the analog input at the nyquist frequency $f_n$ such that $f_s = f_n = 2 \times B$, where $f_s$ is the sampling frequency and $B$ is the bandwidth of the input signal. The second type of ADCs samples the analog input at much higher frequencies than the nyquist frequency and are called oversampling ADCs [21], sigma-delta ADCs come under this category. In sigma-delta ADC, the input signal is sampled at an oversampling frequency $f_s = K \times f_n$ where $K$ is defined as the oversampling ratio and is given by

$$K = \frac{f_s}{2B} \quad (2.1)$$

The block diagram of a sigma-delta ADC is shown in Fig. 2.1. The modulator samples the analog input signal at much higher frequencies set by the oversampling ratio and converts the analog input signal into a pulse density modulated digital signal containing both the original input signal and the unwanted out-of-band noise [21]. A decimation filter following the modulator filters out the out-of-band noise. Both the modulator and the decimator are operated with the same oversampling clock. In Fig. 2.1, the modulator shown is of first order with a 1-bit quantizer and generates a 1-bit output. The output of the decimator is shown as N-bit digital data, where $N$ is the output resolution of the ADC and is dependent on the oversampling ratio. The order of the decimator depends on the order of the modulator. Usually the order of the decimator is one more than the order of the modulator.
Figure 2.1: Block diagram of a sigma-delta analog to digital converter.
2.2 Modulator

The modulator is the analog part of a sigma-delta ADC. The final output resolution of the ADC is dependent on the order of the modulator and also the oversampling ratio set at the modulator stage. Since the modulator uses the principle of oversampling the need for anti-aliasing filter is eliminated and the analog input signal can directly be sampled using the oversampling clock [21]. Due to oversampling of the analog signal, the accuracy of the analog circuitry can be compromised with the speed [22]. The modulator pushes the quantization noise to higher frequencies, which can be filtered out using a digital low pass filter at the decimation stage. In the present work, a first order modulator has already been designed in CMOS using floating gate MOSFETs as differential amplifiers [10]. The modulator outputs a 1-bit oversampled digital data, which is applied as an input to the decimator. The basic block diagram of the modulator design is shown in Fig. 2.2. The difference between the analog input and the output of a digital-to-analog converter (DAC) is applied to an integrator, which is quantized to generate a pulse density modulated 1-bit digital output.

2.3 Decimator

The process of digitally converting the sampling rate of a signal from a given higher rate \( f_s \) to a lower rate \( f_n \) is called decimation [3]. Decimation in strict sense means reduction by 10 percent but in signal processing decimation means a reduction in sampling rate by any factor [4]. Basically a decimator is a digital low pass filter, which also performs the operation of sample rate reduction. The sigma-delta modulator does operation of noise shaping and hence the noise is pushed to higher frequencies so that the decimation stage following the modulator can filter out this noise above the cutoff frequency, \( f_n \).
Figure 2.2: Block diagram of a first-order modulator [21]. $X(z)$ is the analog input signal, $A(z)$ is the transfer function of the integrator and $N(z)$ is the noise transfer function, $Y(z)$ represents the output signal. DAC in the feedback loop is a 1-bit digital-to-analog converter.

$A(z) = \frac{z^{-1}}{1 - z^{-1}}$
The band limited signal can then be resampled by discarding $K - 1$ samples out of every $K$ samples, where $K$ being the oversampling ratio. By averaging $K$ samples out of the quantized sigma-delta output, the decimation filter achieves a high output resolution and also the frequency of the output data is at twice the input signal bandwidth which is the nyquist rate.

2.4 Literature Survey

The decimator occupies a large area on a chip and is difficult to implement in hardware form. A large number of related publications have concentrated on explaining the mathematical model and theory of decimation [3, 23]. A significant amount of work has been done on sigma-delta ADCs starting from a first order modulator to multi-order modulator designs [24, 25] but not much has been mentioned on implementations schemes of decimators.

Decimation is an important principle in digital signal processing and was initially implemented using an accumulate and dump circuit [26, 27] which also acts as a digital low pass filter. These circuits have poor attenuation of signal in stop band and also degrade the signal in pass band [28]. The accumulate and dump circuits also have the problem with register overflow. In order to have a sharp attenuation at the cut off frequency, the need for efficient digital filters has become a stringent condition. Optimal low pass digital filters can be designed using Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filters but hardware implementation of these filters is very cumbersome. An optimal low pass digital filter to have sharp transition between the pass band and stop band requires large number of taps. Each tap contains memory and multiplier circuits to store and multiply the filter coefficients with the input data. A hardware implementation of the multiplier and memory circuits consume a large silicon area causing the problems with the real estate. To overcome the problem with the area of implementing the optimal digital filters, many decimators use ROM devices to store and perform the coefficient
multiplication operation [8]. The use of ROM imposes complication in building a stand-alone analog-to-digital converter. One useful way of implementing the decimators is by using Cascaded Integrator Comb (CIC) filters [29]. These filters are area efficient for hardware implementation and also have satisfactory digital low pass filter characteristics. Due to these reasons, the CIC filter has become a prominent way of implementing the decimators for sigma-delta ADC. In literature different architectures have been reported both for area efficiency and performance efficiency [29, 30]. In this work, an area efficient CIC filter has been implemented which can as well be programmed to work for two different resolutions.
Chapter 3

Decimator Theory and System Description

3.1 Decimator Theory

Decimation is the processes of lowering the word rate of a digitally encoded signal, which is sampled at high frequencies much above the nyquist rate. It is usually carried out to increase the resolution of an oversampled signal and to remove the out-of-band noise. In a sigma-delta ADC, oversampling the analog input signal by the modulator alone does not lower the quantization noise; the ADC should employ an averaging filter, which works as a decimator to remove the noise and to achieve higher resolutions. A basic block diagrammatic representation of the decimator is shown in Fig. 3.1.

The decimator is a combination of a low pass filter and a down sampler. In Fig. 3.1 the transfer function, \( H(z) \) is representative of performing both the operations. The output word rate of the decimator is down sampled by the factor \( K \), where \( K \) is the oversampling ratio. The function of low pass filtering and down sampling can be carried out using an averaging circuit. The transfer function of the averaging circuit is given by equation (3.1). It establishes a relation between the input and output functions [28].

\[
H(z) = \frac{Y(z)}{X(z)} = \frac{1}{k} \sum_{x=0}^{k-1} z^{-x}
\]

(3.1)

\[
H(z) = \frac{1}{K} \frac{1 - z^{-k}}{1 - z^{-1}}
\]

The averaging circuit defined by the equation (3.1) averages every \( K \) samples. By converting the \( z \)-domain transfer function into the frequency domain the characteristics of the circuit can be plotted. The frequency response of the decimator is given by equation (3.2) and the plot of the frequency response of the filter is shown in Fig. 3.2 [28].
Figure 3.1: Basic block diagram of a decimator.

Figure 3.2: Frequency response of a sync averaging filter.
The frequency response of the averaging circuit, which is used as a decimator, is similar to that of a sync filter [28]. A sync filter is a digital low pass filter which can be used to filter out the high frequency noise from the modulated input signal.

\[
H(f) = \frac{\sin c(K\pi \frac{f}{f_s})}{\sin c(\pi \frac{f}{f_s})}
\]  

(3.2)

The signal band of interest is the range of frequencies from 0 to the signal bandwidth \((f_s/2K)\) and the sync filter attenuates any signal above the nyquist rate \((f_s/K)\), removing the out-of-band noise. In order for the decimator to satisfy the digital low pass filter characteristics the attenuation in the stop band should be high. The ratio of the main lobe to the side lobe forms a critical factor in designing a decimator. The filter characteristics can be improved to have sharp transition between the pass band and stop band and also good attenuation in the stop band by cascading the decimation stages. In Fig. 3.2, the gain of the filter is given by the value \(K\). Increasing the value of \(K\) simply means increasing the final output resolution and has no direct significance on the frequency response. The decimator averages every \(K\) samples and has an output at every \(K^{th}\) sample. As defined earlier, \(K\) is the oversampling ratio and since the output occurs at every \(K^{th}\) sample, the output rate of the decimator is \(f_s/K\). The input to a decimator is the sequence of bits of 1’s and 0’s and since the averaging operation involves the addition of these bits, the output resolution increases due to the addition of every \(K\) number of bits. As the \(K\) value increases the output resolution also increases. The relation between the number of bits increased to the oversampling ratio \(K\) for a sigma-delta ADC is given by equation (3.3) [28].

\[
N_{inc.} = \frac{30 \log K - 5.17}{6.02}
\]  

(3.3)
The final output resolution of the decimator not only depends on the oversampling ratio but also on the input resolution. The output of the modulator is applied as an input to the decimator but the output resolution of the modulator depends on the order of the modulator designed. In this work, a first order modulator is considered, hence the output of the modulator is a 1-bit digital data. The final resolution of the decimator or the sigma-delta analog-to-digital converter is given by equation (3.4) [28],

\[ N_{\text{final}} = N_{i/p} + N_{\text{inc}} \]  

(3.4)

where \( N_{\text{final}} \) is the final output resolution, \( N_{i/p} \) is the input resolution of the decimator and \( N_{\text{inc}} \) is the increase in resolution achieved by the decimator.

In the present work, the decimator is designed to form a sigma-delta ADC by cascading it with an already designed modulator. The designed modulator is of first order and hence based on the following equation (3.5), the order of the decimator has to be two [28].

\[ L = 1 + M \]  

(3.5)

In equation (3.5), \( L \) is the order of the decimator and \( M \) is the order of the modulator. The complete transfer function of the decimator of order \( L \) is given in equation (3.6).

\[
H(z) = \left( \frac{1}{K} \frac{1 - z^{-k}}{1 - z^{-1}} \right)^L
\]  

(3.6)

Higher order decimators can be designed by cascading single stage decimation stages. By designing a second order decimator improvement in filter characteristics is achieved.

3.2 Literature Review on Decimation Filters

As discussed in Sec. 3.1, a basic decimator is an averaging circuit which can be implemented using the sync filter. One way of implementation is by using an accumulate and dump circuit [21]. A simpler accumulate and dump circuit uses couple of latches, an adder circuit and a clock divider circuit. A latch is a register circuit used to store data. The adder circuit
performs the addition operation on the input bits and the bits stored in the input latches. The clock divider circuit generates a clock signal output at every KT seconds ($f_s/K$). This output of the clock divider circuit is used to trigger the output latch so that the sum stored in the input latch is transferred to the output latch. After the data transfer has occurred the input latch is reset. The complete operation of addition followed by transfer of data to the output latch at a frequency $f_s/K$ is termed as the averaging operation. A block diagram of an accumulate and dump circuit is shown in Fig. 3.3. The accumulate and dump circuit is a sync filter and also acts as a digital low pass filter. To achieve better attenuation in the stop band as discussed in Sec. 3.1 the cascading of decimation stages is necessary. Accumulate and dump circuit also has some serious limitations with cascading more number of stages [28] which are explained as follows.

The output of each stage occurs at a frequency of $f/K$ where $f$ is the input signal frequency of that stage. So by cascading $M$ number of stages the final output frequency coming out of the circuit is $f/(K^M)$. The output of a decimator should occur at twice the input signal frequency of the ADC. Since the output of the $M$ stage cascaded accumulate and dump circuit occurs at a frequency $f/(K^M)$ the input to the ADC should be at $0.5 f/(K^M)$. Due to this reason accumulate and dump circuit places a severe limitation on the input signal band width of the converter. The other ways of implementing the decimators is by using a digital low pass filter to filter out the out-of-band noise and then follow it with a decimator stage to reduce the output frequency to the nyquist rate. Digital filters can be designed using commonly known window techniques [4]. The filters designed using window techniques takes the specifications for the attenuation in stop band and pass band, the values for cut off frequency and transition band and gives an optimal solution with a large number of taps.
Figure 3.3: Block diagram of an accumulate and dump circuit.
The filter designed using the window techniques have better filter characteristics but have severe problem when implementing in hardware because of the number of taps the filters required. Tap is the order of the filter and each tap requires multiplier and adder circuits which take up a large space on silicon. The multiplier circuit is required to multiply the filter coefficients with the input data; the filter coefficients are stored in a memory element usually a ROM circuit. The decimator designed using this method consumes large silicon area and also requires ROM memory circuits, hence poses a severe limitation in implementing in hardware. These types of designs are used in high-end applications which require sharp filter characteristics.

The above problems can be solved by using a Cascaded Integrator Comb (CIC) filter. The CIC filters are most economical when implementing in hardware [29] and have better filter characteristics compared to the accumulate and dump circuit. The following section gives a detailed description about the CIC filter and its advantages.

3.3 Cascaded Integrator Comb (CIC) Filter Theory

The CIC filter is a combination of digital integrator and digital differentiator stages which perform the operation of digital low pass filtering and decimation. The CIC filters do not require any multiplier circuits and hence are very economical for implementation in hardware and the problems with cascading faced by the accumulate and dump circuit are also overcome with the CIC design. Equation (3.7) gives the transfer function of the CIC filter in z-domain which is similar to equation (3.6) except the numerator term and the denominator terms are separated [28]. The numerator represents the transfer function of a differentiator and the denominator indicates that of an integrator.

\[
H(z) = \frac{1}{K^L} \cdot (1 - z^{-k})^L \left( \frac{1}{1 - z^{-1}} \right)^L
\]  

(3.7)
The transfer function of both the CIC filter and the accumulate and dump circuit are similar but the way both circuits are implemented are different. The CIC filter first performs the averaging operation then follows it with the decimation not like in accumulate and dump circuit where the averaging and decimation operations occur at the same time. A simple block diagram of a first order CIC filter is shown in Fig. 3.4. The hardware needed to implement the CIC filter shown in Fig. 3.4 is very significant because of the delay elements that are used in the differentiator stage. It can be seen that the differentiator circuit needs K delay elements. Usually the delays are implemented using registers. As will be discussed in the later sections that as the oversampling ratio increases, the number of delay elements also increases and as well the number of register bits that are used to store the data. The above design also requires another decimation circuit for decreasing the data rate, which requires additional hardware. Hence it becomes very cumbersome to design the differentiator with many delay elements. The problem with the area can be overcome by implementing a clock divider circuit in between the integrator and differentiator stages as shown in Fig. 3.5. The clock divider circuit divides the oversampling clock signal by the oversampling ratio K. By dividing the clock frequency by K the number of delay elements used in the differentiator can be reduced to just one. In Fig. 3.5, the integrator operates at the sampling clock frequency, $f_s$, while the differentiator operates at down sampled clock frequency of $f_s/K$. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved. In this research, the CIC filter based on this model has been designed.
Figure 3.4: First order CIC filter with a decimation stage.

Figure 3.5: Block diagram of a first order CIC filter without external decimation stage.
3.3.1 Digital Integrator

The integrator circuit is similar to an accumulator which is used to accumulate or store the sum of the input data. It is a single-pole Infinite Impulse Response (IIR) filter with a filter coefficient factor of one. The transfer function of the integrator is shown in equation (3.8) [28].

\[ Y(nT_s) = X(nT_s) + Y((n-1)T_s) \]

\[ H(z) = \frac{z}{z-1} \]

(3.8)

The output of the integrator is the sum of the present input and the past output as can be observed from the time domain representation equation (3.8). Based on equation (3.8), a stick diagrammatic representation of the digital integrator can be modeled and is shown in Fig. 3.6. The delay element is used to delay the output signal by one clock period and can be implemented using a memory element. A simple register can be used to achieve the delay. The transfer function in z-domain representation can be converted into a frequency domain by substituting \( Z \) with \( e^{2\pi(f/fs)} \). The magnitude response of the integrator is given by equation (3.9) and the plot showing the magnitude response of the integrator is shown in Fig 3.7 [28].

\[ |H(f)| = \frac{1}{\sqrt{2 \left(1 - \cos(2\pi \frac{f}{f_s})\right)}} \]

(3.9)

The magnitude plot of the integrator shows that the integrator has an infinite gain at DC and at multiples of the sampling frequency, \( f_s \). The integrator has a minimum value of 0.5 but the frequency of operation that is of interest is at \( f_s \). Since the gain is infinite at DC and at \( f_s \), it might cause the integrator to become unstable and there is every chance that the register used in the delay element could overflow causing data loss. In order to avoid problems with register overflow, two’s complement coding scheme is used.
Figure 3.6: Stick diagram of a digital integrator.

Figure 3.7: Magnitude response of a digital integrator.
By using the two’s complement method of coding, the data will not be lost even when the register overflow occurs. In accumulate and dump circuit, an accumulator is an integrator and since binary form is used, data loss could be possible. This is another advantage of the CIC filter as it avoids the data loss due to register overflow.

However, in using the two’s complement number representation, the data will not be lost due to register overflow unless the register used to store the data is long enough to store the largest word given by \( K \times 2^N \). Here \( N \) is the number of input bits to that particular integrator stage. Each integrator achieves an increase in resolution by \( \log_2 K \) bits. The register size of an integrator stage to avoid data loss is given by equation (3.10) [28].

\[
\text{Register size } M \text{ (in bits)} = \log_2 K + N
\] (3.10)

where \( N \) is the input bit resolution of that integrator stage. In order to boost the word size to that shown in equation (3.10) each integrator is preceded with a coder circuit. A coder circuit is a simple multiplexer circuit and is discussed in Chapter 4.

### 3.3.2 Digital Differentiator

A differentiator circuit also called as a comb filter is a Finite Impulse Response (FIR) filter. A comb filter is a digital low pass filter. The time domain and the transfer function of the differentiator are given in equation (3.11). From the time domain representation it can be explained that the output of the differentiator is the difference between the present input and the past input.

\[
Y(nT_s) = X(nT_s) - X((n-1)T_s)
\] (3.11)

\[
H(z) = \frac{Y(z)}{X(z)} = (1 - z^{-1})
\]
Based on equation (3.11), the stick diagram of the differentiator can be modeled and is shown in Fig. 3.8. The transfer function is converted into the frequency response and the expression for the magnitude response is given by equation (3.12) [28]. The plot of magnitude response of the differentiator is shown in Fig. 3.9. The two’s complement output of the integrator is applied as the input to the differentiator, and so the differentiator also uses the two’s complement scheme of coding.

\[ |H(f)| = \sqrt{2\left(1 - \cos 2\pi \left(\frac{f}{f_s}\right)\right)} \]  

(3.12)

The final output of the decimator which is the output of the differentiator circuit has to be in binary form for further signal processing. So the two’s complement output is converted back to the binary form. It should be noted that the differentiator operates at a different clock frequency compared to the clock frequency of the integrator as explained above. Because of this, both the circuits act as individual blocks and can be used for cascading in order to form a cascaded integrator comb filter.

3.3.3 Multi-Order CIC Filter

As explained above a CIC filter is formed by cascading the digital integrator and the digital differentiator. In order to have better filter characteristics higher order CIC filter is designed based on equation (3.5). In the present work, a second order CIC filter is designed, its block diagram of it is shown in Fig. 3.10. The filter has a second order integrator and a second order differentiator circuits separated by a clock divider circuit. The integrator stage and the differentiator stage operate at different frequency. The complete block diagram of the second order CIC decimation filter implementation is shown in Fig. 3.11.
Figure 3.8: Stick diagram of a digital differentiator (comb filter).

\[ Y(z) = (1 - z^{-1}) X(z) \]

Figure 3.9: Magnitude response of a digital differentiator.

Figure 3.10: Block diagram of a second order CIC filter. Note: Two’s complement output of the decimator is converted into binary output.
Figure 3.11: Block diagrammatic implementation of a second order CIC filter. Note: The oversampling ratio, $K = 64$. 
In the present work, the input to the decimator, which is the output of the modulator, is a 1-bit oversampled binary signal. The decimator shown is for an oversampling ratio set at K=64. The same design can be used for an oversampling ratio of 16 with the help of a circuit for programmability. The circuit for programmability is not shown in Fig. 3.11 but is discussed in chapter 4. The operation of the design is explained by considering K=64 and similar references are made for K=16 with out loss of generality. In the differentiator circuit, the difference operation is implemented by performing the summation of first input sequence and the complement of the second input sequence.

The coder circuits are responsible for achieving the increase in resolution. As discussed earlier in Sec. 3.3.1, equation (3.10) shows that each integrator should have a register size of \( \log_2 (K + N) \) and each integrator stages increase the resolution by \( \log_2 K \) bits. So a coder circuit is used to encode the input data to the respective resolution. In Fig. 3.11, the coder circuit-1 before the first integrator stage boosts the 1-bit input to 7-bit data. Since \( K = 64 \), the increase in resolution is 6-bits (\( \log_2 64 \)). Hence integrator-1 works with 7-bit data. In a similar way, integrator 2 works with 13 bits of data. The two coder circuits not only increase the resolution but also convert the binary data into two’s complement data.

In order to convert the 1-bit binary data input of the coder circuit-1 to 7-bit two’s complement form, the representation shown in equation (3.11) is used.

\[
1 − 0000001 \quad (+1 \text{ in two’s complement}) \\
0 − 1111111 \quad (-1 \text{ in two’s complement})
\]

(3.11 a)  
(3.11 b)

Similarly, the input to the coder circuit-2 which is the output of integrator 1 is 7-bits and these 7-bits are converted to two’s complement 13-bits of data. This is achieved by complementing the MSB bit which is bit-7 and substituting the complemented value in bits 7 through 13. The bit
information is clearly shown in Fig. 3.11. For K=16 case, integrator-1 boosts the bit resolution from 1-bit to 5-bit using similar method of coding scheme as defined in equation (3.11) and is shown in equation (3.12).

\[1 – 00001 \text{ (+1 in two’s complement)}\]  \hspace{1cm} (3.12 a)

\[0 – 11111 \text{ (-1 in two’s complement)}\]  \hspace{1cm} (3.12 b)

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two’s complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios. The detailed explanation and hardware implementation of the programmable decimator circuit is presented in Chapter 4.
Chapter 4

Decimation Filter Design and Implementation

4.1 Decimation Filter Design

In this work, the design of a decimation filter is presented for integrating with an existing designed modulator [10] to form a complete sigma-delta ADC. The specifications for the decimator are to achieve a 10-bit output resolution for an input signal of 1-bit data. The input to the decimator is a 1-bit pulse density modulated output from the modulator. A fixed hardware implementation of the decimator has been done in 1.5 µm n-well CMOS technology. The decimator can be operated with two oversampling ratios of 64 and 16 and achieves an output resolution of 10-bit and 7-bit, respectively. A simple design block diagram of the CIC filter, used as a decimator, is shown in Fig. 4.1 and illustrates the hardware implementation blocks of the design.

4.2 Level Shifter Circuit

A level shifter circuit is used to provide the level shift in the voltage range from -2.5 V to +2.5 V to 0 V to 5 V. It is at the input end of the decimator and forms the interface between the modulator and the decimator. The available modulator operates within a voltage range of ±2.5 V for the purpose of biasing the operational amplifier and setting the reference voltage at 0 V. The decimator is a digital circuit and designed to work in the 0 to 5 V range. Since the output of the modulator is in the ±2.5 V, it becomes necessary for having a circuit at the input stage of the decimator which can provide the necessary shift in the voltage level. The transistor level schematic of the level shifter circuit is shown in Fig. 4.2. The circuit shown is a simple buffer circuit.
Figure 4.1: Block diagram showing the internal circuits used in the decimation filter design.

Figure 4.2: Transistor level schematic of the level shifter circuit.
The input inverter has been modeled such that the output of that inverter is 0 V when the input is +2.5 V and the output is 5 V when the input is –2.5 V. The first inverter output is given as the input to the second, so when ever the input to the level shifter circuit is +2.5 V the second inverter output is 5 V and when ever the input is –2.5 V the second inverter output is 0 V. When the input is +2.5 V, both the NMOS (M1) and PMOS (M2) transistors are in the ON state putting the output node A at an intermediate value between 0 V and 5 V. To avoid this situation the W/L ratio of the NMOS transistor has been increased such that the output goes to 0 V. Thus by increasing the W/L ratio of M1 the pull down strength of the NMOS transistor is increased. When the input voltage is -2.5 V, NMOS transistor is OFF and PMOS transistor turns ON strongly pulling up the output node A to 5 V.

Figure 4.3 shows the layout of the level shifter circuit and SPICE simulation results are shown in Fig. 4.4. From the layout shown in Fig. 4.3, it can be observed that the W/L ratio of the NMOS transistor, M1 is comparatively large with respect to the other transistors. From the simulation results shown in Fig. 4.4, the circuit achieves the output voltage 0–5 V from a ±2.5 V input.

4.3 Clock Divider Circuit

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency $f_s/K$, where $f_s$ is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies $f_s/64$ and $f_s/16$. 

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Figure 4.3: Layout of the level shifter circuit.

Figure 4.4: SPICE simulated input and output of the level shifter circuit.
The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q’ output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

4.3.1 Clock Division by a Ratio of 64 and 16

In order to have an area efficient clock divider circuit, a single circuit has been designed which can provide clock frequency division by two K values of 64 and 16. The output of a single stage T-flip flop for a clock input of frequency f is a clock of frequency f/2. By cascading more number of T-flip flop stages, the clock frequency can be reduced in multiples of 1/2. Thus N-stage cascaded T-flip flop provides with a frequency division by a value of 2^N. The final output of the cascaded design will have the same duty cycle as that of the input clock. In the present
application, the differentiator circuit has to be operated with a clock such that the difference between two pulses should be $K \times T_s$, where $T_s$ is the time period of the oversampling clock signal. A representative output of the clock divider circuit that has to be applied to the differentiator circuit is shown in Fig. 4.6 and illustrates the frequency division by $K$. The output has an ON time same as that of the oversampling clock ON time of $T_s/2$ sec. The output pulses are separated by $K$ samples i.e., in between two pulses there exists $K$ samples since each sample with a time period of $T_s$.

To generate clock output as shown in Fig. 4.6, the circuit shown in Fig. 4.7 is designed and shows the gate level schematic of the clock divider circuit that is used to generate two different output pulses with a clock frequency division by 64 and 16, respectively. To achieve a frequency division by 64 and 16, 6-stage and 4-stage T-flip flops are required. But to make the design area efficient, a single cascaded 6-stage T-flip flop design is taken into consideration as shown in Fig. 4.7. When ever the input and output of a T-flip flop are given as inputs to an AND gate, only the ON time of the input clock is transmitted and the output of the AND gate remains at logic ‘1’ during that time. The operation of clock divider circuit is explained with respect to $K = 16$ and the operation for $K=64$ case can be understood in similar lines. For the divide by 16 case, the output of the T-ff 4 and the output of the T-ff 3 is given as inputs to AND 10. The output of AND 10 is at logic 1 during the ON time of the T-ff 3 output. This output is applied as one input to AND 9; the other input is from the output of T-ff 2. The output of AND 9 remains at logic 1 only during the ON time of the T-ff 2 output. The operation is continued and the final output obtained from the AND 7 is a pulse waveform with the pulses separated by $16 \times T_s$. The detailed operation of the clock divider circuit for the divide by 16 case is clearly shown in Fig. 4.8.
Figure 4.5: Figure showing the conversion from D-flip flop to a T-flip flop.

Figure 4.6: Representative output of the clock frequency divider circuit. Note: K can be 64 or 16.
Figure 4.7: Gate level schematic of the clock divider circuit.
Figure 4.8: Waveforms illustrating the operation of the clock divider circuit for the divide by 16 case.
The operation of divide by 64 case can be explained in similar lines. The output is a sequence of pulses which are separated by 64 samples, i.e., the time difference between two consecutive samples is $64 \times T_s$, where $T_s$ is the time period of the input clock. The output pulse ON time in both the cases of divide by 16 and 64 is same as the pulse ON time of the input oversampling clock.

The layout of the complete clock divider circuit for generating both the divide by 64 and divide by 16 outputs is shown in Fig. 4.9. The T-flip flops which are designed using the D-flip flop have been implemented using the NAND gates. The W/L ratios of the NMOS and PMOS used in the design are of values $25.6/1.6$ and $12.8/1.6$, respectively. The AND gates are also designed using the same W/L ratios. The reason for using slightly higher ratios is to achieve a sharp rise and fall times in the clock output waveform and also to better drive the loads. Since the higher values of W/L ratios are considered, care is taken in the layout to avoid latch up. The latch up is avoided by laying out more contacts on the source/drain and the metal lines [31].

The simulated output for the clock frequency division by the oversampling ratio of $K=16$ taken from the output of AND 7 gate of Fig. 4.7 is shown in Fig. 4.10 which also shows the input clock whose time period is chosen to be $1 \, \mu s$. The obtained output pulses are separated by $16 \, \mu s$ ($16 \times 1 \, \mu s$) illustrating input clock frequency division by a factor 16. Figure 4.11 shows the simulation results for $K=64$ case. The obtained output pulses are separated by $64 \, \mu s$ ($64 \times 1 \, \mu s$) illustrating input clock frequency division by a factor 64.
Figure 4.9: Layout of a clock divider circuit for generating two outputs.
Figure 4.10: Simulated output of the clock divider circuit for divide by 16 case. The time period of the input clock is 1 μs.

Figure 4.11: Simulated output of the clock divider circuit for divide by 64 case. The time period of the input clock is 1 μs.
4.4 Adder Circuit

Addition forms the basis for many signal processing techniques. Adder is a very crucial circuit in implementing the decimator. The adder circuit is extensively used in both the integrator and the differentiator stages and is used to perform the addition operation on the input bits. A binary full adder circuit is used for the addition operation and its truth table is shown in Table 4.1. The table contains two input bits A and B. $C_{in}$ is the carry from the earlier stage and the output of the adder are the sum bit and the carry bit $C_{out}$. The Sum and $C_{out}$ bits shown in the truth table are defined using equation (4.1).

Table 4.1: Truth table of a binary full adder

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>$C_{in}$</th>
<th>Sum</th>
<th>$C_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[
\text{Sum} = A \oplus B \oplus C \\
C_{out} = AB + BC_{in} + AC_{in} \tag{4.1}
\]

The hardware implementation of the above equation can be done in different forms. Careful optimization of the adder circuit is required for optimum operation. The optimization can be done both at the logic level and at the circuit level. Logic level optimization is done by
optimizing the Boolean equation defined above so that a faster circuit can be designed by reducing the min terms [32]. Optimization at circuit level is achieved by reducing the number of transistors to achieve an area efficient design. In both of the optimizations, a trade off between the area and speed of operation exist. In the present work, a binary full adder circuit is designed which is area efficient and uses the minimum number of transistors. Since the operation of the ADC is not at very high frequencies, area becomes the critical specification in the design of the adder circuit. Different architectures have been developed in literature depending upon the area and speed specifications.

The adder circuit used for the decimator has been designed using transmission gates. The transistor schematic of the adder circuit is shown in Fig. 4.12. Transmission gate based design is used because the design has the minimum number of transistors. A total count of 18 transistors is used in the design of the adder [31]. Since the decimator uses adder circuit in every bit operation, optimizing the adder yields an area efficient design. Figure 4.12 also shows the W/L ratios of each transistor. Transistors with constant and higher W/L ratio are used to reduce the internal propagation delay that could exist during the transmission of the signal to the output. The technique of lowering the delay through the circuit by properly sizing the transistors is called transistor sizing [32]. Transistor sizes can be calculated by considering the worst case path in which maximum delay can occur. Parasitic capacitances exist at each node and the transistor at that node should be sized such that the time it takes to charge or discharge that capacitor is minimized. In the adder circuit of Fig. 4.12, the worst case path for maximum delay exists from the input to the C_{out} and the path can be illustrated using parasitic resistance and capacitors as shown in Fig. 4.13. The transistors M2, M4, M6 and M8 with their associated parasitic resistance and capacitors constitutes for the delay.
Figure 4.12: Circuit diagram of an 18 transistor binary full adder.

Figure 4.13: R-C model for illustrating the transistor sizing.
In Fig. 4.13, R_{1,2} to R_{7,8} are the parasitic resistance associated with transistors from M1 to M8 and C_{1,2} to C_{5,6} are the parasitic capacitances of transistors M1 to M6 respectively. The output capacitance of C_{out} is shown with load capacitor C_L. The propagation delay based on Elmore delay model \([32]\) is given by equation (4.2).

\[
\tau_{\text{Elmore}} = 0.69 R_{1,2} C_{1,2} + (R_{1,2} + R_{3,4}) C_{3,4} + (R_{1,2} + R_{3,4} + R_{5,6}) C_{5,6} + (R_{1,2} + R_{3,4} + R_{5,6} + R_{7,8}) C_L
\]  \hspace{1cm} (4.2)

In equation (4.2) R_{1,2} appears in all the RC time constant terms and R_{3,4} appears three times and R_{5,6} appears two times. So in order to decrease the delay, the resistance has to be decreased. The resistance of a transistor can be decreased by increasing its W/L ratio. By making all the resistances equal to one common value R, equation (4.2) can be written as shown in equation (4.3).

\[
\tau_{\text{Elmore}} = 0.69 R [C_{1,2} + 2C_{3,4} + 3C_{5,6} + 4C_{7,8}]
\]  \hspace{1cm} (4.3)

By using a constant large value of W/L ratio for all the NMOS and for all PMOS transistors the resistance can be decreased and also the delay through the circuit.

In the adder circuit shown in Fig. 4.12, the transistor combination formed by transistors M1 through M6 performs the XOR operation taken at node Y. The operation of the XOR gate formed by using these six transistors is explained as follows. When signal A is high, node X is low disconnecting the transmission gate formed by transistors M5 and M6 and signal B appears at node Y as \(B\). When signal A is low, node X is high disconnecting the inverter formed by transistors M3 and M4 and signal B appears at node Y.

The sum output in Fig. 4.12 obtained from the two transmission gates formed by transistors M11 through M14 is given by \(A \oplus B \oplus C_{\text{in}}\) where \(C_{\text{in}}\) is the carry input. The carry output \(C_{\text{out}}\) is equal \(C_{\text{in}}\) when \(A \oplus B\) is HIGH and \(C_{\text{out}}\) is either A or B when ever \(A \oplus B\) is LOW.
as revealed from the adder truth table given in Table 4.1. This adder uses minimum number of transistors and has equal Sum and Carry delay times.

The layout of the area efficient adder circuit is shown in Fig. 4.14. Here in the layout the output carry bit \( C_{\text{out}} \) of the adder is applied as the input carry \( C_{\text{in}} \) to the next adder. If all the three inputs to the next adder are not applied at the same time, glitches can exist in the output. Glitches occur due to the delay in the signal lines. The metal line connecting the \( C_{\text{out}} \) of the first adder to the \( C_{\text{in}} \) of the second adder is long then the metal can cause a delay in the carry bit. In order to avoid this problem, the \( C_{\text{out}} \) of the adder is placed such that it is close to the \( C_{\text{in}} \) of the next adder. Since a decimator circuit requires large number of adders i.e., it requires 46 adder circuits, hence it is very crucial to have the adder outputs with minimum delays. The simulation results of the adder circuit are shown in Fig. 4.15. The input signal bit information shown in the simulation results is in accordance with the bit order shown for the input bits in the adder truth table. The results for Sum and \( C_{\text{out}} \) exactly match with that of the values for sum and \( C_{\text{out}} \) in the adder truth table in Table 4.1.

4.5 Delay Element

Delay element is a register circuit which is used to provide a delay by one clock period. The delay element can be implemented using a register structure which can store data. In the present work, the integrator and differentiator circuits of a 2nd order CIC filter requires 46 delay elements. From Fig. 3.11 of chapter 3, the integrator block alone requires 20 delay elements, 7 for the first stage and 13 for the second stage. The differentiator block requires 26 delay elements which are divided equally between the two differentiator stages. Hence it is very important to design a delay element which is area efficient and has smaller rise and fall times. A delay element can be implemented using a combination of switches and inverters.
Figure 4.14: Layout of the binary full adder circuit.

Figure 4.15: Simulation results showing the inputs and outputs of the adder circuit.
The circuit which is used to delay the input by an oversampling clock time period is shown in Fig. 4.16. The circuit is operated with an oversampling clock, which is used to alternatively transfer the data to the right. Simple NMOS switches are used for data transfer from left to right in alternate clock cycles. When clock signal is HIGH switch S1 is closed and the inverted input is available at node A. Since switch S2 is operated with $\overline{\text{clock}}$, it is open and no transfer occur through this switch. When ever the clock signal goes LOW, switch S1 is opened and the input is disconnected from the delay circuit. Now, $\text{clock}$ is HIGH so switch S2 is closed and the previous inverted input stored on the node A is inverted and transferred towards the node B. During the next cycle when clock is HIGH, the value stored on node B is transferred to the output and fed to the stages following the delay element. It can be observed that an input bit takes one clock cycle to reach to the output. Hence the delay element works fine in providing a delay by one clock period. The time delay is achieved by data transfer using two non-overlapping clock signals. But in practice, the two non-overlapping clocks exhibit clock skew, if the clock skew is large then the delay circuit does not work as delay element. To avoid this condition an NMOS switch based design is used here instead of a transmission gate based design. Since the transmission gates requires two non-overlapping clocks to work as a switch, the presence of clock skew can degrade the signal. By using NMOS switches, non-overlapping clocks should be applied to two different switches and the problem with the clock skew is neutralized with the delay of the inverters. The other advantage of the NMOS based design is that the use of buffer circuit at the output will give the delay circuit better driving capability in driving the loads connected to the circuit.

The layout of the delay circuit is shown in Fig. 4.17. The clock in the layout is represented with clock_inv. The simulation results of the delay element are shown in Fig. 4.18.
Figure 4.16: Transistor level schematic for achieving a delay by two clock cycles.

Figure 4.17: Layout of the delay circuit showing the input, output and power supply connections.

Figure 4.18: Simulated input and output of the delay circuit. Input clock frequency = 1 MHz.
The simulations are done with a clock input frequency of 1 MHz. From the Fig. 4.18 it can be observed that the output is same as the input except that the output is delayed by one clock time period (1 μs).

4.6 Integrator Block Design

A 2\textsuperscript{nd} order digital integrator is used in designing the 2\textsuperscript{nd} order CIC filter. The integrator is the main circuit for achieving increase in resolution. The block diagram schematic of a 2\textsuperscript{nd} order integrator circuit is shown in Fig 4.19 (a). Each one bit integrator circuit in both stages of the design is clocked with an oversampling clock of oversampling frequency $f_s$. A one bit integrator contains an adder circuit followed by a delay element as shown in Fig. 4.19 (b). The clock is used by the delay circuit to provide a delay in the adder output by one clock period. The output of the delay circuit is applied as one of the input to the adder circuit. The other inputs to the adder are the output from the coder circuit and the carry out of the preceding significant bit adder. The carry input for the least significant bit adder is taken as 0 and the carry out for the most significant bit adder is ignored. The integrator circuit shown in the Fig. 4.19 (b) is easier for implementation in hardware and is slightly different from the integrator shown in Fig. 3.6 in Chapter 3. The magnitude response of both the circuits is same and the only difference is the change in the phase response of the circuit.

As discussed in Chapter 3, each stage of the integrator stage increases the resolution by $\log_2 K$ bits. The 2\textsuperscript{nd} order integrator block shown in the Fig. 4.19 (a) works for both the oversampling ratios of 64 and 16. For $K = 64$ case, the first stage has an output resolution of 7-bits (1-bit input + $\log_2 64$) and second stage has an output resolution of 13-bits (7-bit first stage output + $\log_2 64$). Similarly for $K = 16$ case, first stage should have 5-bit output resolution (1-bit input + $\log_2 16$) and second stage should have an output resolution of 9-bits (5-bit first stage output + $\log_2 16$).
output + log₂16). So K = 16 case, 5-bit and 9-bit registers are needed from the designed 7-bit and 13-bit registers, respectively. This is achieved by using an additional circuit for programmability so that the same register set can be used for both cases of K. The coder circuit and the circuit for programmability are very important blocks in the integrator circuit and are explained below.

4.6.1 Coder Circuits

In the 2nd integrator circuit shown in Fig. 4.19 (a), two coder circuits were used for two integrator stages. Coder circuits are used to adjust the resolution of an integrator stage. These circuits are also used to convert the binary form into two’s complement representation. As discussed in Chapter 3, Sec. 3.3.1, since the integrator circuits have infinite gain at DC and at multiples of f_s, register overflow occurs at these frequencies. The data loss due to register overflow can be avoided by using the two’s complement method of coding as discussed in Chapter 3. The two coder circuits of Fig. 4.19 (a) have different architectures but their function is same i.e., to convert the binary data into two’s complement form and increase the resolution by 6 bits for K = 64 case and by 4 bits for K = 16 case. The input to the coder circuit-1 is the output of the first order modulator circuit. Since the modulator output is 1-bit, the input to the coder circuit-1 is either 1 or 0. For K = 64 case, the circuit should increase the resolution by 6-bits such that the output of the coder is a two’s complement 7-bit data. Similarly for k = 16 case the output is a two’s complement 5-bit data. The circuit to achieve this is shown in Fig. 4.20 (a). Figure 4.20 (b) shows the coder circuit-2 which is used for the second integrator stage. These two circuits shown use basic gates for achieving the required outputs. The output of the two circuits is given in tabular form and is shown in Table 4.2. For coder circuit–1, the input and output values are as defined by equation (3.11) in Sec. 3.3.3 of Chapter 3.
Figure 4.19 (a): Hardware implemental block diagram of the 2nd order integrator circuit.

Figure 4.19 (b): 1-bit integrator circuit used in Fig. 4.19 (a).
**Figure 4.20:** (a) Gate level schematic of coder circuit–1, (b) Gate level schematic of coder circuit–2.

**Table 4.2:** Tabular representation of input and output values of the two designed coder circuits.

<table>
<thead>
<tr>
<th></th>
<th>Coder Circuit -1</th>
<th>Coder Circuit - 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td><strong>Output</strong></td>
<td><strong>Input</strong></td>
</tr>
<tr>
<td><strong>For K = 64 Case</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0000001</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1111111</td>
<td>0</td>
</tr>
<tr>
<td><strong>For K = 16 Case</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>00001</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1111</td>
<td>0</td>
</tr>
</tbody>
</table>
For coder circuit–2 the 7-bit output of the first stage integrator is converted into 13- bit two’s complement form by complementing the MSB of the 7-bit output and extended the complemented value to form 13-bit. So the operation of coder circuit - 2 is just to complement its input hence an inverter is used.

4.6.2 Circuit for Programmability

The CIC filter has been designed to work for two oversampling ratios and this is made possible with the use of the circuit for programmability. This circuit works with the coder circuit -2 defined in the above section to give correct inputs to the second stage integrator for the two oversampling ratio cases. Referring to Fig. 4.19, for case K = 64, the MSB of the 7-bit output of the first stage integrator is complemented by the coder circuit -2 and extended to form a 13- bit data so that the second stage integrator works with 13-bits of data. But for K = 16 case, the second stage integrator should work with 9-bit data and only the first 5-bits of the first stage integrator output should be considered. For K = 16 case, the 5-bits from the first stage integrator are to be extended to 9-bits two’s complement data and to do this the 5th bit output of the first stage integrator has to be complemented and the complemented value should be substituted from 5th bit to the 9th bit. As an example for K = 64 case, a 7-bit digital output of the first integrator stage of (0)111000 is adjusted to two’s complement 13-bit data in the second integrator stage by complementing the MSB and substituting it at the MSB of the 7-bit so as to form 13-bit data which gives the output (1111111)111000. In the same example for K = 16 case, the output of the first integrator stage is 5-bits and read as (1)1000. This is adjusted to two’s compliment 9-bit data at the second integrator stage as (00000)1000. In both cases, four least significant bits (1000) are the same but bit 5 to bit 13 or most importantly bit 5 to bit 9 are not same. So in order to use the same CIC filter for both oversampling ratios, a circuit has to be designed which can
program bit 5 to bit 9. The circuit for programmability is designed to solve this problem. The circuit takes an enable signal as an input for choosing either of the two K values. When enable is HIGH, K =16 case is considered and when enable is LOW, K=64 case in considered. The circuit for programmability is shown in Fig. 4.21. The circuit has been divided into three blocks shown as a, b, and c in Fig. 4.21. It should be noted that the complement of bit 5 exists in all the three circuits. When enable is HIGH, K = 16 case is considered and the complement of bit 5 to 13 is applied to the next stage. Even though the circuit has 13-bit output, only the first 9 bits are considered for this case. When the enable signal is LOW, K = 64 is considered and the bits 5 and 6 are transferred from the output of the first stage integrator without any change but the complement of bit 7 is applied as the input to the bit 7 to bit 13 of the next stage. When the enable is LOW, bit 5 has no valid output so in Fig. 4.21 (c), bit 7 is transferred to the next stage.

The layout of the circuit for programmability is shown in Fig. 4.22. The layout shows the three circuits shown in Fig. 4.21 along with their inputs and outputs. The simulations results for the circuit for programmability are shown in Fig. 4.23. The simulations are done with all the three inputs i.e., bit 5, bit 6 and bit 7 in the logic HIGH state. The enable signal changes after 3 µs, but in actual the enable is fixed for a given particular case of oversampling ratio. When enable is HIGH, K = 16 case is selected, bit 5 to bit 13 will be the complement of the input bit 5. Since the input bit 5 is HIGH, the output is LOW as shown in results of Fig. 4.23 i.e., all the output bits 5 to 13 are LOW. When enable is LOW, K = 64 case is considered, hence the complement of input bit 7 is applied to output bits 7 to 13 which is the logic LOW state. The output bit 5 and bit 6 should be same as the input bits 5 and 6 and is evident from the simulation results. The enable is a control signal and decides the oversampling ratio for the ADC.
Figure 4.21: Circuits for programming the CIC filter to operate at two different oversampling ratios of 16 and 64. Note: Bit 5 has a valid value only if Enable = 1, if Enable = 0 it is at high impedance state.

Figure 4.22: Layout of the circuit for programmability used in the 2nd order integrator.
Figure 4.23: Simulation results showing the output and enable signals of the circuit for programmability. The simulations are done with a logic HIGH state for all the three inputs (bit 5 – bit 7).
For the K = 16 case, even though the output of the integrator block is 13-bits only, the least 9 bits are considered for the $2^{nd}$ order differentiator following the $2^{nd}$ order integrator.

The layout of the complete $2^{nd}$ order integrator circuit is shown in Fig. 4.24. The layout contains two integrator stages, two coder circuits, circuit for programmability and the level shifter circuit. Simulations have been performed on the integrator circuit and the experimental results of the complete CIC filter are discussed in Chapter 5.

4.7 Differentiator Block Design

A digital differentiator circuit is also called as a comb filter and acts as a low pass filter. The 13-bit output of the integrator is applied as the input to the differentiator. Unlike the integrator circuit which is clocked by the oversampling clock, the differentiator circuit is triggered by a clock whose frequency is $1/K$ times the oversampling clock frequency. The block diagram of the digital differentiator circuit is shown in Fig. 4.25 (a). The circuit shown is of $2^{nd}$ order and has two fixed 13-bit differentiator stages. A simple 1-bit differentiator which was shown in Chapter 3 is shown in Fig. 4.25 (b). The circuit is used to calculate the difference between the one input bit and the other input bit delayed by $KT_s$, where $T_s$ is the time period of the oversampling clock. In Boolean algebra, the difference operation of two inputs is nothing but the summation of the first input with the complement of the second input. To perform the difference operation, the second input is complemented and two’s complement method is used as the complementing scheme. To implement this in hardware, the second input which is delayed by a time $KT_s$ (sec) compared with the original input, is complemented using an inverter circuit. The carry input to the adder circuit is set at logic HIGH. By implementing these two conditions as illustrated in Fig. 4.25 (b), a two’s complement difference operation can be achieved. At the beginning of the differentiator circuit operation, there is no meaningful output until $2xKT_s$ (sec).
Figure 4.24: Complete layout of the 2nd order integrator circuit.
Figure 4.25 (a): Hardware implementation of a 2\textsuperscript{nd} order differentiator circuit.

Figure 4.25 (b): 1-Bit differentiator used in the Fig. 4.25 (a).
The reason for this is that the first differentiator stage has a valid output only after KT s seconds. Because the delay element delays the input by KT s, it has a valid output only after KT s seconds. Similarly the second stage differentiator also requires KT s to have a valid output. So, the output should be considered after this initial no-valid output time period has elapsed. The differentiator circuit operates with two’s complement 13-bit data that is supplied from the integrator stage. The output of the differentiator is also a two’s complement 13-bit data. This data has to be converted into binary form and also the least significant bits should be dropped in order to achieve the required resolution as was given in equation (3.4) in Chapter 3. The equation is again repeated here as equation (4.5).

\[
N_{\text{final}} = N_{\text{ip}} + N_{\text{inc}}
\]

\[
N_{\text{inc}} = \frac{30 \log K - 5.17}{6.02}
\]

From the equation (4.5) the final resolution depends on the input resolution of the decimator and also on the oversampling ratio K. For K = 64 case, the final resolution is 10 bits and this can be obtained from the 13-bit output of the differentiator circuit by dropping the lower 3 bits. Hence for K = 64 case, the upper 10 bits i.e., from bit 4 to bit 10 are considered. These bits are in two’s complement form and in order to convert them into binary the MSB bit, which in the present case is bit 13, is complemented. For K = 16 case, out of the 13-bits output only 9-bits are considered i.e., from bit 1 to bit 9 since for K = 16 case, the 2\textsuperscript{nd} order integrator boosts the resolution to 9 bits as discussed in the integrator block in Sec. 4.6. Even though the circuit has been designed to work with up to 13 bits, only 9 bits should are considered and the upper 4 MSB bits are ignored. Based on equation (4.5), the final resolution for K = 16 is 7 bits. These 7 bits are be obtained from the 9 bit output by dropping the lower two bits. Hence the final resolution for
K = 16 case is the bits starting from bit 3 to bit 9. The obtained 7-bit data is in two’s complement form and in order to convert into binary, the MSB bit i.e., bit 9 is complemented. The layout of the complete 2\textsuperscript{nd} order digital differentiator circuit is shown in Fig. 4.26. The layout has been done so as to optimize the area to achieve an area efficient design. For the MSB bits i.e., bit 13 for K=64 case which is to be complemented in order to covert the two’s complement scheme into binary form, an inverter circuit has been provided for that bit. For K=16 case no inverter has been provided because bit 9 is also an output bit for K=64 case. Providing an inverter for bit 9 will misinterpret the results when reading the output for K = 64 case. When the ADC is being operated with K=16, an external inverter can be placed at bit 9 in reading the 7 bit output.

4.8  CIC Filter Integration

A complete 2\textsuperscript{nd} order Cascaded Integrator Comb (CIC) filter can be obtained by integrating the 2\textsuperscript{nd} order digital integrator circuit with a 2\textsuperscript{nd} order differentiator circuit. A tabular representation of the type of circuits used and the number of transistors that have been designed is shown in Table 4.3. The table shows the total number of transistors that a CIC filter design contains. In Table 4.3, the circuit count implies the number of circuits that have been used in the design of the complete CIC filter. The number of full adder circuits and the number of delay elements required are very high and hence, the design has been done to minimize the area and to decrease the delay. The complete layout of the CIC filter has been designed and the layout of the design which has been done in 1.5 μm n-well CMOS process is shown in Fig. 4.27. The design is placed inside a 40 pin padframe. As can be seen from the layout in Fig. 4.27 that the CIC filter consumes huge area on silicon chip which is the main reason why these filters are complex to build in hardware. The experimental results of the CIC filter are presented in Chapter 5.
Figure 4.26: Layout of the 2nd order digital differentiator circuit.

Table 4.3: Tabular representation of the different circuits used and the number of transistors designed for a 2nd order CIC filter.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Circuit count (M)</th>
<th>No. of transistors (N)</th>
<th>Total No. of transistors/Circuit (M*N)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Adder</td>
<td>46</td>
<td>18</td>
<td>828</td>
</tr>
<tr>
<td>Shift Register</td>
<td>46</td>
<td>12</td>
<td>552</td>
</tr>
<tr>
<td>D-flip flops</td>
<td>6</td>
<td>34</td>
<td>204</td>
</tr>
<tr>
<td>AND gates</td>
<td>10</td>
<td>6</td>
<td>60</td>
</tr>
<tr>
<td>MUX and buffers</td>
<td></td>
<td></td>
<td>76</td>
</tr>
<tr>
<td><strong>Total Transistors</strong></td>
<td></td>
<td></td>
<td><strong>1720</strong></td>
</tr>
</tbody>
</table>
Figure 4.27: Complete layout of the Cascaded Integrator Comb (CIC) filter in a 40 pin padframe (2.25 X 2.25 mm$^2$).
Chapter 5
Experimental Results and Discussion

A 2\textsuperscript{nd} order CIC filter has been designed to work as a decimator for the sigma-delta analog-to-digital converter in 1.5 \textmu m n-well CMOS process. The complete sigma-delta ADC system has been tested for proper working by integrating the decimator with the modulator. In this chapter, the experimental results of the ADC are presented and will be discussed.

5.1 Experimental Setup

The experimental setup of the complete ADC system is shown in Fig. 5.1. Figure 5.2 shows the microphotograph of the decimator integrated circuit. The modulator and decimator are two different integrated circuits designed in 1.5 \textmu m n-well CMOS process and the output of the modulator is fed as the input to the decimator. The input to the modulator is an analog signal is fed from a function generator. The decimator can deliver a 10-bit and 7-bit output which is observed through a logic analyzer. Both the modulator and the decimator require an oversampling clock, and is supplied externally using a clock generator. The ADC system can work up to an oversampling clock frequency of 8 MHz.

The input specifications that are applied to the ADC are shown below:

Modulator Specifications:

- Analog input signal amplitude of 4 V peak - peak at a frequency of 1 kHz is given from a function generator.
- DC power supplies of +2.5 V and -2.5 V are given from a power supply.
- The oversampling clock signal is given from a pulse generator.
- The output is analyzed through an oscilloscope.

Decimator Specifications:

- The input digital data to the decimator is given from the output pin of the modulator.
- The same oversampling clock as that of the modulator is applied.
- The digital output data and the clock divider output are analyzed using a logic analyzer.
Figure 5.1: Experimental setup showing the modulator and decimator integrated circuits.

Figure 5.2: Microphotograph of the fabricated decimation filter.
The input sine wave frequency is set at 1 KHz frequency with a band width of 2 KHz. The oversampling clock frequency is given by the product of the oversampling ratio (K) with twice the input signal band width (Nyquist rate). Hence for K = 64 case, the oversampling clock frequency is 256 KHz (64 X 4 KHz). For K = 16 case, the oversampling clock frequency is 64 KHz (16 X 4 KHz). In both the cases, the input to the ADC is set at the same band width of 2 KHz.

The output of the modulator is a 1-bit pulse density modulated signal occurring at the oversampling clock rate. Since K = 64 the input sine wave is sampled with an oversampling clock of frequency 256 KHz. The output of the first order modulator circuit for K= 64 case is shown in Fig. 5.3. The output is 1-bit digital data and the average of the modulator output follows the actual input sine wave signal shown in Fig. 5.3. Since the modulator is operated in the voltage range – 2.5 V to + 2.5 V the 1-bit output is also in that range. This 1-bit modulator output is applied as the input to the decimator circuit and the voltage range is shifted to 0 to 5 V.

5.2 Clock Divider Circuit Output

The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.
Figure 5.3: Experimental results showing the 1-bit pulse density modulated output and inputs sine wave of an already designed sigma-delta modulator.
The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KT_s, where T_s is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KT_s and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KT_s remains constant for both the cases.

The clock divider circuit plays a crucial role in generating the high resolution digital output at twice the input signal band width or at the nyquist frequency for further processing. Since the clock divider circuit has an output at the nyquist rate. The output of the decimator appears at the same time instants as that of the output pulses of the clock divider circuit.
Figure 5.4: Experimental results showing the output of the clock frequency divider circuit for frequency division by the ratio 64.

Figure 5.5: Experimental results showing the output of the clock frequency divider circuit for frequency division by the ratio 16.
5.3 CIC Filter Output

The modulator output is applied to the integrator stage which boost the resolution from 1-bit to higher resolutions of 13-bit and 9-bit for $K = 64$ and $K = 16$, respectively. The output of the integrator is applied as the input to the differentiator circuit working at the same resolution as that of the second integrator stage. The output of the differentiator which is also the output of the decimator is the final output of the sigma-delta analog-to-digital converter.

The output of the decimator is an $N$-bit binary data occurring at twice the input signal bandwidth. Since the input signal frequency at which the ADC is operated is at 1 KHz and of bandwidth 2 KHz, the output occurs at 4 KHz. The input signal has a time period of 1 ms, this is the time a sine wave takes to complete one cycle. Since the output data frequency is 4 KHz the output takes 0.25 ms to complete one cycle. So in each cycle of the input signal there exists four output signals i.e., at every time instant of 0.25 ms there is an $N$-bit digital output representing the analog signal value at that time instant. As the decimator can be programmed to work for two different oversampling ratios, the results of the decimator are also analyzed separately for the two different cases i.e., for two different oversampling ratios of 64 and 16.

For an ADC 1 LSB is defined as [28]

\[ 1\text{LSB} = \frac{V_{\text{FSR}}}{2^N} \] (5.1)

Where $V_{\text{FSR}}$ is the full scale voltage range of the input signal and $N$ is the number of output bits. In the present application a $V_{\text{FSR}}$ is 4 V.

5.3.1 $K = 64$ Case

Both the modulator and the decimator are operated with the same oversampling clock of frequency 256 KHz. As discussed in Chapters 3 and 4, the output resolution of the ADC for $K =$
64 case is 10-bits and the experimental results are illustrated in Table 5.1 which shows the 10-bit binary output, its decimal equivalent, analog equivalent and the actual analog voltage. In Table 5.1 a set of two data samples is shown together. Based on the equation (5.1), for the case of K = 64, the value of 1 LSB for a 10-bit digital output is \(4/2^{10} = 3.9 \text{ mV}\). The LSB value is used in finding the analog equivalent of the digital output. From the Table 5.1, the first two output samples are 1011000001 and 0011000010. These are read in the order they are written i.e., the left most bit is the Most Significant Bit (MSB) and the right most bit is the Least Significant Bit (LSB). The decimal equivalent of the above two 10-bit data are given by the values 705 and 194, respectively. These values are obtained by multiply the bit coefficient with the respective powers of 2. For example the decimal equivalent value for the first data stream is obtained as shown below:

\[1 \times 2^9 + 0 \times 2^8 + 1 \times 2^7 + 1 \times 2^6 + 0 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 705.\]

Using the similar approach the decimal equivalent for other outputs can be found.

The analog equivalent can be calculated from the decimal equivalent by multiplying the decimal equivalent value with the value for 1 LSB. For the decimal value of 705, its analog equivalent is given by 705 \(\times 3.9 \text{ mV} = 2.749\). The analog equivalent values for the two data outputs taken into consideration are given as 2.749 and 0.756, respectively. As already mentioned the ADC is operated with a peak-to-peak voltage of 4 V but in the voltage range –2 V to +2 V. The calculated value of LSB and the analog equivalent values are both positive. The analog equivalent that is represented in Table 5.1 represents the voltage range from 0 to 4 V but to represent the actual input voltage which ranges from -2 V to +2 V, a drop of 2 V in the value of analog equivalent is required as shown in the last column of the Table 5.1. The experimental output results for the two considered decimal values are shown in Fig. 5.6.
Table 5.1: Tabular data representation of the 10-bit decimator output for K = 64 case

<table>
<thead>
<tr>
<th>Digital Code</th>
<th>Decimal Equivalent</th>
<th>Analog Equivalent (A)</th>
<th>Actual Analog voltage (A – 2 V) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1011000001</td>
<td>705</td>
<td>2.749</td>
<td>0.749</td>
</tr>
<tr>
<td>0011000010</td>
<td>194</td>
<td>0.756</td>
<td>-1.244</td>
</tr>
<tr>
<td>0101101111</td>
<td>367</td>
<td>1.431</td>
<td>-0.569</td>
</tr>
<tr>
<td>1101011001</td>
<td>857</td>
<td>3.428</td>
<td>1.428</td>
</tr>
<tr>
<td>1010001001</td>
<td>658</td>
<td>2.632</td>
<td>0.632</td>
</tr>
<tr>
<td>1101001010</td>
<td>842</td>
<td>3.368</td>
<td>1.368</td>
</tr>
<tr>
<td>1100111111</td>
<td>831</td>
<td>3.324</td>
<td>1.324</td>
</tr>
<tr>
<td>1010011110</td>
<td>670</td>
<td>2.68</td>
<td>0.68</td>
</tr>
<tr>
<td>1001111010</td>
<td>634</td>
<td>2.472</td>
<td>0.472</td>
</tr>
<tr>
<td>0010001001</td>
<td>137</td>
<td>0.534</td>
<td>-1.466</td>
</tr>
<tr>
<td>1011111001</td>
<td>761</td>
<td>2.967</td>
<td>0.967</td>
</tr>
<tr>
<td>0011110111</td>
<td>247</td>
<td>0.963</td>
<td>-1.037</td>
</tr>
<tr>
<td>1011111000</td>
<td>760</td>
<td>2.964</td>
<td>0.964</td>
</tr>
<tr>
<td>1011110100</td>
<td>756</td>
<td>2.948</td>
<td>0.948</td>
</tr>
<tr>
<td>1010100110</td>
<td>685</td>
<td>2.671</td>
<td>0.671</td>
</tr>
<tr>
<td>0011000101</td>
<td>197</td>
<td>0.768</td>
<td>-1.232</td>
</tr>
<tr>
<td>1101011101</td>
<td>861</td>
<td>3.357</td>
<td>1.357</td>
</tr>
<tr>
<td>0100110011</td>
<td>307</td>
<td>1.197</td>
<td>-0.803</td>
</tr>
<tr>
<td>1100001101</td>
<td>781</td>
<td>3.045</td>
<td>1.045</td>
</tr>
<tr>
<td>1011100101</td>
<td>741</td>
<td>2.889</td>
<td>0.889</td>
</tr>
</tbody>
</table>
Figure 5.6: Experimental results showing the waveforms for two digital output codes 1011000001 and 0011000010. The waveforms for the oversampling clock(lab1-11) of frequency 256 KHz and the output of the clock divider circuit(lab1-10) is also shown.

10-bit digital output where Lab1-9 is the MSB and Lab1-0 is the LSB.

output of the clock divider circuit.

oversampling clock.
The waveforms for the 10-bit digital output data shown in Fig. 5.6 using the labels Lab1 0 through Lab1 9 where Lab1 9 represents the MSB value and Lab1 0 represents the LSB value. The waveforms for the oversampling clock and the output of the clock divider circuit by a ratio of 64 are also shown using the labels Lab1 10 and Lab1 11, respectively. The output of the decimator exists only at the output of the clock divider circuit and since the clock divider circuit has an output at the nyquist frequency, the decimator output is also at the nyquist rate.

In this way the decimal, analog and actual analog voltage for the other digital outputs can be calculated for other analog samples as shown in Table 5.1. The voltage difference between every two set of data samples is 2 V. Since the output frequency is at 4 KHz and the input signal is at 1 KHz, there exist four output data words in one clock cycle of the input signal as discussed above in Sec. 5.3. This implies that the actual analog output values should differ by 2 V i.e., the voltage difference between two output data words is 2 V. In Table 5.1 more than four data samples are shown which were observed at different time instants and also at different experimental runs. The data samples are identical and illustrate the periodic nature.

5.3.2 $K = 16$ Case

The output of the decimator for $K=16$ case has an output resolution of 7-bits as discussed in Chapters 3 and 4. The experimental results for the decimator output for $K = 16$ case are presented in Table 5.2. The table has been divided into four columns for representing the output binary code, its decimal and analog equivalent and also the actual analog input voltage. The value for 1 LSB based on equation (5.1) which has an output resolution of 7-bits is $4/2^7 = 0.031$ V. In similar lines as explained with $K=64$ case, the analog equivalent of the decimal code can
be calculated by multiplying the LSB value with that of the decimal equivalent. The actual analog input voltage can be obtained by dropping 2 V from the analog equivalent value.

The experimental waveforms for the decimator output for the first two digital codes shown in Table 5.2 are shown in Fig. 5.7. In the Fig. 5.7, the 7-bit output is represented using labels Lab1 0 through Lab1 6, where Lab1 0 is the LSB and Lab1 6 is the MSB. The MSB is represented using label Lab1 6 is not complemented. However, the MSB value should be complemented in order to convert the two’s complement output into binary form. For this reason when reading the output from the logic analyzer the complement of the MSB value is read. The correct value of the MSB for the 7-bit code is shown in Table 5.2. The voltage difference between two set of output data words is 2 V.
Table 5.2: Tabular data representation of the 7-bit decimator output for K = 16 case

<table>
<thead>
<tr>
<th>Digital Code</th>
<th>Decimal Equivalent</th>
<th>Analog Equivalent (A)</th>
<th>Actual Analog Voltage (A – 2 V) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1101000</td>
<td>104</td>
<td>3.224</td>
<td>1.224</td>
</tr>
<tr>
<td>0100110</td>
<td>38</td>
<td>1.178</td>
<td>-0.822</td>
</tr>
<tr>
<td>1101110</td>
<td>118</td>
<td>3.658</td>
<td>1.658</td>
</tr>
<tr>
<td>1001100</td>
<td>76</td>
<td>2.358</td>
<td>0.358</td>
</tr>
<tr>
<td>0101000</td>
<td>40</td>
<td>1.24</td>
<td>-0.76</td>
</tr>
<tr>
<td>0100000</td>
<td>32</td>
<td>0.992</td>
<td>-1.008</td>
</tr>
<tr>
<td>1110010</td>
<td>114</td>
<td>3.534</td>
<td>1.534</td>
</tr>
<tr>
<td>1010010</td>
<td>82</td>
<td>2.542</td>
<td>0.542</td>
</tr>
<tr>
<td>1011100</td>
<td>92</td>
<td>2.852</td>
<td>0.852</td>
</tr>
<tr>
<td>0011110</td>
<td>30</td>
<td>0.93</td>
<td>-1.07</td>
</tr>
<tr>
<td>1011000</td>
<td>88</td>
<td>2.728</td>
<td>0.728</td>
</tr>
<tr>
<td>1110010</td>
<td>114</td>
<td>3.534</td>
<td>1.534</td>
</tr>
</tbody>
</table>

7-bit digital output where Lab1-6 is the MSB and Lab1-0 is the LSB.

Output of the clock divider circuit.

Oversampling clock.
Figure 5.7: Experimental results showing the waveforms for two digital output codes 0101000 and 1100110. The output codes are read after complementing the MSB as 1101000 and 0100110. The waveforms for the oversampling clock (Lab 1-11) of frequency 64 KHz and the output of the clock divider circuit (Lab 1-10) are also shown.

Chapter 6

Conclusion

A 2nd order programmable CMOS decimation filter has been successfully designed and fabricated which can be used to integrate with a first order modulator in forming a complete sigma-delta analog-to-digital converter. The fabricated decimator has been implemented using a 2nd order Cascaded Integrator Comb (CIC) filter which has a 2nd order digital integrator and a 2nd order digital differentiator circuits. The decimator designed is programmable to work with two oversampling ratios of 64 and 16 in generating the output resolution of 10-bit and 7-bit, respectively. Programmability into the design has been made possible with the design of a circuitry which works using an enable signal to select either one of the oversampling ratios for which the decimator has to be operated. Clock frequency divider circuit has been designed to generate two clock signals whose frequencies are divided by 64 and 16 with respect to the input clock frequency for operating the decimator at the two oversampling ratios. The experimental results of the fabricated sigma-delta ADC have been carried out with a clock oversampling frequency of 256 KHz and with an input signal bandwidth of 2 KHz. The output of the decimator occurs at twice input signal bandwidth of 4 KHz and the obtained experimental results are in close agreement with the designed specifications. The oversampling clock frequency can be set based upon the input signal frequency and the integrated ADC can be operated with oversampling clock frequency of up to 8 MHz. Since the decimator can be programmed and also the input signal frequency can be set by the user, the complete ADC can be programmed to work for two different oversampling ratios and also for different input signal bandwidths.
Part II: Charge Pump Circuits
Chapter 7

Charge Pump Circuits

The method of generating voltages greater than the supply voltage is not new. Crockcroft and Walton [33] proposed a design to achieve higher voltages using multiple capacitances. However it does not allow for a monolithic integration due to large capacitances. This problem is solved to a larger extent by the Dickson charge pump design which can be integrated and can generate higher output voltages using on-chip capacitors [16].

7.1 Dickson Charge Pump Design

Figure 7.1 shows an N-stage Dickson charge pump circuit. Each stage in the design is referred to as a pumping stage and comprises of an NMOS transistor followed by a coupling capacitor. NMOS transistors in diode connected configuration act as one directional switches transferring charge from the drain terminal to the source terminal. The coupling capacitors are used to store and pump the charge forward in alternate clock cycles. The charge is transferred and stored in the load capacitor. Complementary clock scheme is used to transfer the charge alternatively from the coupling capacitors to the load capacitor. The coupling capacitors of a particular stage gets charged to the voltage available at the drain terminal less the threshold voltage drop of the NMOS transistor of that particular stage, whenever the clock voltage on its lower plate is at ground potential. When a transition from $0 \text{ V}$ to $V_{\text{DD}}$ occurs on the lower plate of the capacitor, the voltage on the top plate gets boosted to the sum of its previously stored voltage on the capacitor plus the clock voltage $V_{\text{DD}}$. This way the coupling capacitors gets charged and boosted in alternate clock cycles and transfer the charge in forward direction. The final boosted charge is accumulated on the load capacitor achieving higher output voltages. The final voltage stored on the load capacitor can be given by equation (7.1) [16].
Figure 7.1: An N-stage Dickson charge pump circuit.
\[ V_{\text{out}} = V_{DD} + N \left[ \left( \frac{C}{C + C_p} \right) \times V_{DD} - V_T \right] - V_T \]  

(7.1)

where \( V_{DD} \) is the supply voltage and also the magnitude of the complementary clock signals. Usually in most applications involving charge pump circuits both the supply voltage and the clock voltage are considered equal and taken as \( V_{DD} \). \( N \) is the number of pumping stages and \( V_T \) is the threshold voltage of the NMOS transistor switch. The threshold voltage is assumed to be same for all the switches. The equation takes into account the parasitic capacitances, \( C_p \) associated with the coupling capacitor in the design. The equation can be written after neglecting the parasitic capacitances as

\[ V_{\text{out}} = V_{DD} + N\left[V_{DD} - V_T\right] - V_T \]  

(7.2)

From the equation (7.2) the gain of each stage of a charge pump can be given by \( V_{DD} - V_T \) and the complete gain of the charge pump is given by \( N(V_{DD} - V_T) \). It is observed that the output voltage and the gain of the Dickson charge pump circuit directly depend on the clock voltage \( V_{DD} \) and on the threshold voltage \( V_T \). In actual the threshold voltage of all the NMOS transistors used in the design is not constant due to the body effect. Since the source and the body terminal of NMOS transistor are at different potential based on the following equation (7.3) the \( V_T \) of the transistor varies.

\[ V_T = V_{TO} + \gamma \left( \sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right) \]  

(7.3)

where \( V_{TO} \) is the zero body bias threshold voltage, \( \gamma \) is the body effect coefficient, \( \phi_f \) is the bulk potential and \( V_{SB} \) is the source to body voltage. Since each transistor has its source at different potential compared to the body which is at ground potential, each transistor will have different threshold voltage. Since the threshold voltage increases with body effect the gain of the
transistor decreases. Many different charge pump circuits have been designed to overcome this problem with the threshold voltage [12, 17, 18, 19].

The problem with the threshold voltage is overcome using a charge pump design based on PMOS transistor switches [19]. The body of the MOSFET is used as an active terminal to avoid the problem associated with the threshold voltage. The body of the PMOS transistor switches is controlled using two auxiliary PMOS transistors such that the source to body diode of these PMOS transistor switch is always reverse biased eliminating the body effect. The output voltage obtained from this design is higher compared to the Dickson charge pump when the number of pumping stages is higher. This design addresses the threshold voltage problem well but uses PMOS transistors instead of the NMOS transistors as the switches. Since the mobility of holes in a PMOS transistor is less than the mobility of electrons of an NMOS transistor, the rise time for the output voltage of the charge pump to reach 90% of its steady state value is increased. Also, the design uses two additional auxiliary PMOS transistors for each stage. Hence the transistor count for a single charge pumping stage is three while the transistor count for a Dickson charge pump design is one.

A different charge pump design has been presented using NMOS transistor switches similar to the Dickson charge pump. The gate of the one directional charge transfer switches is controlled using the concept of back control [34]. The gate is at a higher potential such that the switch is closed and there is no voltage drop between the source and the drain terminals unlike in a Dickson charge pump. The design overcomes the problem associated with the threshold voltage by operating the gate at higher voltages. This design achieves high output voltages from a low supply voltage. But the design requires large number of transistors to establish the higher gate voltages for the charge transfer switches. The design also requires precise control of the
complementary clock signals required for the charge pump. The complementary clock signals are used to turn on and turn off the charge transfer switches.

An area efficient charge pump structure is designed using cross-coupled charge pump architecture [12]. The charge pump uses $V_{DD}$ to $2V_{DD}$ clock voltages to reduce the number of capacitors and the transistors required. The design uses minimum number of transistors and capacitors in achieving an output voltage of four times and six times the input supply voltage. In the reported design [12] only four-stage and six-stage design have been presented. The concept of cross-coupled structure becomes quiet complex in the design of higher order charge pump circuits.

Several charge pump designs are reported [17, 19] and concentrates on the existing threshold voltage problem in Dickson charge pump circuit. Power efficient and area efficient design have been reported [12, 18]. But in this work a modified Dickson charge pump is presented which targets the clock voltage. In the present work, a new technique has been developed to boost the clock internally to achieve higher output voltages. The main focus of the design is to keep the simplicity of the Dickson charge pump and to use minimal number of transistors and capacitors. Using the developed technique, a four-stage and a six-stage charge pump circuits have been designed and implemented in 1.5 µm n-well CMOS process.

### 7.2 Charge Pump Circuits Based on Internal Clock Voltage Boosting Technique

#### 7.2.1 Four-Stage Charge Pump Design

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, $C_1$, $C_2$, $C_3$ and $C_4$ are used as coupling capacitors and the pumped charge is
transferred to the load capacitor, $C_L$ using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors $M_1$ to $M_3$, $M_6$ and $M_7$ are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, $M_5$ and the NMOS transistor, $M_4$ form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor $C_1$ is $V_{DD} - V_{TN}$, the voltage on capacitor $C_2$ is $2V_{DD} - 2V_{TN}$ and voltage on capacitor $C_3$ is $3V_{DD} - 3V_{TN}$. With this initial condition, voltages on the capacitor $C_4$ and the load capacitor, $C_L$ can be obtained as follows under clocking conditions.

When $CLK$ is high, $CLK_{INV}$ is low, the voltage at node A is $V_{AH} = 2V_{DD} - V_{TN}$, voltage at node B is $V_{BH} = 2V_{DD} - 2V_{TN}$. The voltage at node C is $V_{CH} = 3V_{DD} - 3V_{TN} + V_{DD}$. The PMOS transistor $M_5$ will turn off since its $V_{GS} = V_{AH} - V_{BH} = + V_{TN}$ which is greater than its threshold voltage $-V_{TP}$ and NMOS transistor $M_4$ turns on which pulls down the voltage at node D to 0 V. The capacitor $C_4$ now gets charged to the voltage equal to $V_{CH} - V_{TN}$. In the next clock cycle when $CLK$ is low, $CLK_{INV}$ is high, the voltage at node A is $V_{AL} = V_{DD} - V_{TN}$ and voltage at node B is $V_{BL} = V_{BH} + V_{DD}$ assuming $C_2$ remains charged to $V_{BH}$ when clock goes low. The voltage at node C is $V_{CL} = V_{BL} - V_{TN} = 3V_{DD} - 3V_{TN}$. The transistor $M_5$ turns on since its $V_{GS} = V_{AL} - V_{BL} = -2V_{DD} + V_{TN}$ and transistor $M_4$ turns off.
Figure 7.2: Four-stage charge pump circuit based on internal clock voltage boosting.
The node D is pulled up to the voltage at node B by $V_{BL}$, which is equal to $3V_{DD} - 2V_{TN}$. This voltage pumps-up the capacitor $C_4$ which already has a voltage of $V_{CH} - V_{TN} = 4V_{DD} - 4V_{TN}$ when CLK was high. Now the total voltage at node E, is $V_{CH} - V_{TN} + V_{BL} = 7V_{DD} - 6V_{TN}$. The pumped voltage is transferred to the load capacitor, $C_L$ with a voltage drop equal to the threshold voltage, $V_{TN}$ of the transistor $M_7$. The voltage, $V_{out}$ on the load capacitor, $C_L$ is now given by $7V_{DD} - 7V_{TN}$.

The four-stage charge pump has been designed to work with both on-chip and off-chip capacitors. The layout shown in Fig. 7.3 is for a four-stage charge pump with on-chip capacitors. The W/L ratios of the transistors $M_1$ to $M_7$ (except $M_4$) of Fig. 7.2 corresponding to the on-chip design are 160/1.6 and the W/L ratio of transistor $M_4$ is 80/1.6. The values for the coupling capacitors $C_1$ to $C_4$ of Fig. 7.2 corresponding to the on-chip design are 5 pF and the on-chip load capacitors value is 10 pF. Figure 7.4 shows the layout of the four-stage charge pump which incorporates off-chip capacitors. The W/L ratios of transistors $M_1$ to $M_7$ (except $M_4$) for the off-chip case are 221.6/1.6 and for transistor $M_4$ is 1110.4/1.6.

The simulation of the four-stage charge pump with on-chip and off-chip capacitors has been performed using SPICE. Figure 7.5 (a) show the comparison curves for the four-stage charge pump and a four-stage Dickson charge pump using on-chip capacitors. The capacitors for both the designs are chosen to be 5 pF for the coupling capacitors and 10 pF for the load capacitor. The designs are simulated with in the input voltage range of 1.2 V to 3 V. The complementary clocks required for the charge pump circuits is set at 1 MHz. The plots in Fig. 7.5 (a) show the variation of output voltage with respect to the input voltage of both the designs.
Figure 7.3: Layout of the four-stage charge pump with on-chip capacitors.

Figure 7.4: Layout of the six-stage charge pump with off-chip capacitors.
It can be observed that the modified four-stage charge pump offers higher output voltages compared to the Dickson charge pump. The output voltage of the modified charge pump is more than the output voltage of the Dickson charge pump by 0.8 V in the 1.2 to 2 V input voltage range and by 2 V in 2 to 3 V of the input voltage range. Figure 7.5 (b) shows the comparison for the four-stage charge pump and a four-stage Dickson charge pump using off-chip capacitors. For simulation the off-chip capacitors values are chosen to be 100 nF and a load capacitor value is set at 1 µF. The clock frequency is chosen to be 100 KHz. The output voltage of the modified charge pump is higher than the Dickson charge pump output voltage by 1 V in the 1.2 to 2 V input voltage range and by 3 V in 2 to 3 V of the input voltage range.

Figure 7.6 shows the input and output voltage of the four-stage charge pump using off-chip capacitors. An output voltage of 14.5 V is achieved with an input supply voltage of 3 V. The output voltage is more than four times the input voltage. The time for the output to reach from 10 % to 90 % of the steady state value is defined as the rise time. From the Fig. 7.6 the rise time of the four-stage charge pump is observed to be 2 ms. The same charge pump circuit can also be used to generate higher amplitude clock signals. Figure 7.7 shows the clock output taken from node D in Fig. 7.2. The clock output is an inverted version of the input clock signal but the amplitude of which is higher than the input clock by a factor of 2.5. The obtained higher amplitude clock and its complement can be used as a clock for other charge pump stages for achieving much higher voltages. The limitation for such application is the magnitude of the voltages the charge pump can operate with. Gate oxide breakdown voltage and the diode breakdown voltage due to the diode that exists between the source/drain to the substrate of the MOSFET limit the voltages.
Figure 7.5 (a): The simulated performance of the modified four-stage charge pump design and comparison with the four-stage Dickson charge pump using on chip capacitors.

\[ \Delta V_{out} = 0.8 \text{ V in } 1.2 \text{ V} - 2 \text{ V} \]
\[ = 2 \text{ V in } 2 \text{ V} - 3 \text{ V}. \]

Figure 7.5 (b): The simulated performance of the proposed four-stage charge pump design and comparison with the four-stage Dickson charge pump using off chip capacitors.

\[ \Delta V_{out} = 1 \text{ V in } 1.2 \text{ V} - 2 \text{ V} \]
\[ = 3 \text{ V in } 2 \text{ V} - 3 \text{ V}. \]
Figure 7.6: Simulation results showing the input and output voltage of the four-stage charge pump using off-chip capacitors.

Figure 7.7: Simulation results showing the clock input and amplified clock output taken from the intermediate node of the four-stage charge pump using off-chip capacitors.
7.2.2 Six-Stage Charge Pump Design

Figure 7.8 shows the design of a six-stage charge pump CMOS circuit designed similar to the design presented in Fig. 7.2 for the four-stage charge pump circuit. The circuit uses six coupling capacitors and a load capacitor. In Fig. 7.8, the inverter formed by the PMOS transistor M₆ and NMOS transistor M₇ does the operation of boosting the clock voltage internally and the output of the inverter generates a higher clock voltage. Similar to the analysis described in Sec. 7.2.1, the output voltage, $V_{out}$ for the six-stage charge pump design is given by $11V_{DD} - 11V_{TN}$.

The layout of the six-stage charge pump using on-chip and off-chip capacitors is shown in Fig. 7.9. For the six-stage charge pump with off-chip capacitors, the W/L ratios of the transistors M₁ to M₉ (except M₇) are 2217.6/1.6 and for transistor M₇ is 1110.4/1.6.

Post-layout SPICE simulation is performed on the six-stage charge pump using on-chip capacitors of Fig. 7.9 (a). The values for the coupling capacitors have chosen to be 5 pF and a load capacitor value of 10 pF. Figure 7.10 (a) shows the comparison curves of the six-stage charge pump and a six-stage Dickson charge pump using on-chip capacitors. The simulations have been performed in the voltage range of 1.2 to 3 V and the clock frequency is chosen to be 1 MHz. The output of the modified charge pump is higher than the Dickson charge pump by 0.8 V in the 1.2 to 2 V input voltage range and by 3 V in 2 to 3 V of the input voltage range. Figure 7.10 (b) shows the comparison curves for the six-stage charge pump of Fig. 7.9 (b) and a Dickson charge pump using off-chip capacitors. The simulations have been done with coupling capacitors of value 100 nF and a load capacitor value is set at 1 µF. The clock frequency is chosen to be 100 KHz. The output voltage of the modified charge pump is higher than the Dickson charge pump output voltage by 1 V in the 1.2 to 2 V input voltage range and by 4 V in 2 to 3 V of the input voltage range.
Figure 7.8: Six-stage charge pump circuit based on internal clock voltage boosting.

Figure 7.9: (a) Layout of the six-stage charge pump using on-chip capacitors and (b) layout of the six-stage charge pump using off-chip capacitors.
Figure 7.10 (a): The simulated performance of the modified six-stage charge pump design and comparison with the six-stage Dickson charge pump using on chip capacitors.

Figure 7.10 (b): The simulated performance of the proposed six-stage charge pump design and comparison with the six-stage Dickson charge pump using off chip capacitors.
Figure 7.11 shows the input and output voltage of the six-stage charge pump using off-chip capacitors. An output voltage of 22 V is achieved with an input supply voltage of 3 V. The output voltage is more than six times the input voltage. The same charge pump circuit can be used to generate higher amplitude clock signals. Figure 7.12 shows the clock output taken from lower plate of capacitor $C_6$ in Fig. 7.8. The clock output is an inverted version of the input clock signal but the amplitude of which is higher than the input clock by a factor of 4.

One clock voltage booster stage is used in both the four-stage and six-stage charge pump circuits. But higher output DC voltages can be achieved by using more than one clock voltage boosting stage and also by cascading more number of pumping stages. The limitation for achieving very high output voltages is that the transistors that are being used as switches should be able to withstand such high voltages. High voltages can cause oxide breakdown. The threshold voltage of the switches can also limit the possibility of achieving large output voltages.

**7.2.3 High Voltage Clock Generator Circuit**

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors $M_4$ to $M_7$ and the pumping stage containing capacitor $C_3$ forms the clock voltage boosting stage. By using the coupling capacitor $C_3$, the voltage power supply to the inverter formed by the transistors $M_6$ and $M_7$ is boosted to the voltage stored on capacitor, $C_3$ plus the clock amplitude $V_{DD}$. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the four-stage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.
Figure 7.11: Simulation results showing the input and output voltage of the six-stage charge pump using off-chip capacitors.

Figure 7.12: Simulation results showing the clock input and amplified clock output taken from the intermediate node of the six-stage charge pump using off-chip capacitors.
Figure 7.13: Circuit for generating higher clock voltages.

Figure 7.14: Simulated input and output of the circuit for generating higher amplitude clocks.
When CLK is high, CLK_INV is high and the output of the inverter formed by the transistors M4 and M5 is pulled low. The output of the circuit is pulled high to a voltage at node C which is \( 4V_{DD} - 3V_{TH} \). It can be observed that this amplitude of the output clock voltage is much higher than the input clock voltage of \( V_{DD} \). When CLK is low, CLK_INV is high and the output of the inverter formed by transistors, M4 and M5 is pulled high to voltage at node B, \( 3V_{DD} - 2V_{TH} \). This pulls the output of the circuit to 0 V. The circuit generates clock of higher amplitudes and also retains the frequency, phase and duty cycle of the input clock. The values of the coupling capacitors are chosen to be 0.1 \( \mu F \) and the charge pump is operated at a clock frequency of 100 KHz. The output clock amplitude achieved with an input clock of amplitude 3 V is 9.5 V with a current drive of 500 \( \mu A \).

### 7.3 Experimental Results and Discussion

The four-stage and six-stage charge pump circuits have been designed and fabricated in 1.5 \( \mu m \) n-well CMOS process. The layout and the microphotograph of the IC chip containing the Dickson and proposed charge pump circuits is shown in Fig. 7.15 (a) and 7.15 (b), respectively. In the Fig. 7.15, block A represents the four-stage Dickson charge pump circuit using on-chip capacitor. Block B shows the proposed four-stage charge pump circuit using on-chip capacitors. Both the designs use on-chip capacitors of value 5 pF. Block C and Block D represent the proposed four-stage and six-stage charge pump circuits using off-chip capacitors. The Block-C for the four-stage charge pump is designed with very large size transistors. The transistors, M1 to M7 (except M4) are designed with W/L ratio of 2217.6/1.6. The transistor, M4 is designed with W/L ratio of 1110.4/1.6. The Block-D for the six-stage charge pump also uses very large size transistors. The transistors, M1 to M9 (except M7) are designed with W/L ratio of 2217.6/1.6. The transistor, M7 is designed with W/L ratio of 1110.4/1.6.
Figure 7.15 (a): IC layout showing the charge pump circuits.

Figure 7.15 (b): Microphotograph showing the charge pump circuits.

Block-A represents a four-stage Dickson charge pump with on chip capacitors.

Block-B represents the proposed four-stage charge pump with on chip capacitors.

Block-C and Block-D represent the proposed four-stage and six-stage charge pumps with external capacitors.
The W/L ratios of the four-stage Dickson charge pump circuits shown in block A is 160/1.6. The W/L ratios of the proposed four-stage charge pump shown in block B is 160/1.6 for transistors M1 to M7 except M4 of Fig. 7.2. The W/L ratio of transistor M4 is 80/1.6.

The measured results of the four-stage Dickson and the proposed four-stage charge pump using on-chip capacitors are shown in Fig. 7.16. The input to the charge pump circuits is a constant 3 V DC and the clock operating frequency is chosen to be 1 MHz. The output obtained from both the circuits is a constant DC voltage of 8 V. This voltage is less than the simulated voltage obtained with the same clock frequency and input supply voltage. The drop in the output voltage is attributed to the parasitic capacitances associated with the coupling capacitors and the transistors acting as switches.

The measured results of the four-stage charge pump circuit using off-chip coupling capacitors of value 100 nF is shown in Fig. 7.17 (a). The load capacitor is chosen to be 1 µF and the clock operating frequency is chosen to be 100 KHz. For an input DC voltage of 3 V and output DC voltage of 12.5 V is achieved. The obtained output voltage is greater than four times the input supply. As discussed earlier, the same four-stage charge pump circuit can also be used to generate clocks of higher amplitudes. The experimental results showing the clock output for an input clock of amplitude 3 V is shown in Fig. 7.17 (b). The output clock is out-of-phase with input clock but the amplitude is greater than 2.5 times the input clock amplitude.
Figure 7.16: Experimental results showing the input and output voltages of (a) proposed four-stage charge pump and (b) four-stage Dickson charge pump designs using on-chip capacitors.

(a)

(b)

Figure 7.17: Experimental results showing (a) the input and output voltages of the proposed four-stage charge pump and (b) the input clock and the output clock obtained from the intermediate node using off-chip capacitors.

(a)

(b)
The measured results of the six-stage charge pump circuit using off-chip coupling capacitors of value 100 nF is shown in Fig. 7.18 (a). The load capacitor is chosen to be 1 µF and the clock operating frequency is chosen to be 100 KHz. For an input DC voltage of 3 V an output DC voltage of 17.8 V is achieved. The obtained output voltage is almost equal to six times the input supply. As discussed earlier, the six-stage charge pump circuit can also be used to generate clocks of higher amplitudes. The experimental results showing the clock output for an input clock of amplitude 3 V is shown in Fig. 7.18 (b). The output clock is out-of-phase with input clock but the amplitude is greater than 3 times the input clock amplitude.

The proposed charge pump designs use seven and nine transistors for the four-stage and six-stages, respectively. The transistor count is lower when compared to 12 and 18 transistors for the charge pump design without threshold voltage degradation [9], and 13 and 16 for the area efficient charge pump design [2] for the four and six-stages, respectively.
Figure 7.18: Experimental results showing (a) the input and output voltages of the proposed six-stage charge pump and (b) the input clock and the output clock obtained from the intermediate node using off-chip capacitors.
7.4 Conclusion: Charge Pump Circuits

Four and six-stage charge pump designs have been presented based on boosting the clock voltage internally. The designs are implemented in 1.5 μm n-well CMOS process for operation in 1.2 V – 3 V power supply voltage range. The designs are simulated in SPICE and compared with the performance of Dickson charge pump. It is shown that the proposed four-stage and six-stage charge pump designs offer increased output voltages in comparison to other reported designs including Dickson charge pump. The experimental results obtained at 3 V power supply voltage and 3 V input clock show that the proposed four-stage and six-stage charge pump designs offer output voltages four and six times the power supply voltage, respectively. It is also shown that the charge pumps can also be used to generate clock voltages higher than the input clock voltage. The proposed designs uses minimum number of transistors is area efficient and suites for bio-medical applications. The concept of boosting the clock internally has been used in implementation of a battery powered Bio-implantable Electrical Stimulation (BESS) chip presented in the following chapter.
Chapter 8

Revised Bio-implantable Electrical Stimulation System (BESS) Integrated Circuit

A revised second version integrated circuit design and implementation of the Bio-implantable Electrical Stimulation System (BESS) is presented. The BESS IC is used for Functional Neuromuscular Stimulation (FNS) of gastric muscles and its first version is presented in detail in Ref. [15]. However, this IC [15] has serious problems, which obstruct its normal operation for generating the required output defined by the specifications.

8.1 Problems in the BESS IC Design (Older Version)

In this section, design problems associated with the designed BESS IC [15] and the solutions are discussed. The BESS IC as shown in Fig. 8.1 [15] can be divided into three major blocks.

**Block 1: Battery Switching Circuit (BSC)**

The block 1 consists of a voltage reference VR1, two voltage detector circuits VD1 and VD2, two logic blocks L1 and L2, the main control logic CL1, four charge pumps and the four transistor switches forming the battery switching circuit.

**Block 2: Pulse Generator Circuit (PGC)**

This block consists of two astable multivibrators AM1 and AM2, pulse generators PG1 and PG2 and the power on reset circuit PR1 forming the pulse generating block.

**Block 3: Output Stage (OS)**

In this block, the voltage reference VR2, voltage regulator VR3, the charge pump circuit, the AND gate, the inverter and the control for dual polarity pacing circuit are combined to form the final output stage.
Figure 8.1: Overview of the Bio-implantable Electrical Stimulation System (BESS) IC [15].
8.1.1 Switching Between the Two Batteries

The BESS IC chip should always be connected to a charged battery at all times so that Block 2 and Block 3 operates as per the specifications reported in Ref. [15] and also the IC should be able to switch between the two batteries alternatively for efficient usage of the two batteries. Once Bat-1 is discharged, the rest of the circuit formed by Block 2 and Block 3 should be connected to Bat-2 during which Bat-1 is charging and once Bat-2 has discharged the rest of the circuit should shift back to Bat-1 while Bat-2 goes to the charging cycle and the operation continues. But in the design shown in Fig. 8.1, Block 1 does not perform in the above mentioned manner. The operation of Block 1 is described in the following.

While Bat-1 is charging, the main circuit is connected to Bat-2 and the moment the Bat-1 gets charged the control logic CL1 connects the main circuit to Bat-1 independent of the charge stored in Bat-2. This causes an unequal number of charging and discharging cycles between the two batteries and reduces the efficiency of the two batteries and also of the BESS IC over longer periods of time. This problem has been solved by designed a new circuit which does not require the control logic CL1, the two logic blocks L1 and L2 and the four charge pumps CP1 to CP4. Since the new circuit eliminates the use of the control logic, logic blocks and the charge pump it saves the real estate on silicon and also reduces the power consumption.

8.1.2 Charge Pump Design

The four stage charge pump that has been used in the output stage or Block 3 uses 12 external capacitors to boost the voltage from 3 V to 10 V. The usage of such high number of capacitors takes more number of the IC pins and also increases the power consumption. The new design uses a different kind of charge pump design. In literature there are different kinds of charge pump designs [12, 17] but to decrease the number of externally connected capacitors and
also to have a simpler design, Dickson charge pump [16] based design is used. A five stage charge pump is designed which uses just 5 external coupling capacitors and a load capacitor to boost the voltage from 3 V to more than 10 V. The older design uses an external off-chip clock to operate the charge pump but the new design has an in-built clock generator circuit designed using an astable multivibrator circuit.

8.1.3 Charge Leakage Problem

The output stage (Block 3) has an AND gate and a buffer combination before triggering the external electrodes through the dual polarity pacing circuit. The buffer is not shown in Fig. 8.1 instead an inverter is shown. The two inverters forming the buffer as shown in Fig. 8.2 has a charge leakage path from the load capacitor of the charge pump to ground. Hence the output capacitor of the charge pump storing the voltage 10 V has the possibility to discharge and can supply lower voltages to the electrodes. If the discharging cycle of the load capacitor is faster than the charging cycle then there is every chance that the capacitor can be shorted to ground. The operation is explained as follows. When the output of the AND gate is 0 V, the PMOS in first inverter is turned ON and NMOS is turned OFF but when a transition from 0 V to 3 V occurs, the PMOS is not completely turned OFF and at the same time NMOS is turned ON, hence there is a conduction path to ground through which the charge pump load capacitor can discharge. This will cause an indeterminate output at the electrodes. To overcome this problem a novel idea has been developed which uses a boosting capacitor at the first inverter stage to remove the discharge path. The new BESS IC has been designed to eliminate the above mentioned problems and the design is supported with simulation and experimental results.
Figure 8.2: Figure showing the discharge path in the output stage of the BESS IC of Fig. 8.1.
8.2 Revised BESS IC Design Overview

With the same specifications as that of the older BESS IC [15], modified BESS IC has been designed. The block diagram representation of the design is shown in Fig. 8.3. This design satisfies the specification of generating pulses of amplitude 10 V at a frequency of 100 Hz with a duty cycle of 4.5 % occurring for 3.23 seconds and remaining at 0 V for the next 5.15 seconds. The process repeats every 8.38 seconds as explained in Ref. [15]. The new design can also be divided into three major blocks as

Block 1: New Battery Switching Circuit

This block consists of the battery switching circuit (BSC) designed using two voltage references VR1 and VR2 and two voltage detector circuits VD1 and VD2, four switches and a start up circuit as shown in Fig. 8.3.

Block 2: Pulse Generator Circuit

This block is same as the one shown in Fig. 8.1.

Block 3: New Output Stage

The new output stage has major modifications from the earlier design. This block contains a five stage Dickson charge pump circuit followed by a pulse booster circuit. This circuit provides the pulses of amplitude 10 V to the dual polarity pacing circuit which triggers the two electrodes alternatively. The receiver coil receives the induced signal from an intermittently used external transmitter coil and using the rectifier circuit the AC signal from the receiver coil is converted to DC signal and is used to recharge the batteries through a voltage regulator. The voltage regulator maintains a constant voltage of 4.2 V to charge the discharged battery to 3.7 V. Even though the voltage regulator is connected to both the batteries it will not have any effect on the charged battery since no current can flow through the charged battery. It
only recharges the discharged battery. As the external transmitter coil is used intermittently, battery charging is also performed intermittently. The specifications for the battery and time for charging are given in Ref. [15]. The battery switching circuit (BSC) shown as Block 1 in Fig. 8.3 does the function of alternatively shifting between the two batteries such that at any given time the rest of the circuit comprised of Block 2 and Block 3 is always connected to a charged battery. The BSC uses two voltage reference and two voltage detector circuits and needs a start up circuit so that when both charged batteries are connected to the main circuit Bat-2 is given the preference. The output of the BSC is a constant 3 V DC voltage and is used to power Block 2 and Block 3. The pulse generator circuit shown as Block 2 in Fig. 8.3 is used to generate pulses of amplitude 3 V. Figure 8.4 (b) shows the required nature of output from the Block 2. The design specifications call for pulses of frequency 100 Hz with a pulse width of 0.45 ms having amplitudes in the voltage range 3 V as shown in Fig. 8.4 (b). These pulses are present during the 3.23 s pulse ON time of Fig. 8.4 (a).

The power on reset circuit PR1 is used to initialize the pulse generator circuit as soon as power is applied to the system. The output stage which is shown as Block 3 in Fig. 8.3 is used to boost the 3 V pulse amplitude obtained from the pulse generator circuit to 10 V. The output stage contains a five stage Dickson charge pump which is used for DC-DC conversion. The charge pump outputs a 10 V DC voltage from an input DC voltage of 3 V. It needs a clock signal for DC-DC conversion and the internal clock is provided using an astable multivibrator AS3 circuit. The output of the charge pump circuit is a constant DC voltage and acts as the power supply to the pulses booster circuit (PBC). The PBC circuit is designed using a new technique of internal clock voltage boosting.
Figure 8.3: Block diagram of the revised BESS IC design.

Figure 8.4: Design specifications for the output pulses from the BESS IC chip. (a) Pulse waveform envelope of frequency 0.12 Hz with 38.5 % ON time. (b) Required output pulses present during pulse ON time in (a) above with frequency 100 Hz and duty cycle of 4.5 %.
The PBC boosts the output pulse amplitude of 3 V from the pulse generator circuit to the required amplitude of 10 V. These 10 V pulses are applied to the two electrodes in an alternate fashion using the control for dual polarity circuit.

8.2.1 Battery Switching Circuit (BSC)

The battery switching circuit (BSC) forms a crucial part of the BESS design. It helps to connect the main circuit to a charged battery at all times. The circuit provides the logic to alternatively shift between the two rechargeable batteries. Using the batteries alternatively helps to have longer and efficient use of the batteries as each battery can have an equal number of discharging and charging cycles. Figure 8.5 shows the implementation of the BSC.

The battery switching circuit shown has two voltage reference and voltage detector circuits. The voltage reference and detector circuits used here are same as the ones discussed in Ref. [15]. The voltage reference circuit gives a constant voltage of 1.8 V for any variation in supply voltage from 3 V to 4.2 V. The voltage detector circuit detects the battery voltage when it falls below 3.05 V or when the battery voltage goes above 4.2 V. The output of the voltage detector circuit is logic ‘0’, represented as 0 V, if the voltage stored in the battery falls below 3.05 V. Otherwise, the output remains at logic ‘1’ which in the present application is represented using the voltage range 3 V to 3.7 V. Four switches S1-S4 are used in which the two PMOS switches S1 and S2 are used for switching operation and the NMOS switches S3 and S4 are used to provide the voltage supply to the main circuit. The operation of the BSC can be explained by assuming that fully charged batteries of voltage 3.7 V each are connected to the BESS IC.

Initially the gate voltages of switches S1 and S2 are unknown the IC can have 0 V at the gates and hence both the switches are turned ON and both the batteries tend to provide the supply to the blocks 2 and 3.
Figure 8.5: A block diagram of the battery switching circuit (BSC).
To avoid this situation a start up circuit has been designed as shown in Fig. 8.5. This is a simple circuit with two inverters connected in a buffer configuration only difference being that the power supply of inverter I1 is Bat-1, while the power supply of the inverter I2 is the drain voltage of switch S2. As both switches are ON in the given situation, the output of the voltage detector VD2 is HIGH and the output of the inverter I1 is LOW which pulls the output of the inverter I2 to HIGH turning OFF the switch S1. In this case Bat-1 is temporarily disconnected from the circuit and Bat-2 alone is used to supply power to Block 2 and Block 3. It is also possible that when two fully charged batteries are connected, the output of the voltage detector VD1 can also be HIGH. In this case, Bat-2 is disconnected and Bat-1 provides the supply voltage. But since it is hard to predict which voltage detector output would be in the HIGH state, the start up circuit is helpful in avoiding the race between the two batteries. With the use of the start up circuit, Bat-2 is connected to the main circuit and whenever the voltage in Bat-2 falls below 3.05 V, the output of the voltage detector VD2 is LOW. This causes a change in the output of inverter I1 which goes to logic HIGH from the earlier state of logic LOW and the output of inverter I2 goes to logic LOW state, switch S1 is turned ON and Bat-1 is connected and supplies the power to Blocks 2 and 3. Here it should be noted that even though the power supply to the inverter I2 is the drain of switch S2 which is below 3.05 V, it does not affect the output of inverter I2 since the PMOS of the inverter is turned OFF. During the time when Bat-1 is supplying power and if transmitter coil is connected, the induced voltage in the receiver coil is rectified and is used to recharge Bat-2. As discussed earlier in Sec. 8.1.1, since Bat-1 is already charged only Bat-2 will be recharged to 3.7 V. Whenever the voltage of Bat-1 falls below 3.05 V the output of the voltage detector VD1 goes LOW and turns ON the switch S2 since the output of VD1 is directly connected to the gate of S2. As Bat-2 has already been charged, it will now be
able to supply power to the main circuit and since the output of the voltage detector VD2 is HIGH, Bat-1 is disconnected from the system and can be recharged when ever the transmitter coil is connected to the system. The output of the battery switching circuit sees a drop in battery voltage by the threshold voltage of the NMOS transistors S3 and S4. Two transistors S3 and S4 are needed so as two separate the Bat-1 from Bat-2.

Figure 8.6 shows the layout of the complete battery switching circuit and the simulation results of the circuit are shown in Fig. 8.7. Figure 8.7 has been divided into different regions. Each region indicates one of the two batteries that is supplying power to the Blocks 2 and 3. The simulation shown here is for illustration only where the time axis has been taken in the range of µs, but in actual, the batteries take hours to discharge and charge.

At the beginning both the batteries are at 3.7 V, and as discussed above the output follows the Bat-2 with a drop of $V_T$ which is being the threshold voltage of switch S4. Indicating that Bat-2 is providing the supply, the region is marked as Bat-2 in the Fig. 8.7. At 18 µs, Bat-2 discharges to 2 V but the output voltage does not follow Bat-2 instead stays at the same voltage indicating that the supply is now being given by Bat-1 and the region is marked as Bat-1. In the meantime, Bat-2 has been charged to 3.7 V but the lack of any transition in the output indicates that Bat-1 is still providing the voltage to the main circuit and hence the next region is also marked as Bat-1. From this it can very clearly be stated that the battery switching circuit shifts to the other battery if and only if the voltage in the first battery falls below the voltage limit set by the voltage detector circuit which in the present case is 3.05 V.
Figure 8.6: Layout of the Battery Switching Circuit.

Figure 8.7: Simulation results of the battery switching circuit.
At the 45 µs mark, Bat-1 starts to discharge and since Bat-2 is fully charged the supply is shifted back to Bat-2 and after a transient spike the output settles back to the constant voltage. In a continuous manner the battery switching circuit alternatively switches between the two batteries so as to connect block 2 and block 3 to a charged battery.

### 8.2.2 Charge Pump Design

Charge pump is a DC-DC converter which helps to get higher DC output voltages than the DC supply voltage. For the BESS design, in order to get 10 V amplitude pulses from a 3 V DC, a charge pump circuit is best suited for the application. For the new BESS IC design, a five stage charge pump based on Dickson design has been designed. The charge pump uses capacitors in each stage to store and transfer the charge to the successive stages, achieving the voltage boost in each stage.

Figure 8.8 shows the circuit schematic of the five stage Dickson charge pump circuit [16] repeated here for completeness. The operation is very similar to the four stage Dickson charge pump circuit explained in Chapter 7 in Sec. 7.1. The charge pump needs an internal clock generator circuit which provides the complimentary clocks for performing the pumping operation. By choosing the values for the resistor and capacitor of an astable multivibrator [15], complementary clocks of required frequency can be generated.

The gate oxide breakdown strength also poses a limitation on the maximum output voltage that can be achieved using the charge pump circuit. The breakdown strength of the gate oxide is given by $E = V/d$ where $d$ is the thickness of the gate oxide and its value is 300 Å, the oxide strength $E$ is given by 8 to 11 MV per cm or 0.08 – 0.11 V/Å. Thus, the maximum voltage that can be applied to the gate of the MOSFET without causing breakdown voltage is 24 to 33 V. In designing the charge pump, these limitations have been taken into consideration.
Figure 8.9 shows the layout of the five stage charge pump circuit. The layout shows the use of external capacitors. Using internal capacitors, whose range can only be in pF, it is not possible to achieve high current drives in the range of mA and also internal capacitors have parasitics associated with them which would degrade the gain of the charge pump. External capacitors are used for these reasons. External capacitors are shown in the layout as C1 through C5, where C1_top is indicative of the capacitor top plate and C1_low for the bottom plate. The load capacitor is shown as C_{load}. Figure 8.9 also shows the layout of the astable multivibrator which is used to generate the internal clock signal for the charge pumping operation. The C_{as} and R_{as} in Fig. 8.9 are representative of the external capacitor and resistor needed for the astable multivibrator circuit. It can be observed from the layout that the metal lines are made wide enough for carrying the high currents in the range of mA and also to reduce the internal parasitic resistance. The internal parasitic resistance is decreased by increasing the width of the metal line, given by \( R = R_s \times W/L \), where \( R_s \) is the sheet resistance. W and L are the width and length of the metal line, respectively. The layout has been done in 1.5 \( \mu \)m n-well CMOS process and the current density value of the thick metal 1 line shown in the layout is given by 1 mA / (1 \( \mu \)m of metal width). So for a current drive of 10 mA, a metal line of width more than 10 \( \mu \)m is chosen to avoid the electro-migration [20]. The charge pump is operated with a clock frequency of 1 MHz generated using the internal astable multivibrator circuit. The resistor and the capacitor value for the multivibrator are taken to be 10 k\( \Omega \) and 45 pF, respectively and the simulation results are shown in Fig. 8.10. The obtained clk and \( \overline{clk} \) output waveforms are of amplitude 3 V with time period of 1 \( \mu \)s. The simulation results of the charge pump are shown in 8.11.
Figure 8.8: Circuit schematic of a five stage Dickson charge pump circuit.

Figure 8.9: Layout of the five stage charge pump and the astable multivibrator used for generating the complementary clock signals for the charge pump.
Figure 8.10: Simulated clock output waveforms of the internal clock generator circuit.

Figure 8.11: Simulated input and output of the five stage charge pump
The external coupling capacitors for the charge pump are chosen to be 100 nF and a load capacitor value of 1 µF. The input to the charge pump is a constant DC voltage given from the battery switching circuit. The simulation time is shown to be 10 ms since the output voltage reaches a steady state voltage of 10 V with in short time. The rise time of the charge pump which is defined as the time it takes to raise from 10 % to 90 % of its steady state is less than 1 ms. The charge pump output is given to the pulse booster circuit which produces pulses of amplitude 10 V which are ON for a minimum time of 0.45 ms and OFF for 9.55 ms as discussed in Sec. 8.2. During the pulse ON time of 0.455 ms, the load capacitor of the charge pump can discharge so it is very important for the charge pump to restore back to 10 V in the OFF time of 9.5 ms. Therefore, in the next ON time, the output is 10 V. Since the rise time is less than 1ms, the charge pump meets the requirement well and can supply constant 10 V DC for the pulse booster circuit for continuously generating pulses of amplitude 10 V as per the design specifications.

8.2.3 Pulse Booster Circuit (PBC)

The Pulse Booster Circuit (PBC) is used to boost the pulse amplitude from 3 V to 10 V. The circuit has been designed with a new technique of boosting the pulse amplitude. A boosting capacitor is used to eliminate the leakage path that was present in the previous design as discussed in Sec. 8.1.3. The circuit diagram for the pulse booster circuit is shown in Fig. 8.12. The voltage stored on the load capacitor of the charge pump acts as the power supply to the PBC. The load capacitor of the charge pump is charged to a steady state voltage of 10 V. The pulses of amplitude 0 to 3 V from the pulse generator circuit are provided as the input to the PBC. Transistors M1 and M2 are diode connected transistors and conduct current in one direction only. These transistors provide the conduction path for current to charge the capacitor \( C_{\text{boost}} \) by uni-directional charge sharing from \( C_{\text{load}} \) to \( C_{\text{boost}} \).
Figure 8.12: Circuit schematic of the pulse booster circuit (PBC).
The transistor combination of M3 to M6 form a buffer circuit whose output is same as the input to the NMOS transistor M4 except from the amplitude which is boosted to voltage stored on the load capacitor \( C_{load} \). When the input pulse is at 0 V, capacitor \( C_{boost} \) gets charged to

\[
V_a = V_{\text{cloud}} - V_{T1} - V_{T2}
\]

where \( V_{\text{cloud}} \) is the voltage stored on \( C_{load} \) and \( V_{T1} \) and \( V_{T2} \) are the threshold voltages of transistors M1 and M2. Since the output from the pulse generator circuit is directly connected to the gate of NMOS transistor M4 and as the input pulse is at 0 V, M4 is in OFF state. The gate voltage of the PMOS transistor M3 is same as the voltage stored on \( C_{boost} \) which is \( V_a \) and the source voltage of M3 is \( V_{\text{cloud}} \). Since the gate-to-source voltage of M3 is \((-V_{T1} – V_{T2})\) is less than the threshold voltage \( V_{T3} \) of the PMOS, the PMOS transistor M3 turns ON and tries to pull the gate of the inverter formed by M5 and M6 to logic HIGH which in the present case is the voltage \( V_{\text{cloud}} \). This pulls down the output of the PBC to be LOW state i.e., to 0 V.

When the input pulse has a transition from 0 V to 3 V the voltage on the capacitor \( C_{boost} \) is boosted by 3 V and voltage on the top plate of the \( C_{boost} \) reaches \( 3 + V_a \). Since the gate voltage of transistor M3 is same as the voltage on the top plate of \( C_{boost} \), the gate-to-source voltage of PMOS transistor M3 is \( 3 – V_{T1} – V_{T2} \), it is greater than the threshold voltage of PMOS, M3 so the transistor M3 turns OFF. The 3 V amplitude pulse is also the input to transistor, M4 and as the gate-to-source voltage of NMOS transistor, M4 is greater than the threshold voltage of NMOS, the transistor, M4 turns ON and tries to pull down the gate of the inverter formed by M5 and M6 to ground. This causes the output of the PBC to be at logic HIGH which in the present case is \( V_{\text{cloud}} \). When the input pulse amplitude is 0 V, the output pulse amplitude of the PBC is 0 V and whenever the input pulse amplitude in 3 V, the output pulse amplitude of the PBC is \( V_{\text{cloud}} \). The number of diode connected transistors in the PBC design is chosen to be two and are shown in Fig. 8.12 as M1 and M2. The logic for deciding the number of transistors is to provide enough
threshold voltage drops such that the PMOS transistor M3 is turned OFF and turned ON whenever the input pulse is HIGH and LOW, respectively.

Figure 8.13 shows the layout of the PBC showing the boosting capacitor $C_{\text{boost}}$. A small value capacitor of 8 pF is chosen for performing the boosting operation so that there is no loading affect on the pulse generator circuit. Since $C_{\text{boost}}$ is used to drive the gate of the PMOS transistor, M3, which does not pose any serious design difficulties, a small value for the capacitor is justified. The capacitor layout has been done using poly 1 over poly 2 as the poly layer offers more capacitance per unit area and also has lesser parasitic capacitances associated with it. The capacitor is placed inside a guard ring, implemented using n-well, so as to avoid the charge leakage due to interference from external circuits.

The simulation results for the PBC circuit are shown in Fig. 8.14. The PBC is simulated by using a constant 10 V DC acting as the power supply to the circuit. The input is given by a pulse train of amplitude 3 V at frequency 100 Hz with a duty cycle of 4.5 %. The output pulses and input pulses are shown on the same voltage scale. It can observed from the Fig. 8.14 that the pulse boosting circuit outputs pulses of amplitude 10 V from an input pulse train of amplitude 3 V while restoring the frequency and duty cycle of the input pulses.

### 8.2.4 Dual Polarity Pacing (DPP) Circuit

The 10 V amplitude pulses from the PBC need to trigger the two connected electrodes alternatively and to achieve this Dual Polarity Pacing (DPP) circuit has been designed. The DPP circuit has also been discussed in previous BESS IC chip but the circuit was not included in the IC due to unavailability of area on the IC. The gate level schematic of the modified DPP circuit is shown in Fig. 8.15. The circuit uses a master slave JK flip flop to alternate the pulses between the two electrodes.
Figure 8.13: Layout of the pulse booster circuit (PBC).

Figure 8.14: Simulated pulses showing the input and output of the PBC.
The input to the DPP circuit which is also the clock to the JK flip flop is a pulse train of 10 V amplitude provided from the pulse booster circuit. By connecting the J and K both to the charge pump output which is a constant 10 V DC, the JK flip flop acts as a toggle flip flop also called as T-flip flop. The output of the T-flip flop toggles at every falling pulse edge hence called as negative edge triggered flip flop. Clear input of the flip flop is also connected to charge pump output so that it is always in HIGH state, if the clear input is in LOW state the output of the flip flop is LOW. The output of the flip flop here refers to the Q output. $\overline{Q}$ is the complement of the Q output. The layout of the DPP circuit is shown in Fig. 8.16. The metal lines in the layout are made wider so as to decrease the internal parasitic resistance that could affect the output voltage when driving the two electrodes. The simulation results of the DPP circuit are shown in Fig. 8.17. The input pulse train acts as the clock signal to the JK flip flop which is also a T-flip flop as discussed above. At every clock falling edge the outputs of the flip flop Q and $\overline{Q}$ changes their state from the previous state. At the raising edge of the clock at time 0 ms in Fig. 8.17, the output of the gate AND 1 which is the Electrode 1 is at logic HIGH as both the input of the AND 1 are at logic HIGH. The output of the gate AND 2 which is Electrode 2 is at logic LOW since the $\overline{Q}$ output is at logic LOW. Q output goes to logic LOW and $\overline{Q}$ output goes to logic HIGH at the falling edge occurring at time 0.45 ms in Fig. 8.17. At the next raising clock edge occurring at time instant 10 ms the Electrode 1 will be at logic LOW and Electrode 2 will be at logic HIGH state as observed in Fig. 8.17. The pulses thus alternate between the two electrodes with the application of the input pulses.
Figure 8.15: Block diagram of the dual polarity pacing (DPP) circuit.

Figure 8.16: Layout of the dual polarity pacing (DPP) circuit.
Figure 8.17: Simulated results showing the input and output pulses of the DPP circuit.
BESS IC layout in 1.5 μm n-well CMOS and in a 40-pin analog padframe is shown in Fig. 8.18. The IC has been divided into three blocks as explained in Sec. 8.2 for illustrating the three major circuits in the System. Block 1 corresponds to the Battery Switching Circuit (BSC), Block 2 is the Pulse Generator Circuit (PGC) and Block 3 indicates the Output stage which is used to trigger the two electrodes connected external to the IC.

### 8.3 Experimental Results and Discussion

Figure 8.19 shows the microphotograph of the new BESS IC chip. In the Fig. 8.19, the battery switching circuit (BSC), pulse generator circuit (PGC) and the output stages are shown in blocks. The measured output of the battery switching circuit is observed to be 2.2 V which is slightly less than the design value of 3 V. This drop in the output voltage of the BSC is attributed to the loading effect of the PGC and the output stage. The designed five stage Dickson charge pump is tested using off-chip capacitors of 100 nF. The charge pump is able to deliver the required output voltage and is evident in the experimental results shown for the PBC. The experimentally measured output and input of the PBC are shown in Fig. 8.20. The output of the PGC which is the input to the PBC is measured to have a pulse frequency of 103 Hz and a duty cycle of 5 %. The amplitude of the pulses is at 3 V since the PGC and the output stage are supplied with a power supply of 3 V. The PGC output is provided as the input to the PBC. The PBC output as shown in the Fig. 8.20 is able to generate 9.9 V pulses and with same frequency and duty cycle as that of the PGC output. From the output of the PBC it is evident that the five stage charge pump used in the output stage is able to deliver a constant DC voltage of 9.9 V. The output of the PBC is supplied as the input to the DPP circuit whose output is shown in Fig. 8.21. The DPP circuit is able to generate alternate pulses from the PBC output. These pulses are of amplitude 9.9 V and due to their alternating nature can be used for bipolar pacing.
Figure 8.18: Complete BESS IC layout shown in a 40-pin padframe.

Figure 8.19: Microphotograph of the BESS IC chip.
Figure 8.20: Experimental results showing the input and output waveforms of the Pulse Booster Circuit.

Figure 8.21: Experimental result showing the two outputs of the dual polarity pacing (DPP) circuit.
8.4 Conclusion: Revised BESS IC

A modified Battery Powered Electrical Stimulation System (BESS) IC has been designed which overcomes the problems faced in the previous design. The redesigned BESS IC generates pulses of amplitude 9.9 V which can be used to alternatively trigger the two electrodes used for stimulating the gastric muscles. The problems faced by the previous BESS IC design have been analyzed and different circuit techniques have been developed to overcome problems. The second revised BESS IC version generates 10 V pulses at a frequency of 100 Hz and a duty cycle of 4.5%. This has been achieved using 3.7 V rechargeable batteries. The IC chip incorporates a novel battery switching circuit for controlling the supply from the batteries to the pulse generator circuit and the output stage. The required pulse amplitude is achieved from a low battery voltage through a charge pump circuit and a pulse booster circuit developed based on a new concept to boost the pulse amplitude. The fabricated chip resulted in desired bipolar pulses of 9.9 V amplitude with 103 Hz frequency and 5% duty cycle.
A programmable CMOS decimator for sigma-delta analog-to-digital converter has been presented in Part I and new charge pump circuits have been proposed in Part II. The Part II also discusses the design of a revised BESS IC which incorporates new battery switching and pulse booster circuits. The programmability feature in the decimator has enabled to operate the sigma-delta ADC with two different oversampling ratios. By operating the ADC at oversampling ratios of 64 and 16 an output resolution of 10-bit and 7-bit are achieved. The decimator designed for the ADC is a 2\textsuperscript{nd} order Cascaded Integrator Comb (CIC) filter. The ADC can also be programmed to work with more than two oversampling ratios by suitably designing the circuitry based on the presented work. However, operating the ADC with more number of oversampling ratios can make the circuitry complex. Innovative circuit design technologies are to be developed for easy programmability and are suggested for the future work.

The new charge pump circuits presented in Part II which are developed using the new technique of internal clock voltage boosting achieve higher DC output voltages which are higher than the values reported in literature. The developed technique of internal clock voltage boosting has also been applied to design a pulse boosted circuit in the BESS IC to generate pulses of 10 V amplitude. The charge pump circuits presented in this work ignores the body effect on MOS transistors which should, however, be considered and is suggested for the future work.
References


Appendix A

SPICE Parameters from MOSIS (www.mosis.org)

* LOT: T32P                  WAF: 8303  
* DIE: N_Area_Fring          DEV: N3740/10  
* Temp= 27  

.MODEL CMOSN NMOS ( 
  LEVEL = 3  
+ TOX    = 3.07E-8         NSUB   = 1.6853E15   GAMMA  = 0.6872032  
+ PHI    = 0.7            VTO     = 0.5943924   DELTA  = 0.4809824  
+ UO     = 591.0776142    ETA      = 1.191113E-3  THETA  = 0.0767515  
+ KP     = 7.477226E-5     VMAX    = 1.963112E5   KAPPA  = 0.5  
+ RSH    = 0.1292379       NFS      = 5.208477E11  TPG    = 1  
+ XJ     = 3E-7            LD       = 0           WD     = 6.710568E-7  
+ CGDO   = 1.78E-10        CGSO    = 1.78E-10    CGBO   = 1E-10  
+ CJ     = 2.704625E-4      PB      = 0.7318187   MJ     = 0.5  
+ CJSW   = 1.353332E-10    MJSW    = 0.0501583  )  

*LOT: T32P                  WAF: 8303  
* DIE: P_Area_Fring          DEV: P3740/10  
* Temp= 27  

.MODEL CMOSP PMOS ( 
  LEVEL = 3  
+ TOX    = 3.07E-8         NSUB   = 1E17           GAMMA  = 0.4872958  
+ PHI    = 0.7            VTO     = -0.8990733    DELTA  = 0.4233463  
+ UO     = 102.8643057     ETA      = 1.216702E-5  THETA  = 0.1304553  
+ KP     = 2.485475E-5     VMAX    = 3.317472E5   KAPPA  = 100  
+ RSH    = 37.935464       NFS      = 4.741684E11  TPG    = -1  
+ XJ     = 2E-7            LD       = 1E-14        WD     = 1E-6  
+ CGDO   = 2.16E-10        CGSO    = 2.16E-10    CGBO   = 1E-10  
+ CJ     = 3.074102E-4      PB      = 0.7399014   MJ     = 0.4312979  
+ CJSW   = 1.677268E-10    MJSW    = 0.1129143  )
Appendix B

Pin Diagrams

Figure B.1: Pin diagram of the decimator IC (T46B-BH) with input and output connections.
Figure B.2: Pin diagram of the IC (T4BH-AN) containing the charge pump circuits and external components.
Figure B.3: Pin diagram of the modified BESS IC (T4BH-AL) with external components.
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