Testing a CMOS operational amplifier circuit using a combination of oscillation and IDDQ test methods

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TESTING A CMOS OPERATIONAL AMPLIFIER CIRCUIT USING A COMBINATION OF OSCILLATION AND $I_{DDQ}$ TEST METHODS

A Thesis

Submitted to the Graduate faculty of the Louisiana State University and Agricultural and Mechanical College in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

In

The Department of Electrical and Computer Engineering

by

Pavan K Alli
Bachelor of Engineering, Osmania University, 2001
August 2004
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ABSTRACT

This work presents a case study, which attempts to improve the fault diagnosis and testability of the oscillation testing methodology applied to a typical two-stage CMOS operational amplifier. The proposed test method takes the advantage of good fault coverage through the use of a simple oscillation based test technique, which needs no test signal generation and combines it with quiescent supply current (I_{DDQ}) testing to provide a fault confirmation. A built in current sensor (BICS), which introduces insignificant performance degradation of the circuit-under-test (CUT), has been utilized to monitor the power supply quiescent current changes in the CUT. The testability has also been enhanced in the testing procedure using a simple fault-injection technique. The approach is attractive for its simplicity, robustness and capability of built-in-self test (BIST) implementation. It can also be generalized to the oscillation based test structures of other CMOS analog and mixed-signal integrated circuits. The practical results and simulations confirm the functionality of the proposed test method.
CHAPTER 1
INTRODUCTION

With the growing use of analog circuits in commercial mixed-signal integrated circuits and systems, testing of analog integrated circuits is considered as one of the most important problems in analog and mixed-signal integrated circuit design. Analog circuits have traditionally been tested for critical specifications [1] e.g., ac gain over a range of frequencies, common-mode rejection ratio, signal-to-noise ratio, linearity, slew rate, due to the lack of simple fault models. The functional testing usually results in longer test times because of redundant testing. It does not provide either a good test quality or a quantitative measure of test effectiveness or fault coverage. Reducing test time by optimizing the functional test set while achieving the desired parametric fault coverage has also been studied [2]. However, the technique needs a reasonably large number of sample circuits for collecting the test data.

Analog CMOS circuits have also been tested by varying the supply voltage in conjunction with the inputs [3]. This technique aims to sensitize faults by causing the transistors to switch between different regions of operation. A ramped power supply voltage has been used to test faults in op-amp circuits. In [4], an ac supply voltage has been used for improving the fault coverage. Although these techniques have achieved high fault coverage, the number of faults injected was quite small. Using this idea of varying supply voltage and combining it with supply current monitoring [5], larger analog circuits have been tested for short circuit fault detection. But the method suffers from the fact that, gate-source shorts that have negligible effect on supply current and gate-source shorts of transistors which do not switch their mode of operation to any applied stimulus, could not be detected. Other testing methods for analog circuits include
dc testing, power-supply quiescent current (I\text{DDQ}) monitoring and digital signal
processing techniques [6].

On-chip design-for-test (DfT) technique has been suggested as one of the methods
to reduce test costs in analog and mixed-signal integrated circuits [7-18]. An overview of
defect oriented testing and DfT optimization of mixed-signal integrated circuits is
presented in [8, 9]. Several DfT studies have been published, including work on a current
mode DAC where test vectors are optimized and redundancies removed [10], on analog
filters where the controllability and observability are improved to test a number of stages
separately [11-14] and on flash ADC [15,16]. A functional self-test technique, based on
using digital circuitry to generate functional test signals, has been extensively
investigated [17]. This technique also achieves substantial accuracy by moving analog
signal measurement to the digital domain. However, one limitation of the functional test
technique is that the functionality of the filter can only be guaranteed if all specifications
have been tested. In absence of suitable models, one cannot make general deductions
about the ability of a circuit to satisfy all its functional specifications by testing only a
few specifications. Built-in-self test (BIST) is another widely used method, which is
based on measuring the output data and calculating the performance of the system using
an on-chip circuitry [18, 19]. This method reduces complexity of testing for mixed-signal
integrated circuits since all or some of the testing circuitry is incorporated on the silicon.
Generic DfT guidelines that can be applied in the early design stages and practical mixed-
signal BIST could pave the way to satisfying industrial demands for the use of digital
only testers [20, 21].
A DfT based oscillation-testing methodology (OTM) [22] suitable for both functional and defect oriented testing, has been successfully applied to CMOS analog circuits [23-25] such as the analog to digital converters, digitally programmable switched-current bi-quadratic filters, active RC filters, and to circuitry used as embedded blocks [26-28]. OTM is conceptually simple, does not need major circuit modifications and can be implemented in a built-in self-test (BIST) without any additional signal generation circuitry. The test methodology is based on transforming the circuit under test (CUT) into an oscillator whose frequency of oscillation is related to the component values or to the circuit parameters. Hence, a change in the oscillation frequency from its nominal value indicates the possibility of faults in the CUT. OTM is shown to be an effective functional ‘go’ and ‘no-go’ test to verify if the circuit under test conforms to the required specifications. The method achieves good fault-coverage removing test vector generation and output evaluation, while reducing test complexity, area overhead, and test cost. On the other hand, quiescent current (I_{DDQ}) testing shown in Fig. 1.1 is a cost-effective test method to identify defects, which cannot be identified by conventional functional tests and cannot be modeled by classical fault models. I_{DDQ} testing refers to the integrated circuit (IC) testing method based upon measurement of steady state power-supply current. I_{DDQ} stands for quiescent I_{DD}, or quiescent power-supply current. The quiescent current testing has proved to be very efficient for improving test quality of analog circuits [29-31]. The test methodology based on the observation of the quiescent current on power supply buses allows a good coverage of physical defects such as gate-oxide shorts, floating gates and bridging faults.
Figure 1.1: An example to show how $I_{DDQ}$ can be used to detect physical defects.
In this thesis, we discuss a DfT method for a two-stage CMOS amplifier, based on oscillation testing methodology followed by $I_{DDQ}$ testing, for improving fault-coverage, and testability. The proposed test method takes the advantage of good fault coverage through the use of simple oscillation based test technique, which needs no test signal generation and combines it with $I_{DDQ}$ testing to improve the fault coverage. Fault detection is achieved using a simple BICS, which introduces insignificant performance degradation of the CUT, to monitor the power supply quiescent current changes in the CUT and a passive RC network in the feedback path of the amplifier, to enable the CUT to oscillate. The testability has also been enhanced in the testing procedure using a simple fault-injection technique. The approach is attractive for its simplicity, robustness and capability of BIST implementation. It can also be generalized to the oscillation based test structures of other CMOS analog and mixed-signal integrated circuits.

In the digital domain, DfT is well established. With the increasing complexity of the structure of logic circuits, system-timing failures are occurring more frequently. Timing-related failures may be caused by isolated gate delays or process-related timing problems that accumulate along logic paths and prevent the circuit from functioning at the desired speed. The delay faults are becoming critical in deep submicron (DSM) technologies where the interconnection delay exceeds the gate delay. Oscillation Test methodology has successfully been extended to digital circuits [32], for identifying delay and stuck-at faults. This is done by sensitizing all or at least critical paths in the digital circuit under test and then incorporating it in a ring oscillator to test for delay and stuck-at faults in the paths. $I_{DDQ}$ testing has previously been used in identifying bridging, open and stuck-at faults in logic circuits. Hence, the technique discussed above which combines
IDDQ testing with oscillation testing could prove to be an efficient method for testing of
digital integrated circuits as well.

1.1 Testing Methodology

The proposed test methodology shown in Fig. 1.2 consists of first partitioning the
analog /mixed-signal integrated circuit into functional building blocks such as amplifier,
comparator, filter, and data converter and then converting each building block into an
oscillating circuit. In order to implement OTM for the amplifier, it is converted into an
oscillator using a simple first-order derivation feedback circuit. The circuit’s output is
connected to its input via a passive and/or active analog circuit such that, the loop’s
overall gain and phase cause oscillation. The output oscillation frequency from the
amplifier is measured and is compared with the nominal oscillation frequency of the fault
free circuit. If the oscillation frequency lies close to the nominal frequency range, the
CUT is accepted to be fault-free. The nominal frequency range of the CUT is determined
using a Monte-Carlo analysis taking into account the tolerance of significant technology
and design parameters.

The faults that result in loss in oscillation frequency are then diagnosed through
IDDQ testing in a second phase. A built-in current sensor (BICS) has been used [33] for
this purpose to monitor the changes in the quiescent current in the power supply rails.
The BICS used in the present design introduces insignificant performance degradation
and the CUT can be made independent of its operation in the normal mode using only
two control pins. The injected faults are simulated using a simple and novel fault-injection technique [34].
Figure 1.2: Block diagram of the proposed test strategy.
1.2 Advantages of Combined Oscillation and I\textsubscript{DDQ} Testing

In CMOS integrated circuits, the dominant failures are due to gate oxide shorts (GOS). GOS are unexpected connections between the gate and the drain, source, or channel (substrate, p-well, and n-well) that are caused by pinholes in the gate oxide layer. These faults initially may not cause functional failure but will first appear as parametric drifts and can manifest into potential defects over a period of time [35]. Gate oxide shorts can cause degraded signals and can increase leakage currents in CUT. Leakage current based I\textsubscript{DDQ} testing will detect these parametric drifts before they actually change the circuit behavior. In [36, 37], data exists that show that a device that fully passes the logic functional tests but fail the I\textsubscript{DDQ} test, fall in a significant category that functionally fail more frequently earlier than its normal life. Current testing also is an invaluable tool for detecting faults in devices that contain both analog and digital functions on a single substrate [38]. On the other hand oscillation testing combines the advantages of a vectorless test, simple signal analysis procedure, functional as well as defect-oriented testability, cost effectiveness, easy implementation and applicability to large class of mixed-signal circuits. In addition faults which would have negligible effect on the supply current could be monitored for deviation from oscillation frequency, resulting in high fault coverage. Moreover, the oscillation frequency may be considered as a digital signal and therefore can be evaluated using a pure digital circuitry. These characteristics imply that the oscillation-test strategy is very attractive for wafer-probe testing as well as final production testing.
1.3 Chapter Organization

In the following chapters, the methodology, circuit design, oscillation and \( I_{\text{DDQ}} \) testing methods, simulation results, post-layout measurements and experimental results are discussed.

**Chapter 2** explains the basic structure and operation of a two-stage CMOS amplifier, compensation and frequency analysis. It also explains the methodology for oscillation testing, converting the CUT into an oscillator, effects of the amplifier’s open loop gain, location of the dominant pole and unity gain bandwidth on performance of the oscillator. The simulation results for the Monte-Carlo analysis using the Fast Fourier Transform (FFT) for determining the tolerance band of the oscillation frequency have also been described.

**Chapter 3** explains the concept of \( I_{\text{DDQ}} \) testing, design and implementation of the built-in current sensor. The mechanism of fault simulation and fault detection in the amplifier using the BICS is explained.

**Chapter 4** describes the simulation results and design considerations for the combined oscillation and \( I_{\text{DDQ}} \) testing method. Finally, a description of the fault detection and coverage of the amplifier using a combined testing procedure is presented and simulations are included. Experimental results on the fabricated device are also presented and compared with the corresponding simulated values.

**Chapter 5** provides a summary of the work presented and scope for future work.

**Appendix A** presents the MOS model parameters used for the design.

**Appendix B** presents the chip-testing procedure and pin numbers of the designed chip.
CHAPTER 2
DESIGN FOR TEST OF A TWO-STAGE CMOS OPERATIONAL AMPLIFIER USING OSCILLATION TESTING METHODOLOGY

CMOS operational amplifier is a core element of almost all analog and mixed-signal systems. If the amplifiers are proven to be fault-free, the fault coverage would significantly be improved. In this chapter, the testing methodology called oscillation testing used for testing operational amplifiers is presented. Before introducing the testing methodology, the design and the important frequency domain parameters of the operational amplifier are presented in the next discussion.

2.1 Design of a CMOS Operational Amplifier

An ideal op-amp with a single-ended output has a differential input, infinite voltage gain, infinite input impedance and zero output impedance. A conceptual schematic diagram of an operational amplifier is shown in Fig. 2.1. Op-amps and a few passive components can be used to realize such important functions as summing and inverting amplifiers, integrators, and buffers. The combination of these functions and comparators can result in many complex functions, such as high-order filters, signal amplifiers, analog-to-digital (A/D) and digital-to-analog (D/A) converters, input and output signal buffers, and many more.

A typical high performance operational amplifier is characterized by a high open loop gain, high bandwidth, very high input impedance, low output impedance and an ability to amplify differential-mode signals to a large extent and at the same time, severely attenuate common-mode signals. The design of an operational amplifier consists of three functional building blocks as shown in Fig. 2.2. First, there is an input
Figure 2.1: Ideal operational amplifier.
Figure 2.2: Block diagram of an integrated operational amplifier.
differential gain stage that amplifies the voltage difference between the input terminals, independently of their average or common-mode voltage. Most of the critical parameters of the op-amp like the input noise, common-mode rejection ratio (CMRR) and common-mode input range (CMIR) are decided by this stage. The differential to single-ended conversion stage follows the differential amplifier and is responsible for producing a single output, which can be referenced to ground. The differential to single-ended conversion stage also provides the necessary bias for the second gain stage. Finally, additional gain is obtained in the second gain stage which is normally a common-source gain stage that has an active load. Capacitor, $C_C$ is included between the differential and the common-source stages to ensure stability when the amplifier is used with feedback. An output stage can be added to provide a low output resistance and the ability to source and sink large currents, but in this design we are not employing it since it is not necessary in the present work. In the following subsections, the description as well as the design methodology of each of the stages mentioned above is presented.

2.1.1 A Two-Stage CMOS Amplifier Topology

Figure 2.3 shows the circuit diagram of a two-stage, internally compensated CMOS amplifier used for the testing. The circuit provides good voltage gain, a good common-mode range and good output swing. Before the analysis of the op-amp is done, some of the basic principles behind the working of MOS transistors are reviewed. The first stage in Fig. 2.3 consists of a p-channel differential pair $M_1$-$M_2$ with an n-channel current mirror load $M_3$-$M_4$ and a p-channel tail current source $M_5$. The second stage consists of an n-channel common-source amplifier $M_6$ with a p-channel current-source
Figure 2.3: A two-stage CMOS operational amplifier.
load M7. The high output resistances of these two transistors equate to a relatively large gain for this stage and an overall moderate gain for the complete amplifier. Because the op-amp inputs are connected to the gates of MOS transistors, the input resistance is essentially infinite when the amplifier is used in internal applications. The sizes of the transistors were designed for a bias current of 100 µA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product.

2.1.2 Current Mirrors

Current mirrors are used extensively in MOS analog circuits both as biasing elements and as active loads to obtain high AC voltage gain [40,41]. Enhancement mode transistors remain in saturation when the gate is tied to the drain, as the drain-to-source voltage ($V_{DS}$) is greater than the gate-to-source voltage ($V_{GS}$) due to the threshold voltage ($V_{th}$) drop, i.e.,

$$V_{DS} > V_{GS} - V_{th}$$

(2.1)

Based on Eq. (2.1), constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor. Figures 2.4(a) and (b) show the p-MOS and n-MOS current mirrors design. A p-MOS mirror serves as a current source while the n-MOS acts as a current sink. The voltage developed across the diode-connected transistor is applied to the gate and source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, the currents when both transistors are in the saturation region of operation, are governed by the following equation (2.2) assuming matched transistors. The current ratio $I_{OUT}/I_{REF}$ is determined by the aspect ratios of the transistors. The reference current that was used in the design is 100 µA. The desired
V_{DD} = +2.5 V

\[ I_{\text{REF}} = 100 \mu A \]

\[ I_{\text{OUT}} \approx 200 \mu A \]

Figure 2.4(a): p-MOS current mirror.

V_{SS} = -2.5 V

\[ I_{\text{REF}} = 50 \mu A \]

\[ I_{\text{OUT}} \approx 50 \mu A \]

Figure 2.4(b): n-MOS current mirror.
output current is 200 µA. For the p-MOS current mirror, we can write,

\[ \frac{I_{\text{OUT}}}{I_{\text{REF}}} = \frac{(W_7/L_7)}{(W_8/L_8)} \]  

(2.2)

For \((W_7/L_7)/(W_8/L_8) = 2\),

\[ I_{\text{OUT}} = 2 \times I_{\text{REF}} \cong 200 \text{ µA} \]  

(2.3)

For identical sized transistors, the ratio is unity, which means that the output current mirrors the input current. Because the physical channel length that is achieved can vary substantially due to process variations, the accurate ratios usually result when devices of the same channel length are used, and the ratio of currents is set by the channel width.

For the n-MOS current mirror design shown in Fig. 2.4(b),

\[ \frac{I_{\text{OUT}}}{I_{\text{REF}}} = \frac{(W_4/L_4)}{(W_3/L_3)} \]  

(2.4)

For \((W_4/L_4)/(W_3/L_3) = 1\),

\[ I_{\text{OUT}} = I_{\text{REF}} \cong 50 \text{ µA} \]  

(2.5)

2.1.3 Active Resistors

There are two active resistors used in the design. Firstly, the reference current that is applied to the current mirror is obtained by means of an active resistor. The resistor here is obtained by simply connecting the gate of a MOSFET to its drain as shown in Fig 2.5(a). This connection forces the MOSFET to operate in saturation in accordance with the equation,

\[ I_{DS} = \{\beta (V_{GS} - V_{th})^2\}^{1/2} \]  

(2.6)

where \(\beta\) is the transconductance parameter, \(V_{th}\) is the threshold voltage and \(V_{GS}\) is the gate-source voltage. Since the gate is connected to the drain, current \(I_{DS}\) is now controlled
directly by $V_{DS}$ and therefore the channel transconductance becomes the channel conductance. The small signal resistance is given by

$$r_{out} = \frac{r_{ds}}{1 + g_m r_{ds}} \cong \frac{1}{g_m} \quad (2.7)$$

where $g_m$ is the transconductance of the MOS transistor. It is described by the following equation.

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} \bigg|_{V_{DS,cons tan t}} = \sqrt{2 \beta I_D} \quad (2.8)$$

It is to be noted that the trans-conductance of a MOS increases as the square root of the drain current. Hence, MOS amplifiers need several stages to achieve large gains.

The second active resistor shown in Fig 2.5(b) has been used to realize the nulling resistance to reduce the effects of the right hand plane zero in the transfer function. The gate of this transistor $M_{11}$ is biased at $V_{DD}$. Its small signal output resistance is obtained from Eq (2.7).

The small signal gain of the amplifier stage of Fig. 2.3 is described as follows [39],

$$A_1 = g_m (r_{o2} \ || \ r_{o4}) = \frac{2 \sqrt{\beta}}{\lambda_2 + \lambda_4} \sqrt{I_{SS}} = \frac{2}{\lambda_2 + \lambda_4 (V_{GS} - |V_{th,p}|)} \quad (2.9)$$

where $I_{SS}$ is the differential amplifier bias current and $|V_{th,p}|$ is the threshold voltage of the p-MOS transistors forming the differential pair. The differential pair needs to be biased by a constant current source, which is provided by the 100 µA current source. The same current is supplied to the two stages of the operational amplifier by the p-channel current mirrors $M_8, M_7, M_5$ which provide the bias current for the two stages. In the differential amplifier stage, differential amplification is accomplished and differential to single-ended
Figure 2.5: Active resistors: (a) gate connected to drain and (b) gate connected to $V_{DD}$. 

$V_{BIAS} = V_{DD}$
conversion is done. Thus, the output is taken only from one of the drains of the transistors. The n-channel devices M₃ and M₄ which are the load for the p-channel devices, also aid in the single-ended conversions. The second stage provides the additional gain. It is once again biased by a current source, which is also used to maximize the gain of the second stage. To get a high gain with reasonable high output resistance, the minimum channel length used is 3.2 µm and the maximum width of the transistor used is 235.6 µm. Transistor M₆ is critical to the frequency response, is biased at I_{D₆} = 200 µA and has \( \frac{W}{L}_6 = \frac{W}{L}_{\text{max}} \approx 22 \). The second stage is biased at \( -I_{D₇} \approx 200 \) µA to avoid input offset voltage. Transistors M₃ and M₄ are dimensioned according to [40],

\[
\frac{(W/L)_6}{2 \times (W/L)_{3,4}} = \frac{I_{D₇}}{I_{D₅}} = \frac{200 \mu A}{100 \mu A} = 2 \Rightarrow \left( \frac{W}{L} \right)_{3,4} = \frac{1}{4} \left( \frac{W}{L} \right)₆ \approx 5.5 \tag{2.10}
\]

Choose the smallest device length that will keep the channel modulation parameter constant and give good matching for current mirrors. The channel length is chosen to be \( L = 3.2 \) µm. Therefore, \( W = 17.6 \) µm for the transistors M₃ and M₄. To obtain the bias current of 50 µA, a MOS transistor is used with appropriate value of width (which is the MOSFET simulating resistors). Large W/L ratios for the transistors in the operational amplifier are obtained by using the following technique. Multiple numbers \( (n) \) of transistors are connected in such a way that the effective W/L ratio is \( n \) times the W/L ratio of each transistor. In present design, \( n=2 \) for transistors M₃ and M₄, and \( n=8 \) for transistor M₆. The technique reduces the required area, in comparison to a device laid out in a straight forward manner. The benefit of this technique is reduced junction capacitance, and is well characterized [40]. The simplicity, modularity and predictability of the device overcome the penalty of associated area.
The physical layout of the amplifier was made using the L-EDIT 8.3 and the ‘spice’ netlist extracted including parasitic capacitances. The layout of the amplifier is shown in the Fig 2.6. The value of the compensating capacitor, \( C_C \) used in the layout is 2 pF, whose area (46.4 x 52.8 \( \mu \text{m}^2 \)) has been designed using the average value of area capacitance (\( C' = 596 \text{ aF/}\mu\text{m}^2 \)) between the poly and poly2 layer provided by MOSIS [43]. Figure 2.7 shows the simulated transfer characteristics using MOS level-3 model parameters [43], obtained from DC sweep analysis. The maximum input range is \( \pm 100 \) mV. Figure 2.8 shows the transient analysis for a sinusoidal input with peak-to-peak amplitude of 200 mV applied to the inverting terminal of the operational amplifier at a frequency of 500 kHz. An inverted waveform is obtained at the output of the op-amp with peak-to-peak amplitude of 4.6 V, giving a voltage gain of 23 at 500 kHz. Figure 2.9 shows the frequency response characteristics. The 3 dB bandwidth of the amplifier obtained is approximately 1.1 kHz and the 3 dB gain is 78 dB. The output offset voltage calculated from the transfer characteristics is 20.6 mV. With an open-loop gain of 81 dB, the input offset voltage is approximately 1.8 \( \mu \text{V} \). Figure 2.10(a) shows the amplitude versus frequency behavior. Figure 2.10(b) shows the phase versus frequency characteristics. The phase noise margin calculated at 0 dB is 77\(^\circ\). The slew rate of the operational amplifier is 46 V/\( \mu \text{s} \) as shown in Fig 2.11.
Figure 2.6: Layout of an operational amplifier design of the circuit of Fig 2.3.
Figure 2.7: Post layout transfer characteristics of the circuit of Fig 2.3.
Figure 2.8: Post layout simulated response of the CMOS amplifier circuit of Fig 2.6.
Figure 2.9: Post layout (Fig 2.6) simulated frequency response characteristics of the amplifier circuit of Fig 2.3. Note: The open loop gain is 81dB and the 3dB bandwidth is 1.1 kHz.
Figure 2.10: Post layout (Fig 2.6) simulated (a) amplitude and (b) phase versus frequency response characteristics. Note: The phase margin is 77°.
Figure 2.11: Post layout (Fig 2.6) simulated slew rate characteristics of the amplifier circuit of Fig 2.3.
Figure 2.12: Effect of pole-splitting capacitor on the gain and phase of an op-amp.
2.2 Frequency Analysis of the Two-Stage Op-amp

An important part of an amplifier design is to ensure that the gain of the amplifier is less than unity at the frequency where phase shift around the loop is zero. To achieve this, one of the simplest ways is to give the op-amp a dominant pole. Figure 2.12 shows a typical variation of the gain and phase versus frequency which exhibits the gain roll-off after the first dominant pole $p_1$. After the second pole $p_2$, the amplifier becomes unstable or oscillatory since gain becomes greater than unity. A pole-splitting capacitor is used to push $p_1$ to the left and $p_2$ to the right (Fig. 2.12(b)). Figure 2.13(b) shows the two-port network equivalent small signal model of the circuit of Fig. 2.13(a). $V_{\text{id}}$ is the differential mode input voltage, $G_{m1}$ is the gain of differential stage equal to $g_{m1}$ and $g_{m2}$, and $G_{m2}$ is the gain of the second stage equal to $g_{m6}$. $R_2$ is the output resistance of second stage equal to $r_{o6} \parallel r_{o7}$. $R_Z$ is the zero nullifying resistance, $C_C$ is the compensation capacitance, $C_2$ is the load capacitance and $R_1$ is the output resistance of first stage equal to $r_{o2} \parallel r_{o4}$. The mid-frequency gain of the op-amp circuit of Fig. 2.13(a) is given by,

$$a_f = \frac{g_{m1}g_{m6}}{(g_{ds5} + g_{ds4})(g_{ds5} + g_{ds6})}$$

(2.11)

where

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \bigg|_{i_D} \approx \sqrt{(2\mu_0 C_{ox} W / L) I_D}$$

(2.12)

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \bigg|_{i_D} \approx I_D \lambda$$

(2.13)

in which $\mu_0$ is the channel surface mobility, $C_{ox}$ is the capacitance per unit area of the gate oxide, $W$ and $L$ are the effective channel length and width respectively, $\lambda$ is the channel length modulation parameter of the transistor. $I_D$ represents the quiescent current and is provided by M8, M10 and M5 transistors.
Figure 2.13(a): A two-stage CMOS op-amp showing the feedback components.

Figure 2.13(b): Two-port network equivalent small signal model of a two-stage op-amp configuration of Fig. 2.13(a) with an equivalent zero nulling resistance ($R_Z$).
Due to the low transconductance of MOS transistors, the transistor $M_{11}$ shown in Fig. 2.13(a) is needed to provide a nullifying resistance to reduce the effects of the right hand plane zero in the transfer function, and in fact, can be used to improve the frequency response of the amplifier. The small signal equivalent circuit in Fig. 2.13(b) has two poles and a zero, whose magnitudes are [see Ref. 42, pp.644-650],

\[ \omega_{p1} = \frac{1}{G_{m2} R_2 C_C R_1} \]  
\[ \omega_{p2} = \frac{G_{m2} C_C}{C_1 C_2 + C_C (C_1 + C_2)} \approx \frac{G_{m2}}{C_1 + C_2} \]  

and,

\[ \omega_z = \frac{1}{(1/G_{m2} - R_z) C_C} \]  

By choosing $R_z$ to be equal to the inverse of the transconductance of the second stage, the frequency response of the amplifier can be further improved.

2.3 Stability and Feedback Analysis

Operational amplifiers can have either a closed-loop operation or an open-loop operation determined by whether or not feedback is used. In the closed-loop configuration, the output signal is applied back to one of the input terminals. Negative feedback is widely used to stabilize the gain of the amplifier against parameter changes in the active devices due to supply voltage variation, temperature changes, or device aging. It is also used to modify the input and output impedances of the circuit, reduce signal waveform distortion, and increase the bandwidth of circuits. A circuit configuration for voltage feedback applications using amplifiers is shown in Fig. 2.14.
Figure 2.14: Feedback circuit configuration.
The transfer function of the feedback circuit configuration of Fig. 2.14 is given by [26],

\[ A_f(s) = \frac{V_o}{V_i} = \frac{a_v(s)}{1 + a_v(s)f(s)} \]  \hspace{1cm} (2.17)

where \( a_v(s) \) is the approximated single pole transfer function of the compensated operational amplifier and is given by

\[ a_v(s) = \frac{a_v}{1 - s/p_1} \approx \frac{-a_v p_1}{s}, \text{ assuming } s/p_1 >> 1 \text{ for high frequencies} \]  \hspace{1cm} (2.18)

where \( a_v \) is the low-frequency gain of the amplifier and \( p_1 \) is the amplifier pole in radians per second. The unity-gain frequency of the op-amp is the frequency at which \(|a_v(j\omega)|=1\) and given by,

\[ |a_v(j\omega)| = 1 \approx \frac{a_v}{\omega T / p_1} \]  \hspace{1cm} (2.19)

\[ \omega T \approx a_v p_1 \]  \hspace{1cm} (2.20)

For the op-amp in feedback to be stable, the denominator of the closed loop transfer function must not equal zero i.e.

\[ |a_v(j\omega)f(j\omega)| < 1 \text{ where } \angle a_v(j\omega)f(j\omega) = 0 \text{ degrees} \]  \hspace{1cm} (2.21)

This condition is known as the Barkhausen criterion [42]. The Barkhausen criterion states that at the frequency of oscillation (\(\omega_{OSC}\)), the signal must traverse the loop with no attenuation and no phase shift. For positive feedback, the phase shift must be zero, but for negative feedback, the phase shift must be 180° to cancel the feedback sign and produce a total phase shift of zero.
2.4 Testing Faults Using Oscillation Testing Methodology

During the test mode, the CUT is separated from the original circuit using a design-for-test (DfT) structure based on OTM [26]. Figure 2.15 shows the DfT structure which uses simple test switches to isolate the amplifier from its normal external input and output pins and connect it to a feedback system which may have active or passive components. When the test mode (TM) signal is active, the negative, positive and output pins are separated from the original circuit using switches S₁, S₂ and S₃ respectively and will be available for the test structure. This feedback makes the CUT an oscillator.

Converting the CUT into an oscillator requires a mechanism to force displacement of at least a pair of poles. Since the compensated op-amp with an approximated single pole transfer function given by Eq. (2.18) has a stable frequency response, a new pole is introduced into the simplified first-order system using an RC-delay circuit in the feedback path during the test mode to create oscillations. Figure 2.16(a) shows a second order oscillator and Fig 2.16(b) shows the CMOS amplifier used in the inverting mode, which is converted into an oscillator using the RC feedback network [26]. The loop’s overall gain and phase cause oscillation. The values of the feedback components can be adjusted to achieve self-sustained oscillations. The oscillation frequency \( f_{\text{osc}} \) can be expressed either as function of the CUT components or as function of its important parameters.

The feedback function, \( f(s) \) for the system shown is the net negative feedback and is given by [26],

\[
f(s) = G - \left( \frac{-s}{p_2} \right) \left( \frac{1 - s/p_2}{1 - s/p_2} \right)
\]

\[ \quad \quad \quad (2.22) \]
Figure 2.15: Schematic representation of a testable op-amp [26].
Figure 2.16: A second order oscillator. (a) Block diagram (b) CMOS oscillator
where $G$ corresponds to a negative feedback and the second term corresponds to a positive feedback. $G$ is a constant given by

$$G = \frac{R_2}{R_2 + R_1} \quad \text{and} \quad p_2 = -\frac{V}{RC} \quad (2.23)$$

Substituting $f(s)$ and $G$ from Eqs. (2.22) and (2.23) in Eq. (2.17) and using Eq. (2.18), we obtain,

$$A_v(s) = \frac{a_v}{1 + \left( \frac{a_v}{p_1} \right) \left( \frac{s}{p_1} \right) \left( \frac{s}{p_2} \right) \left( \frac{s}{p_2} \right)}$$

or

$$A_v(s) = \frac{a_v p_1 (p_2 - s)}{s^2 + \{(1-G)a_v p_1 - (p_1 + p_2)\} + (Ga_v p_1 p_2 + p_1 p_2)} \quad (2.24)$$

The poles for the new transfer function described by Eq. (2.24) are obtained by equating its denominator to zero. In order for the network to oscillate with constant amplitude, the poles must be placed on the imaginary ($j\omega$) axis. In practice, the poles must be placed on the right half of the s-plane. For the poles to be placed in the right half of the s-plane,

$$G \geq 1 - \frac{(p_1 + p_2)}{a_v p_1} \quad (2.25)$$

With $G = 1 - \frac{(p_1 + p_2)}{a_v p_1}$, i.e., for the imaginary axis of s-plane, the natural frequency of oscillation of the new system can be described by,
\[ \omega_{osc}^2 = G a_v p_1 p_2 + p_1 p_2 = a_v p_1 p_2 - p_2^2 \]  

(2.26)

Hence the poles of the op-amp oscillator shown in Fig. 2.17 can be derived as

\[ p'_{osc} = \omega_{osc} = \pm \sqrt{a_v p_1 p_2 - p_2^2} \]  

(2.27)

Placing the poles on the imaginary axis converts the system into an oscillator which produces sinusoidal oscillations at the natural frequency as shown in Fig 2.18. From Eq. (2.26), the maximum frequency and the condition for maximum achievable oscillation frequency can be derived as follows,

\[ \omega_{osc}^2 = G a_v p_1 p_2 + p_1 p_2 \]  

(2.28)

\[ \omega_{osc} = \left( G a_v p_1 p_2 + p_1 p_2 \right)^{1/2} \]  

(2.29)

Differentiating Eq. (2.29) with respect to \( p_2 \),

\[ \frac{\partial \omega_{osc}}{\partial p_2} = \frac{1}{2} \left( G a_v p_1 + p_1 \right) \]

Substituting \( G \) from Eq. (2.25),

\[ \frac{\partial \omega_{osc}}{\partial p_2} = \frac{1}{2} \left( a_v p_1 - \frac{(p_1 + p_2)}{a_v p_1} \right) \]

\[ = \frac{1}{2} \left( a_v p_1 - (p_1 + p_2) \right) + p_1 \]  

(2.30)

\[ \frac{\partial \omega_{osc}}{\partial p_2} = \frac{1}{2} \left( a_v p_1 - p_2 \right) = 0 \]  

(2.31)

or \( p_2 = \frac{a_v p_1}{2} \)  

(2.32)
Figure 2.17: Pole locations for the amplifier and oscillator configurations in $s$-domain. Note: $\omega$ is the frequency in radians and $\sigma$ is a real number in radians.
2.5 Fault Sensitivity and Tolerance Band of Oscillation Frequency Using Monte-Carlo Simulation

The nominal frequency range of the CUT is determined using a Monte-Carlo analysis taking into account the tolerance of significant technology and design parameters. The oscillation frequency of the oscillatory operational amplifier is measured and is compared with the nominal oscillation frequency of the fault-free circuit. If the oscillation frequency lies close to the nominal frequency range, the amplifier is accepted to be fault-free. The observability of a fault in a component (or a parameter) can be defined as the sensitivity of the oscillation frequency with respect to the variations of the component (or the parameter). In order to increase the observability of a defect in a component (or the fault in a parameter), the oscillator architecture is chosen such that the amplifier’s frequency varying components contribution to the oscillation frequency is maximized.

The oscillator circuit of Fig. 2.16 (b) has been simulated in SPICE. The output signal is a sine wave as shown in Figure 2.18. FFT analysis has been performed to determine the natural oscillation frequency ($f_{\text{NAT}}$) and is shown in Fig. 2.19. It was observed to be 875 kHz. Process variation effects on one of the most important electrical characteristics, namely the threshold voltage has been included in the tolerance band for oscillation frequency with a tolerance of 5% for threshold voltage. With 5% tolerances for the important frequency components (R, C, R1, R2) of the circuit of Fig. 2.16 (b), the tolerance band of oscillation frequency was observed to be [-3.7%, +4.1%] obtained from Monte-Carlo simulations as shown in Fig. 2.20, where $f_{\text{MAX}}$ is 910 kHz and $f_{\text{MIN}}$ is 842 kHz, which are the maximum and minimum acceptable limits of oscillation frequency.
Figure 2.18: Simulated natural oscillation frequency of the CUT oscillator.
Figure 2.19: Simulated FFT analysis for obtaining the natural oscillation frequency.
Figure 2.20: Monte-Carlo analysis for parametric tolerances of important CUT parameters. 
Note: the tolerance band is calculated as follows: $[\text{Min}, \text{Max}] = [(f_{\text{MIN}} - f_{\text{NAT}})/f_{\text{NAT}}, (f_{\text{MAX}} - f_{\text{NAT}})/f_{\text{NAT}}]$. 
CHAPTER 3

IDDQ TESTING USING BUILT-IN CURRENT SENSOR †

IDDQ testing has been used to complement the high fault coverage achieved by oscillation testing and to provide fault confirmation. This chapter focuses on IDDQ testing using built-in current sensors (BICS). It also describes the design and implementation of the BICS used to detect faults in a two-stage CMOS operational amplifier, the fault simulation and detection methodologies. Important physical faults commonly seen in the design of CMOS circuits have also been discussed.

3.1 Quiescent Current (IDDQ) Testing in CMOS Circuits

IDDQ stands for quiescent I_DD, or quiescent power-supply current. IDDQ testing of CMOS ICs is shown very efficient for improving test quality. The test methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects such as gate oxide shorts, floating gates and bridging faults, which are not very well modeled by the classic fault models, or undetectable by conventional logic tests [44]. It has been recognized as the single most sensitive test method to detect CMOS IC defects [45]. The major advantage of current-based testing is that it does not require propagation of a fault effect to be observed at the output; it requires only exercising the fault model and then measuring the current from the power supply. The fault effect observance is the measurement of current, and the detection criteria are the current flow value exceeding some threshold limit [46]. The current passing through the V_DD or GND terminals is monitored during the application of an input stimulus. In the quiescent state the circuit draws a very low current (micro-amp

† Part of the work is reported in Ref [33].
levels); for certain input states this current may raise to an abnormal level due to the presence of defects.

Current fluctuations can be monitored using on-chip or off-chip current sensors. On-chip or built-in current sensors (BICS) have speed and resolution enhancements over off-chip current sensors mainly because the large transient currents in the output drivers are by-passed and a few parasitics are encountered. On-chip current testing is both time-efficient and sensitive. Moreover, on-chip current tests can also be used as an on-line testing tool, and is important when components are to be used in high reliability systems. For high speed and high sensitivity, unaffected by large pad currents, a fast built-in current testing circuit is desired [47]. In the present work, a simple design of a built-in current sensor is presented to detect bridging faults in a two-stage CMOS amplifier circuit. A simple method for the fault injection has been used to simulate physical defects present in a chip.

Figure 3.1 shows the block diagram of the I_{DDQ} testing with BICS. Essentially, I_{DDQ} testing technique adds a BIC sensor in series with V_{DD} or GND lines of the circuit under test. A series of input stimuli is applied to the device under test while monitoring the current of the power supply (V_{DD}) or ground (GND) terminals in the quiescent state conditions after the inputs have changed and prior to the next input change [48]. Typically, subthreshold current in the transistors, which are ‘off” in a CMOS static circuit should be negligibly small. However, in some cases, due to charge presence in a gate oxide or latch-up, the sub-threshold current may be large enough to become an essential component of I_{DDQ}. The BICS can be designed to detect this current also.
Figure 3.1: Block diagram of I$_{DDQ}$ testing.
3.2 Physical Defects in CMOS Integrated Circuits

In CMOS technology, the most commonly observed physical failures are bridges, opens, stuck-at-faults and gate oxide shorts (GOS). These defects create indeterminate logic levels at the defect site [44]. Very large-scale integrated circuits processing defects cause shorts or break in one or more of the different conductive levels of the device [49]. We briefly discuss these physical defects that cause an increase in the quiescent current.

3.2.1 Bridging Faults

Bridges can be defined as undesired electrical connections between two or more lines in an integrated circuit, resulting from extra conducting material or missing insulating material. When $I_{DDQ}$ measurements are used, a bridge is detected if the two nets, which comprise it, have opposite logic values in the fault-free circuit [50] and are connected by a bridge due to the introduction of the fault in the circuit. Bridging faults can appear either at the logical output of a gate or at the transistor nodes internal to a gate. Bridge between the outputs of independent logic gates or an inter-gate bridge can also occur. Bridging fault could be between the following nodes 1) drain and source, 2) drain and gate, 3) source and gate, and 4) bulk and gate. Figure 3.2 shows an example of possible drain to source and gate to source bridging faults in an inverter chain in the form of low resistance bridges $R_1$ and $R_2$, respectively. Resistance bridge, $R_3$ is an example of inter-gate bridge. Figure 3.3 shows examples of gate to source and gate to drain bridges in an NAND gate circuit. Bridging defect cannot be modeled by the stuck-at model approach, since a bridge often does not behave as a permanent stuck node to a logic value [50]. $I_{DDQ}$ testing using BICS is an effective method of detecting bridging shorts.
Figure 3.2: Drain-source, gate-source and inter-gate bridging faults in an inverter chain.
Figure 3.3: Bridging defects.
3.2.2 Open Faults

Logic gate inputs that are unconnected or floating inputs are usually in high impedance or floating node-state and cause elevated $I_{DDQ}$ [47]. Figure 3.4 shows a 2-input NAND with open circuit defects. Node $V_N$ is in the floating node-state caused due to an open interconnect. For an open defect, a floating gate may assume a voltage because of parasitic capacitances and cause the transistor to be partially conducting [50]. Hence, a single floating gate may not cause a logical malfunction. It may cause only additional circuit delay and abnormal bus current [47]. In Fig. 3.4, when the node voltage ($V_N$), reaches a steady state value, then the output voltage correspondingly exhibits a logically stuck behavior and this output value can be weak or strong logic voltage. Open faults, however, may decrease or may cause only a small rise in $I_{DDQ}$ current, which the off-chip current sensor may not detect because of its low-resolution [44]. It can be detected using BIC sensors. An open source or open drain terminal in a transistor may also cause additional power-bus current for certain input states. Another open fault shown in Fig. 3.4 is an open FET ($M_2$). In the scope of this work, only bridging faults have been dealt for $I_{DDQ}$ testability. $I_{DDQ}$ testing cannot detect some of the opens which result in decrease of the quiescent current. Oscillation testing has been used to test this type of faults.
Figure 3.4: Floating input and open FET – open circuit defects.
3.4 Definition of $I_{DDQ}$ of a Faulty Circuit

$I_{DDQ}$ is defined as the level of power supply current in a CMOS circuit when all the nodes are in a quiescent state. Static CMOS circuits use very little power and at standby or quiescent state, it draws practically negligible leakage current [48]. In steady state, there should not be a current path between $V_{DD}$ and GND path. Ideally, in a static CMOS circuit, quiescent current should be zero except for associated p-n junction leakage currents. Any abnormal elevation of current should indicate presence of defects. To assure low stand-by power consumption, many CMOS integrated circuit manufacturers include $I_{DDQ}$ testing with other traditional DC parametric tests [49].

3.4.1 Description of $I_{DDQ}$ Testing for a Faulty Inverter

Figure 3.5 shows how an $I_{DDQ}$ test can identify defects. The current in static CMOS is not constant during transient [51]. When an output transition occurs, a peak of $I_{DDQ}$ current is observed. This peak is due to charging and discharging of the load capacitance at the output circuit and corresponds to the short circuit. When the transition is completed, the circuit is in the quiescent state. $I_{DDQ}$ is very sensitive to physical faults in the circuit.

Let us evaluate current testing in CMOS circuits in the presence of bridging faults. Two nodes connected by a bridge must be driven to opposite logic levels under fault-free conditions for bridging fault to occur. In Fig.3.5, a typical bridge is one between the node $V_{O1}$ and $V_{DD}$. To detect this defect, input pattern must drive the node $V_{O1}$ to the logic low value (‘0’), as this node is assumed to be bridged with the power rail.
Figure 3.5: Bridging fault causing $I_{DDQ}$ drop and a path to the ground.
Thus, a path from power to ground appears allowing the existence of an abnormal high \( I_{DDQ} \) current. \( I_{DDQ} \) value is directly dependent on the resistance offered by the conducting path and hence on the size of the transistors in the conducting path. The presence of the physical fault causing the high abnormal current can be effectively detected by \( I_{DDQ} \) testing using BICS. A set of realistic bridges have been modeled between adjacent metal lines in a two-stage CMOS amplifier circuit at three different (conducting levels), to examine the effect on the value of \( I_{DDQ} \) and detect the presence of the fault using the BICS.

### 3.5 Design Considerations of BICS

A simple design of a BIC sensor built into the two-stage operational amplifier is presented using the current mode design. It determines whether the circuit quiescent current is below or above a threshold level. Previously proposed schemes and the characteristics required for a good BICS are discussed briefly in this section.

#### 3.5.1 Previously Proposed Schemes

Different BICS schemes have been proposed for detection of the abnormal \( I_{DDQ} \) current and the physical faults commonly observed. While most BICS designs concentrate on mere detection of the fault, some can detect the location of the fault as well [52]. The entire design is divided into \( n \) sub-blocks (SB) where \( n \) equals the number of outputs. The divided SB’s are checked individually through their corresponding output and a faulty area is easily detected by observing the outputs. The performance impact of a BICS on a circuit under test (CUT) is the key issue to be considered when designing BICS. Insertion of the BIC sensor between CUT and GND involves series voltages, and
these voltages could degrade the performance of the CUT [51,53]. A large number of earlier BICS are based on voltage amplifiers such as differential amplifiers or sense amplifiers. The stability of the BICS is limited in this case since the quiescent point (Q-point) of an amplifier may not be stable and can vary with the change of dc supply voltage, $V_{DD}$. The detection time and hardware overhead is increased due to the extra hardware required to stabilize the Q-point.

To overcome problems of slow detecting time, resolution, instability of the BICS and large impact on the CUT performance, the current-mode circuit design approach has been adopted using a single power supply. In this work, simple design of a BICS employing current mirrors and current differential amplifier has been used. It has minimum area overhead in the chip and no impact on overall performance.

Characteristics required for a good BIC sensor are [54]:

1. Detection of abnormal static and dynamic characteristics of the CUT.
2. Minimal disturbance of the static and dynamic characteristics of the CUT.
3. The design should be simple and compact to minimize the additional area necessary to build it.
4. The $I_{DDQ}$ test should have good resolution and speed.

### 3.6 Design and Implementation of the BICS

Figure 3.6 shows the CMOS circuit diagram of the built-in current sensor [33] with the CUT. It consists of a current differential amplifier ($M_2$, $M_3$) and two current mirror pairs ($M_1$, $M_2$ and $M_3$, $M_4$). The n-MOS current mirror ($M_1$, $M_2$) is used to mirror the current from the constant current source which is used as the reference current $I_{REF}$ for the BICS. The current mirror ($M_3$, $M_4$) is used to mirror the difference current...
Figure 3.6: CMOS built-in current sensor circuit with the CUT [33].
(I_{\text{DEF}}-I_{\text{REF}}) to the current inverter, which acts as a current comparator. The differential pair (M_2, M_3) calculates the difference current between the reference current I_{\text{REF}} and the defective current I_{\text{DEF}} from the CUT. The W/L size of the n-MOS current mirror (M_1, M_2) is set to 36/1.6. The size of M_3 is set to 100/1.6 and M_4 is set to 400/1.6. Therefore I_{D3} = I_{\text{DEF}}-I_{\text{REF}}. The constant reference current is set to approximately the same value as the quiescent state current when the CUT is fault free. In the present design, the reference current, I_{\text{REF}} is set to 450 µA. The output inverter buffer has an aspect ratio ((W/L)_P / (W/L)_N) of 2/1 to counter capacitive parasitics at the output node and detect the presence of the physical fault through the PASS/FAIL flag at the output.

The BICS is inserted in series with GND or V_{SS} line of the circuit under test. The proposed BICS works in two modes: the normal mode and the test mode. The mode of operation is decided by the V_{ENABLE} signal applied to the gate of transistor M_0. The W/L size of the enable transistor M_0 is 92/1.6. This enables the two-stage CMOS amplifier, which is the CUT to operate as fault-free in the normal mode of operation. In the normal mode (V_{ENABLE} = ‘1’), the BICS is isolated from the CUT. In the test mode (V_{ENABLE} = ‘0’), the quiescent current from the CUT is diverted into the BICS and compared with reference current to detect the presence of the fault.

3.6.1 BICS in Normal Mode

During the normal operation, the signal ‘V_{ENABLE}’ is at logic ‘1’ and all the I_{DD} current flows to ground through M_0 (enable transistor). When switching occurs, M_0 is turned on. Therefore, the n-MOS current mirrors have no effect on dynamic current. It follows that the BIC sensor’s output is not affected by the dynamic current. Thus, in the normal mode, the BICS is isolated from the two-stage compensated CMOS amplifier.
(CUT). Since in normal mode the current coming from the CUT is same as the reference current the difference current $I_{\text{DEF}} - I_{\text{REF}}$ becomes negligible and the output of the BICS is at logic ‘0’. In the normal mode, it cannot detect the presence of any physical fault in the CUT. Since the BICS is inserted in series with GND line of the CUT, it causes a voltage drop and large capacitance between the CUT and the substrate. These effects cause performance degradation and ground level shift. To reduce these extra undesirable effects, an extra pin EXT is added to the proposed BICS. Pin EXT is connected to the drain of transistor $M_0$. In the test mode, it is left floating. In the normal mode, EXT gets connected to logic ‘0’. In the normal mode, since the EXT pin is grounded by passing the BICS, the disturbance of the ground level shift during normal operation of the circuit never happens. Therefore, there is no impact on the performance of the amplifier under test, while the BICS is in normal mode.

3.6.2 BICS in Test Mode

During the test mode, the ‘$V_{\text{ENABLE}}$’ signal is at logic ‘0’. The $I_{\text{DDQ}}$ current from the CUT is diverted by the BICS and the n-MOS current mirror pair replicates the reference current to the current differential amplifier which assigned a value nearly same as the fault-free current. This mirrored reference current is compared with defective current $I_{\text{DEF}}$ current coming from the CUT. The output of the current comparator, which is in the form of PASS/FAIL, will detect the presence of the fault.

The difference current is converted to a voltage by mirroring it and getting the drop of $V_{\text{DS}}$ across the transistor $M_4$. In the test mode, the difference current is large which turns-on $M_4$ heavily and forces its output node pulled-down to logic ‘0’ and is
detected as PASS/FAIL output ‘1’, indicating presence of defects in CUT. In the testing mode, EXT pin is floating. The ‘VENABLE’ signal is connected to GND and M0 is off.

### 3.7 BICS Layout

Figure 3.7 shows the layout of the BICS of the circuit shown in the Fig. 3.6. The test signal $V_{\text{ENABLE}}$ is applied to the gate of an n-MOS transistor, $M_0$ (W/L = 92/1.6), which decides the mode of operation. When the test signal is ‘0’, the BICS is in the test mode. When the test signal is at logic ‘1’, the BICS is isolated from the CUT and its output is at logic ‘0’. In the normal mode the operation of the CUT can be made independent of the BICS by connecting the EXT node to $V_{\text{SS}}$. Several simulations have been performed to test the functionality of the BICS. These are presented in the next chapter.

### 3.8 Fault Models, Simulation and Detection

For analog CMOS circuits, faults can be classified into either catastrophic or parametric [55, 56]. Research results claim that 80-90% of observed analog faults are catastrophic faults which consist of shorts or opens in diodes, transistors, resistors and capacitors [57]. Moreover, the yield losses in CMOS process are primarily due to catastrophic faults [56]. It is known that when 100% of catastrophic faults are detected by a test method, the majority of parametric faults depending on the deviation value of the parametric faults can also be detected [58]. As parametric faults are concerned, a tolerance band of ±5% is used. This implies that if the values of parameters to be observed in the testing process appropriate to particular faults are within the tolerance band, these faults will be considered as tolerable and cannot be detected.
Figure 3.7: Layout of a built-in current sensor circuit.
The primary reason for a fault is a defect in the integrated circuit. A manufacturing defect causes unacceptable discrepancy between its expected performance at circuit design and actual IC performance after physical realization [47]. A defect may be any spot of missing or extra material that may occur in any integrated circuit layer.

Two nodes are connected if there is at least one path of conducting transistors between them. If the two nodes are at opposite potentials under fault-free conditions, a conducting path between them will increase the \( I_{DDQ} \) current due to fault in the circuit. After transient switching, each node in a digital circuit is one of the following four states-

1. \( V_{DD} \) state: This state occurs when the node is connected to \( V_{DD} \).
2. GND state: This state occurs when the node is connected to GND.
3. Z state: The high-impedance state occurs when the node is neither \( V_{DD} \) nor GND connected.
4. X state: This state occurs when the node is both \( V_{DD} \)-connected and GND-connected [47].

The ‘X’ state should never occur in fault-free CMOS integrated circuits. Many defects cause an X state to occur in CMOS integrated circuits. Thus, we can view testing as a way to detect the X state, which causes detectable abnormal steady state current.

Bridging faults have been induced in the amplifier at various conducting levels using a fault-injection transistor (FIT), discussed further ahead, which cause abnormal elevation of the steady state current. The faults are injected one at a time.

3.8.1 Fault Injection Transistor

Bridging faults have been placed in the CMOS amplifier design using fault injection n-MOS transistors. Activating the fault injection transistor activates the fault.
The use of a fault injection transistor for the fault simulation prevents permanent damage to the operational amplifier by introduction of a physical metal short. This enables the operation of the operational amplifier without any performance degradation in the normal mode. Figure 3.8 (a) shows the fault injection transistor. To create an internal bridging fault, the fault injection transistor ($M_E$) is connected to opposite potentials. When the gate of fault injection transistor is connected to $V_{DD}$, a low resistance path is created between its drain and source nodes and a path from $V_{DD}$ to GND is formed. In the Fig. 3.8(b), an internal bridging fault is created in the CMOS inverter between the drain and source nodes using the fault injection transistor. Logic ‘0’ is applied at the input of the inverter. Therefore, the output of the inverter is at logic ‘1’ or $V_{DD}$. When the logic ‘1’ is applied to the gate ($V_E$) of the n-MOS fault injection transistor ($M_E$), it turns on. This causes a low resistance path between the output of the inverter and the $V_{SS}$. This gives rise to an excessive $I_{DDQ}$ current as a path from $V_{DD}$ to GND is created, which can be detected by the BICS. In the Fig. 3.9, internal bridging faults created in the CMOS amplifier between the drain and source nodes using the fault injection transistors are shown. In this work, seven bridging faults viz., $M_{10}$ drain-source short (defect 1-$M_{10}$DSS), $M_{5}$ gate-drain short (defect 2-$M_{5}$GDS), $M_{5}$ drain-source short (defect 3-$M_{5}$DSS), $M_{11}$ drain-source short (defect 4-$M_{11}$DSS), $M_{4}$ gate-drain short (defect 5-CCS), compensation capacitor short (defect 6-$M_{6}$GDS), $M_{7}$ gate-drain short (defect 7-$M_{7}$GDS) and $M_{11}$ gate $V_{BIAS}$ connected to $V_{SS}$ (defect 8-$M_{11}$G-VSS) simulating an open fault, have been introduced in the amplifier. Here, defect 1 ($M_{10}$DSS) and defect 3 ($M_{5}$DSS) show an increase in quiescent current when the ERROR signals are applied hence are $I_{DDQ}$ testable. All other faults including defect 1, defect 3 and the open fault are tested using oscillation testing. The
Figure 3.8 (a): n-MOS Fault injection transistor (FIT) used in the layout.

Figure 3.8 (b): Fault injection transistor between drain and source nodes of a CMOS inverter.
results are presented in the next chapter.

In Figure 3.9, the area of the operational amplifier alone is $540 \times 186 \, \mu m^2$. The entire area of the CUT along with BICS is $540 \times 320 \, \mu m^2$. The BICS occupies only $200 \times 106 \, \mu m^2$ of the entire chip area. Seven bridging defects have been introduced using fault injection transistors. The n-MOS fault injection transistor ($M_E$) designed has a maximum aspect ratio ($W/L$) of 41.6/3.2 and the minimum $W/L$ ratio used is 6.4/6.4. The fault injection transistors are activated externally using ERROR signals $V_{E1}$ and $V_{E3}$, which are applied to the gate of the fault injection transistors in defect 1 and defect 3, respectively, forming shorts between the source and drain of the transistors $M_5$ and $M_{10}$ in the operational amplifier circuit shown in Fig. 3.10.
Figure 3.9: Layout of a two-stage CMOS amplifier with BICS showing the defects induced in the CUT using fault injection transistors.
Figure 3.10: Injected faults using FITs.

Note: X_{FIT}: n-MOS fault injection transistor. X_{FIT 1} and X_{FIT 3} are I_{DDQ} testable faults while X_{FIT 1-7} are oscillation testable faults.
CHAPTER 4
FAULT COVERAGE AND EXPERIMENTAL RESULTS FOR THE COMBINED TEST PROCEDURE

This chapter discusses the fault coverage achieved by the combined test approach based on the theoretical results obtained from post-layout PSPICE (Cadence Pspice A/D Simulator, V.10) simulations on combined $I_{DDQ}$ and oscillation testing of the two-stage CMOS amplifier, and the observed experimental results. SPICE level 3 MOS model parameters were used in simulation [42], which are summarized in Appendix A. The chip was designed using L-EDIT, V.8.3 in standard 1.5 $\mu$m n-well CMOS technology. The chip occupies an area of 540 $\mu$m $\times$ 320 $\mu$m. The CMOS amplifier design with the BICS was put in 2.25 mm $\times$ 2.25mm size, 40-pin pad frame for fabrication and testing. In the following sections, theoretical results (simulated from PSPICE) and experimentally measured values will be presented and discussed.

Figure 4.1(a) shows the complete circuit diagram of a two-stage compensated CMOS operational amplifier with seven fault injection transistors and Figure 4.1(b) shows its layout. $X_{FIT}$ denotes the fault injection transistor that is injected in the operational amplifier. Figure 4.2 shows the chip layout of the CMOS amplifier including BICS within a pad frame of 2.25 mm $\times$ 2.25 mm size. The area of the operational amplifier alone is 540 $\times$ 186 $\mu$m$^2$. The entire area of the CUT along with BICS is 540 $\times$ 320 $\mu$m$^2$. The BICS occupies only 200 $\times$ 106 $\mu$m$^2$ of the entire chip area.
Figure 4.1(a): Circuit diagram of a two-stage CMOS amplifier with BICS with seven fault injection transistors.
Figure 4.1(b): Layout of a two-stage CMOS amplifier with BICS with seven fault injection transistors.
Figure 4.2: CMOS chip layout of a two-stage CMOS amplifier including BICS within a padframe of 2.25mm × 2.25mm size.
4.1 Simulated Amplifier Functional Testing Results

Figure 4.3 shows the microphotograph of the fabricated chip with the CUT amplifier and the BICS for \textit{I}$_{DDQ}$ testing. Figure 4.4(b) shows the simulated output of the op-amp when the fault M7GDS is activated (Fig. 3.16). When the op-amp is given a sine wave of 100 mV p-p at 250 kHz, the output obtained is a sine wave of 4.5 mV p-p with a gain of 0.045. Output offset voltage is increased to -1.27V from 20.6 mV without faults (Fig. 2.7). Figure 4.5 shows the transfer function with the fault (M10DSS) activated with significant non-linearity introduced in the narrow transition region. Figure 4.6 shows the gain versus frequency response of op-amp with fault (M5DSS) activated. The amplifier 3 dB-gain with the fault activated is 20 dB as compared to 78 dB when the fault is deactivated. The 3 dB bandwidth is increased to 200 kHz from 1.1 kHz without fault (Fig. 2.16). Thus, the gain-bandwidth product decreases from 8.75 MHz without faults to 2 MHz when M5DSS is activated. In the oscillation test mode, it is to be noted that the frequency of oscillation of the CUT oscillator depends on the gain-bandwidth product of the amplifier. Thus, the output oscillation frequency exhibits a deviation from its tolerance band when the fault M5DSS is activated.

4.2 Simulated \textit{I}$_{DDQ}$ Testing Results

The testable faults which can be detected by \textit{I}$_{DDQ}$ testing, injected into the chip of Fig. 4.2, are defect 1 – M10DSS and defect 3 – M5DSS. Figure 4.7 shows the simulated BICS output when the FIT-1 is activated. FIT-1 is a defect injected between the source and drain of transistor M$_{10}$ (M10DSS) of the operational amplifier circuit (Fig. 3.16) also shown in the layout of Fig 4.1. In Fig. 4.7, when the \textit{V}_\text{ENABLE} signal is ‘high’, the BICS is
Figure 4.3: Microphotograph of the fabricated chip showing the CUT (CMOS amplifier) and the BICS for $I_{DDQ}$ testing.
Figure 4.4: (a) Normal and (b) faulty output of the amplifier for a sinusoidal input voltage of 100 mV p-p.

Offset Voltage = -1.27V
Figure 4.5: Normal and faulty transfer characteristics of the amplifier.
Figure 4.6: Voltage gain versus frequency characteristics of the amplifier without faults and with M5DSS fault.

Note: The gain-bandwidth product of the amplifier decreased from 8.75 MHz to 2 MHz. This would have an effect on the oscillation frequency when the amplifier is converted into an oscillator in the test mode.
by-passed and the defect is not detected. When the $V_{\text{ENABLE}}$ signal is ‘low’, the BICS is enabled and if the Error-signal is ‘high’, the BICS detects the faults and the output of the BICS is ‘high’. Figure 4.8 shows the simulated BICS output when the FIT-3 is activated (Fig.3.16). FIT-3 is a defect injected between the source and drain of transistor $M_5$ (M5DSS) of the amplifier circuit of Fig. 3.16. In Fig. 4.8, when the $V_{\text{ENABLE}}$ signal is ‘high’ the BICS is by-passed and the defect is not detected. When the $V_{\text{ENABLE}}$ signal is ‘low’ the BICS is enabled and if the Error-signal is ‘high’ the BICS detects the faults and the output of the BICS is ‘high’.

Figure 4.9 shows the simulated output of the BICS when FIT’s of M10DSS and M5DSS faults are activated. In Fig. 4.9, when the $V_{\text{ENABLE}}$ is ‘high’ the BICS is disabled and when it is low the BICS is enabled. When the BICS is enabled and if there is any Error Signal going ‘high’ the BICS detects the fault. Table 1 shows the faulty $I_{\text{DDQ}}$ values obtained for the above two faults injected in the chip. The designed BICS has a resolution of nearly of 100 µA. The normal quiescent current is observed to be nearly 380 µA while the defective current, which the BICS detects, is nearly 480 µA. The $M_{10}$ drain source short fault (M10DSS) provides a large current of 1.10 mA, while the $M_5$ drain source short (M5DSS) provides a current of 481.9 µA. Hence, the designed BICS is sensitive for a wide range of faulty current. Figure 4.10 shows the degradation in the voltage levels due to the presence of the BICS. It is observed to be in the order of 30 mV when the BICS is shorted, hence can be considered negligible compared to the supply voltage levels of ±2.5 V. Our BICS design uses only nine transistors. The BICS requires neither an external voltage source nor a current source. Further more, the BICS does not require clocks.
Figure 4.7: Simulated BICS output of the circuit of Fig. 3.17 when Error Signal-1 for defect-1 is activated.
Figure 4.8: Simulated BICS output of the circuit of Fig. 3.17 when Error Signal-3 for defect-3 is activated.
Figure 4.9: Simulated BICS output with defects induced using fault injection transistors.
Figure 4.10: Influence of BICS on $V_{SS}$. 
Table 1 Theoretical \( I_{DDQ} \) for testable faults
Note: The reference current, \( I_{REF} = 400 \, \mu\text{A} \)

<table>
<thead>
<tr>
<th>Defect</th>
<th>Faulty ( I_{DDQ}, \mu\text{A} ) (simulated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M10DSS</td>
<td>1100</td>
</tr>
<tr>
<td>M5DSS</td>
<td>481.9</td>
</tr>
</tbody>
</table>
4.3 Simulated Oscillation Testing Results

The oscillator circuit of Fig. 2.16 has been simulated in SPICE for all the injected faults. As mentioned in Chapter 2, the natural oscillation frequency of the CUT oscillator is 875 kHz, obtained using Fast Fourier Transform (FFT) of Fig. 2.19 and the tolerance band of oscillation frequency is [-3.7%, 4.1%] obtained from Monte-Carlo analysis of Fig. 2.20. The value of $R_1$, $R_2$, $R$ and $C$ used are 1.6 k-ohm, 100 k-ohm, 20 k-ohm, and 100 pF for the simulations. The faults, which deviate from the nominal oscillation frequency range, are $M_{5GDS}$, $M_{11DSS}$, $M_{5DSS}$ and $M_{10DSS}$ while the faults which resulted in loss of oscillation are $M_{6GDS}$, $CCS$, and $M_{7GDS}$ and hence these have been detected. Figure 4.11 (i) – (viii) show the output oscillation frequencies for the injected faults $M_{10DSS}$, $M_{5GDS}$, $M_{5DSS}$, $M_{11DSS}$, $CCS$, $M_{7GDS}$, $M_{6GDS}$ and $M_{11G-VSS}$, respectively. The oscillation frequencies of these faults have also been obtained using the FFT analysis of the output waveforms. Table 2 summarizes the simulated deviations in oscillation frequency from the natural frequency due to fault injections. The simulated results show that the open fault $M_{11G-VSS}$ was also detected with a deviation of 15.71% from the natural frequency, thereby exceeding the limit of 4.1% for faults which show an increase in the oscillation frequency. The results also show that the fault $M_{11DSS}$ could not be detected, since the deviation observed in oscillation frequency with respect to natural frequency was within the lower tolerance limit of -3.7%. Table 3 summarizes the fault coverage obtained by oscillation testing in terms of the short and open faults injected. It can be seen from the Table 3 that the overall fault coverage obtained for the eight injected faults was 87.5%.
Figure 4.11: Output oscillation frequency for the injected faults (i) M10DSS (ii) M5GDS (iii) M5DSS (iv) M11DSS (v) CCS (vi) M7GDS (vii) M6GDS. (fig. con’d.)
(iii)

(iv)

(fig. con’d.)
Table 2: Simulated frequency deviations under fault injections.

<table>
<thead>
<tr>
<th>Fault injected</th>
<th>Output oscillation frequency ($f_{osc}$) (kHz)</th>
<th>Deviation from natural ($f_{nat} = 875$ kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M10DSS</td>
<td>1150</td>
<td>+31.42%</td>
</tr>
<tr>
<td>M5GDS</td>
<td>600</td>
<td>-31.54%</td>
</tr>
<tr>
<td>M5DSS</td>
<td>769.5</td>
<td>+12.05%</td>
</tr>
<tr>
<td>M11DSS</td>
<td>862.5</td>
<td>-1.42%</td>
</tr>
<tr>
<td>M11G-VSS</td>
<td>737.5</td>
<td>-15.71%</td>
</tr>
<tr>
<td>All others faults (M6GDS, CCS, M7GDS)</td>
<td>-</td>
<td>Loss of oscillation</td>
</tr>
</tbody>
</table>
Table 3(a): Simulated fault coverage of oscillation testing.

<table>
<thead>
<tr>
<th>Fault type</th>
<th>Total faults injected</th>
<th>Faults detected (with oscillation)</th>
<th>Faults detected (without oscillation)</th>
<th>Faults undetected (with oscillation)</th>
<th>Fault coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short</td>
<td>7</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>85.7%</td>
</tr>
<tr>
<td>Open</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>100%</td>
</tr>
<tr>
<td>Total</td>
<td>8</td>
<td>4</td>
<td>3</td>
<td>1</td>
<td>87.5%</td>
</tr>
</tbody>
</table>

Table 3(b): Simulated fault coverage of $I_{DDQ}$ testing.

<table>
<thead>
<tr>
<th>Fault type</th>
<th>Total faults injected</th>
<th>Faults detected (with a PASS/FAIL ‘high’)</th>
<th>Faults undetected (with a PASS/FAIL ‘low’)</th>
<th>Fault coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short</td>
<td>7</td>
<td>2</td>
<td>5</td>
<td>28.5%</td>
</tr>
<tr>
<td>Open</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>0%</td>
</tr>
<tr>
<td>Total</td>
<td>8</td>
<td>2</td>
<td>6</td>
<td>25%</td>
</tr>
</tbody>
</table>
4.4 Experimental Results

The post fabrication experimental results of the amplifier ac-characteristics are shown in Figure 4.12. The gain of the amplifier was observed to be 64.5 dB while its 3-dB bandwidth was around 5 kHz. Thus, gain-bandwidth product of the amplifier was observed to be 6 MHz. Figure 4.13 shows the measured output signal from the CMOS amplifier circuit for a sinusoidal input with peak-to-peak amplitude of 1.98 mV applied to the inverting terminal of the operational amplifier at a frequency of 5 kHz. Figure 4.14 shows the slewing response of the amplifier to an input step of 5 V (p-p). The rise time of the output is observed to be 722.4 ns for an output swing of $2.64 - (-2.2) = 4.84$ V, giving a slew rate of $\frac{4.84}{722.4} \text{ ns} = 6.7 \text{ V/µs}$ for the rising input.

Figure 4.15 shows the measured output signal from the CMOS oscillator circuit as implemented in Fig. 2.16 without any faults. This is the natural frequency of the oscillator which is observed to be 324 kHz using component values of $R=2.56 \text{ k-ohm}$, $C=25 \text{ pF}$, $R_1=650 \text{ ohm}$, $R_2=2.556 \text{ k-ohm}$ in the circuit of Fig 2.16. The faults, which have deviated from the nominal oscillation frequency range are $M_5$ drain source short (M5DSS), $M_{11}$ drain-source short (M11DSS) and $M_{11}$ gate bias, $V_{BIAS}$ connected to $V_{SS}$ (M11G-VSS). Figure 4.16 (i)-(viii) show the faulty oscillation frequencies corresponding to the injected faults respectively. The measured frequency deviation due to injected faults is summarized in Table 3. The open-fault (M11G-VSS) could not be detected as no significant ($< -3.7\%$) deviation from the natural frequency could be observed. On the other hand, defect M11DSS shows a significant deviation of -14.7% from its natural frequency and hence could be detected. This discrepancy between the simulated and experimental results can be accounted due the variation in model parameters used for the
design and physical realizations of the amplifier which would also account for the
difference in its simulated and observed frequency response characteristics. In a given
oscillator, the oscillation frequency depends on a wide range of the ac behavior of its
transfer function. For the oscillator circuit of Fig. 2.16, the oscillation frequency depends
on the entire range of its open-loop ac behavior having greater than unity gain. Since we
observed that there is a significant difference in the simulated and observed frequency
response characteristics, the oscillation frequency will get affected.

Figures 4.17 (i) - (iii) show the wave forms obtained from the logic analyzer. The
BICS is tested for its operation in the normal mode and test mode by giving a digital
input with varying frequencies to the $V_{\text{ERROR}}$ (fault-M10DSS) and $V_{\text{ENABLE}}$ voltages.
When the $V_{\text{ENABLE}}$ is ‘low’, the BICS is in the test mode and if the error signal is ‘high’,
PASS/FAIL gives logic ‘1’ and thus, it detects the fault induced. When the $V_{\text{ENABLE}}$ is
‘low’, the BICS is in the normal mode, PASS/FAIL gives logic ‘0’ irrespective of $V_{\text{ERROR}}$
and thus no fault is detected. Figures 4.17 (iv) and (v) show the measured PASS/FAIL
signal from the BICS output under multiple fault-injection conditions. In Fig. 4.17(iv),
the $V_{\text{ENABLE}}$ is connected to GND (‘low’) thus enabling the BICS. When the $V_{\text{ERROR}}$
(fault-M10DSS) or $V_{\text{ERROR}}$ (fault-M5DSS) is high the PASS/FAIL gives logic ‘1’
indicating the presence of a fault. In Fig. 4.17(v) the $V_{\text{ENABLE}}$ is connected to 1 MHz
signal and $V_{\text{ERROR}}$ is connected to 1 kHz while $V_{\text{ERROR}}$ is being held at $V_{\text{DD}}$. In Figs.
4.17 (vi) and (vii) the $V_{\text{ENABLE}}$ is given a digital input at a frequency of 1 MHz and
$V_{\text{ERROR}}$ is given 1 kHz and 1 MHz respectively. This is the frequency at which the BICS
output starts to show a delay in phase with respect to the $V_{\text{ENABLE}}$ signal. Thus, the
maximum speed at which the designed BICS could be operated is observed to be 1 MHz.
Figure 4.12: Experimental ac-characteristics of the designed amplifier.
Figure 4.13: Output response of the amplifier for an input sinusoidal p-p of 200 mV applied across a voltage divider consisting of 1 k-ohm and 100 k-ohm at 5 kHz.
Figure 4.14: Step response of the amplifier to an input step of -2.5 to 2.5 V.

Note: The rise time of the output is observed to be 722.4 ns for an output swing of 2.64-(-2.2) = 4.84 V, giving a slew rate of 4.84/722.4 ns = 6.7 V/µs for the rising input.
Figure 4.15: Experimental natural oscillation frequency.
Figure 4.16 (i): Experimental faulty (defect-1 M10DSS) oscillation frequency with $V_{E1}$ connected to $V_{DD}$. 
Figure 4.16 (ii): Experimental faulty (defect-2 M5GDS) oscillation frequency with $V_{E2}$ connected to 5V.
Figure 4.16 (iii): Experimental faulty (defect-3 M5DSS) oscillation frequency with $V_{E3}$ connected to 5V.
Figure 4.16 (iv): Experimental faulty (defect-4 M11DSS) oscillation frequency with $V_{E4}$ connected to 5V.
Figure 4.16 (v): Experimental faulty (defect-5 CCS) oscillation frequency with $V_{E5}$ connected to 5V.
Figure 4.16 (vi): Experimental faulty (defect-6 M7GDS) oscillation frequency with $V_{E6}$ connected to 5V.
Figure 4.16 (vii): Experimental faulty (defect-7 M6DSS) oscillation frequency with $V_{E7}$ connected to 5V.
Figure 4.16 (viii): Experimental faulty (defect-8 M11G-VSS) oscillation frequency with M11 gate connected to $V_{SS}$.
Table 4: Observed frequency deviations under fault injections

<table>
<thead>
<tr>
<th>Fault injected</th>
<th>Deviation from $f_{nat}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M10DSS</td>
<td>+23.2%</td>
</tr>
<tr>
<td>M5GDS</td>
<td>-78.6%</td>
</tr>
<tr>
<td>M5DSS</td>
<td>+26.3%</td>
</tr>
<tr>
<td>M11DSS</td>
<td>-14.7%</td>
</tr>
<tr>
<td>M11G-VSS</td>
<td>-1.6%</td>
</tr>
<tr>
<td>All others</td>
<td></td>
</tr>
<tr>
<td>faults(M6GDS,</td>
<td></td>
</tr>
<tr>
<td>CCS, M7GDS)</td>
<td>Loss of oscillation</td>
</tr>
</tbody>
</table>
Table 5: Detected faults using theoretical and observed results for oscillation testing

<table>
<thead>
<tr>
<th>Fault injected</th>
<th>Fault detected (Simulated)</th>
<th>Fault detected (Observed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M10DSS</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>M5GDS</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>M5DSS</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>M11DSS</td>
<td>-</td>
<td>x</td>
</tr>
<tr>
<td>M11G-VSS</td>
<td>x</td>
<td>-</td>
</tr>
<tr>
<td>M6GDS</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>CCS</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>M7GDS</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>
Figure 4.17(i): BICS showing PASS/FAIL output from HP1660CS logic analyzer corresponding to fault M10DSS. $V_{\text{ENABLE}}$ and $V_{\text{ERROR}}$ are given a 1 kHz signal.
Figure 4.17(ii): BICS showing PASS/FAIL output from HP1660CS logic analyzer corresponding to fault M10DSS. $V_{\text{ENABLE}}$ and $V_{\text{ERROR}}$ are given a 5 kHz signal.
Figure 4.17(iii): BICS showing PASS/FAIL output from HP1600CS Logic Analyzer corresponding to fault M10DSS. V\textsubscript{ENABLE} connected to 400 Hz signal and V\textsubscript{ERROR} is connected to 1 kHz.
Figure 4.17(iv): BICS showing PASS/FAIL output from HP1660CS logic analyzer corresponding to faults M10DSS and M5DSS. $V_{\text{ENABLE}}$ is connected to GND (BICS active) and Error-signals ($V_{\text{ERROR}}_{1,2}$) are given a 1 kHz signal.
Figure 4.17(v): BICS showing PASS/FAIL output from HP1600CS Logic Analyzer corresponding to fault M10DSS. $V_{\text{ENABLE}}$ connected to 1 MHz signal and $V_{\text{ERROR}_1}$ is connected to 1 kHz while $V_{\text{ERROR}_2}$ is being held at $V_{\text{DD}}$. 
Figure 4.17(vi): BICS showing PASS/FAIL output from HP1600CS Logic Analyzer corresponding to fault M10DSS. \( V_{\text{ENABLE}} \) connected to 1 MHz signal and \( V_{\text{ERROR}} \) is connected to 1 kHz.
Figure 4.17(vii): BICS showing PASS/FAIL output from HP1600CS Logic Analyzer corresponding to fault M10DSS. $V_{\text{ENABLE}}$ and $V_{\text{ERROR}}$ connected to 1 MHz signal.
CHAPTER 5
CONCLUSION AND SCOPE OF FUTURE WORK

The CMOS amplifier is designed in standard 1.5µm n-well CMOS technology, which operates with ±2.5 V supply voltages. A two-step testing methodology for testing the amplifier is presented: 1) Oscillation test-mode, in which a closed loop feedback network enables the CUT to oscillate with the BICS being disabled. 2) IDDQ test-mode, in which inputs of the CUT (amplifier) are grounded, and the BICS operation is enabled. Use of the combined oscillation and IDDQ testing method has improved the fault confirmation and can be used to provide additional insights to help identify the fault locations, thus aiding in fault-isolation. The approach is attractive because of its simplicity and robustness. The technique uses linear resistors and capacitors, which can also be integrated on-chip. The method can easily be extendable to BIST because it doesn’t require external test stimuli and uses a simple measurement. The advantages of the technique are high fault coverage, reduced test time, simple test procedure, and the elimination of a test vector process.

To increase the precision of the test we need a little additional digital circuitry to evaluate the oscillation frequency. This implementation can be done on-chip using a frequency to number converter (FNC), which converts the oscillation frequency into an M-bit number, and a control logic (CL) block [26] which directs all operations and produces the PASS/FAIL test result of the combined test. A simple block diagram of the BIST scheme is presented in Fig. 5.1. The present test method could be extended to larger circuit blocks like Sigma-Delta Modulators and PLLs.
Figure 5.1: Block Diagram of the proposed BIST scheme
BIBLIOGRAPHY


APPENDIX A
SPICE LEVEL 3 MOS MODEL PARAMETERS FOR STANDARD N-WELL CMOS TECHNOLOGY [43]

(A) Model Parameters for n-MOS transistors.

.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+ TPG=1 VTO=0.687 DELTA=0.0000E+00 LD=1.0250E-07 KP=7.5564E-05
+ UO=671.8 THETA=9.0430E-02 RSH=2.5430E+01 GAMMA=0.7822
+ NSUB=2.3320E+16 NFS=5.9080E+11 VMAX=2.0730E+05 ETA=1.1260E-01
+ KAPPA=3.1050E-01 CGDO=1.7294E-10 CGSO=1.7294E-10
+ CGBO=5.1118E-10 CJ=2.8188E-04 MJ=5.2633E-01 CJSW=1.4770E-10
+ MJSW=1.00000E-01 PB=9.9000E-01

(B) Model Parameters for p-MOS transistors.

.MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+ TPG=-1 VTO=-0.7574 DELTA=2.9770E+00 LD=1.0540E-08 KP=2.1562E-05
+ UO=-191.7 THETA=1.2020E-01 RSH=3.5220E+00 GAMMA=0.4099
+ NSUB=6.4040E+15 NFS=5.9090E+11 VMAX=1.6200E+05 ETA=1.4820E-01
+ KAPPA=1.00000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=4.2580E-10 CJ=2.9596E-04 MJ=4.2988E-01 CJSW=1.8679E-10
+ MJSW=1.5252E-01 PB=7.3574E-01
APPENDIX B
CHIP TESTABILITY (CHIP #: MOSIS T37C-BP)

Figure B.1 shows the 2-stage op-amp with BICS in the 2.25 mm × 2.25 mm padframe. It consists of individual sub-modules for testing the chip.

(B.1) Inverter module testing:

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Input</td>
</tr>
<tr>
<td>14</td>
<td>Output</td>
</tr>
</tbody>
</table>

DC test was performed on the independent inverter module to test if the chip did not have fabrication problems. Logic ‘0’ is applied at the input pin #16 and output (logic ‘1’) is observed on the pin #14. Logic ‘1’ is applied at the input pin #13 and output (logic ‘0’) is observed on pin #14.

(B.2) Operational amplifier module and functional testing

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>Negative op-amp input (V⁻)</td>
</tr>
<tr>
<td>37</td>
<td>Positive op-amp input (V⁺)</td>
</tr>
<tr>
<td>2</td>
<td>op-amp output (V_{OUT})</td>
</tr>
<tr>
<td>4</td>
<td>Biasing Input (V_{BIAS})</td>
</tr>
</tbody>
</table>

The op-amp is tested in the unity gain configuration by connecting pin #2 to the negative op-amp input pin #36 and giving a 10 mV sine wave to the positive input pin #37. The output has been observed at the pin #2. It has also been tested in the comparator mode by supplying a 4V peak-to-peak sine wave to the positive input pin #37 observing the output at pin #2 while the negative input pin is being grounded.
Table B.1 summarizes the pin numbers and their description to test the two-stage op-amp.

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BICS output ($V_{BICS}$)</td>
</tr>
<tr>
<td>2</td>
<td>op-amp output ($V_{OUT}$)</td>
</tr>
<tr>
<td>3</td>
<td>Virtual $V_{SS}$ ($V_{VSS}$)</td>
</tr>
<tr>
<td>4</td>
<td>Error Signal-8/ EXT input ($V_{E8}/V_{BIAS}$)</td>
</tr>
<tr>
<td>5</td>
<td>$V_{DD}$ (Corner pad)</td>
</tr>
<tr>
<td>6</td>
<td>Error Signal-7 ($V_{E7}$)</td>
</tr>
<tr>
<td>7</td>
<td>Error Signal-6 ($V_{E6}$)</td>
</tr>
<tr>
<td>8</td>
<td>Error Signal-5 ($V_{E5}$)</td>
</tr>
<tr>
<td>9</td>
<td>Error Signal-4 ($V_{E4}$)</td>
</tr>
<tr>
<td>10</td>
<td>$V_{SS}$</td>
</tr>
<tr>
<td>11</td>
<td>Error Signal-3 ($V_{E3}$)</td>
</tr>
<tr>
<td>12</td>
<td>Error Signal-2 ($V_{E2}$)</td>
</tr>
<tr>
<td>13</td>
<td>Error Signal-1 ($V_{E1}$)</td>
</tr>
<tr>
<td>14</td>
<td>Output of test inverter ($INV_{OUT}$)</td>
</tr>
<tr>
<td>15</td>
<td>$V_{DD}$ (Corner pad)</td>
</tr>
<tr>
<td>16</td>
<td>Input of test inverter ($INV_{IN}$)</td>
</tr>
<tr>
<td>17</td>
<td>2nd op-amp Virtual $V_{SS}$ ($V_{VSS}$)</td>
</tr>
<tr>
<td>18</td>
<td>2nd op-amp node ($M_{6G}$)</td>
</tr>
<tr>
<td>19</td>
<td>2nd op-amp node ($V_{RZCC}$)</td>
</tr>
<tr>
<td>20</td>
<td>2nd op-amp node ($M_{5D}$)</td>
</tr>
<tr>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>---</td>
<td>--------------------------------------</td>
</tr>
<tr>
<td>21</td>
<td>2nd op-amp node (M3G)</td>
</tr>
<tr>
<td>22</td>
<td>2nd op-amp node (M10D)</td>
</tr>
<tr>
<td>23</td>
<td>2nd op-amp negative input (V-)</td>
</tr>
<tr>
<td>24</td>
<td>2nd op-amp positive input (V+)</td>
</tr>
<tr>
<td>25</td>
<td>VSS (Corner pad)</td>
</tr>
<tr>
<td>26</td>
<td>2nd op-amp BICS enable (V_ENABLE)</td>
</tr>
<tr>
<td>27</td>
<td>2nd op-amp BICS output (VBICS)</td>
</tr>
<tr>
<td>28</td>
<td>2nd op-amp EXT pin (EXT)</td>
</tr>
<tr>
<td>29</td>
<td>2nd op-amp output (VOUT)</td>
</tr>
<tr>
<td>30</td>
<td>VDD</td>
</tr>
<tr>
<td>31</td>
<td>op-amp node (M10D)</td>
</tr>
<tr>
<td>32</td>
<td>op-amp node (M5D)</td>
</tr>
<tr>
<td>33</td>
<td>op-amp EXT pin (EXT)</td>
</tr>
<tr>
<td>34</td>
<td>op-amp node (VRZCC)</td>
</tr>
<tr>
<td>35</td>
<td>VSS (Corner pad)</td>
</tr>
<tr>
<td>36</td>
<td>op-amp negative input (V-)</td>
</tr>
<tr>
<td>37</td>
<td>op-amp positive input (V+)</td>
</tr>
<tr>
<td>38</td>
<td>op-amp node (M6G)</td>
</tr>
<tr>
<td>39</td>
<td>op-amp node (M3G)</td>
</tr>
<tr>
<td>40</td>
<td>op-amp BICS Enable (V_ENABLE)</td>
</tr>
</tbody>
</table>
(B.4) Testing the two-stage op-amp in its normal mode

1. Supply voltages of ± 2.5V is given to the power supply pins of the chip (V_{DD}=2.5 V and V_{SS}=-2.5 V).

2. The V\text{DISABLE} \text{pin} (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode.

3. The EXT pin (#33) is connected to the V_{SS} (-2.5 V) when the BICS is in the normal mode. (V\text{ENABLE}= ‘1’ =+2.5 V) and V\text{BIAS} \text{pin} (#4) is connected to V_{DD} (+2.5 V).

4. The fault injection transistors must be de-activated by giving a ‘low’ voltage (-2.5 V) to the error-signals V_{E1}, V_{E3}, V_{E4}, V_{E5}, V_{E6}, V_{E7}.

5. The two-stage op-amp is tested by giving sinewave input in the unity gain feedback mode and comparator mode.

6. The output is observed at pin #2 using an oscilloscope.

(B.5) Testing of the op-amp in IDDQ test mode

1. The V\text{DISABLE} \text{pin} (#40) is given a ‘low’ voltage (-2.5 V), which makes the BICS to function in the test mode.

2. The fault injection n-MOS transistors of the observable faults are activated by connecting the error signals V_{E1}, V_{E3} to a ‘high’ voltage (+2.5 V).

3. The reference current generated on chip is about 450 µA.

4. When the error signals are activated, faults are injected into the chip and the faulty current shoots up to 1.1 mA and 480 µA for V_{E1} and V_{E3}, respectively.

5. The PASS/FAIL output is observed at pin #1. The output of the BICS shows a HIGH value (PASS/FAIL = ‘1’ = +2.5 V) when the faults are injected into the chip and when the
BICS is in test mode. When the BICS is in the normal mode the output is LOW (PASS/FAIL = ‘0’ = -2.5 V).

(B.6) Observing the operation of BICS using Logic Analyzer HP 1660CS

1. The V_ENABLE is given a pulse input. When the pulse input is ‘high’ the BICS is in the normal mode of operation while a ‘low’ pulse input makes the BICS to function in the test mode.
2. The Error-Signal is given a high voltage (+2.5 V).
3. The PASS/FAIL output is observed at pin #1. The output of the BICS shows a HIGH value (PASS/FAIL = ‘1’ = +2.5 V) when the V_ENABLE is ‘low’ and the Error-Signal ‘high’.
4. The output of the BICS shows a low value (PASS/FAIL = ‘0’ = -2.5 V) when the V_ENABLE is ‘high’ irrespective of the Error-Signal being ‘high’ or ‘low’ since the BICS has not been enabled.

(B.7) Testing the two-stage op-amp in oscillation test mode

1. The V_ENABLE pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode while the EXT pin (#33) is connected to the VSS (-2.5 V) and EXT in pin (#4) is connected to the VDD (+2.5 V) to enable the normal operation of the op-amp.
2. Add the following external circuit components. Resistors R_1 between op-amp output (V_{OUT}) pin #2 and positive input (V^+) of the op-amp pin #37, R_2 between positive input (V^+) and Common Ground of the power supply (V_{GND}), R between op-amp output (V_{OUT}) and negative input (V^-) of the op-amp pin #36 and capacitor C, between negative input (V^-) and common ground (V_{GND}).
3. Observe the oscillations being output at the op-amp output (V_{OUT}) pin #2.
4. Measure the natural oscillation frequency of the op-amp ($f_{\text{osc}}$) using an oscilloscope.

5. A tolerance band of oscillation frequency is obtained using Monte-Carlo simulation taking into consideration the tolerances of all components that would affect the natural frequency of the designed oscillator. It is observed to be around $<-4.5\%, 2.3\%>$.

6. $V_{\text{BIAS}}$ pin (#4) can be used as an Error-Signal-8 ($V_{E8}$), if it is connected to the $V_{\text{SS}}$ (-2.5V).

7. The fault injection transistors of the faults are activated by giving a ‘high’ voltage (+2.5 V) to the error-signals $V_{E1}$-$V_{E7}$ and the open-fault is activated by giving a ‘low’ voltage (-2.5 V) to the error-signal $V_{E8}$.

8. When the error signals are activated, faults are injected into the chip, which manifest themselves as a deviation from the natural oscillation frequency much above the tolerance range. This deviation is observed using the oscilloscope.
Fig B.1: 2-stage op-amp with BICS in the 2.25mm × 2.25mm padframe
VITA

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