2003

# Circuitry for a remotely powered bio-implantable gastric electrical stimulation system

Satish Kona
*Louisiana State University and Agricultural and Mechanical College*

# CIRCUITRY FOR A REMOTELY POWERED BIO-IMPLANTABLE GASTRIC ELECTRICAL STIMULATION SYSTEM

A Thesis
Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering

in

The Department of Electrical and Computer Engineering

by
Satish Kona
B.S., Andhra University, India, 2001
December 2003

**Dedicated to my parents**

# ACKNOWLEDGEMENTS

I would like, first, to express my deepest appreciation for the technical guidance and support given by my research advisor, Professor Pratul K. Ajmera. His thorough understanding of the many issues fundamental to circuit operation, his attention to details and basics that most often govern the behavior of even the most complex of problems will always be remembered. Needless to say, his belief in me made this work possible.

I would like to thank Dr. Ashok Srivastava and Dr. Martin Feldman for their valuable suggestions and for being a part of my examination committee.

I want to dedicate this work to my parents and sister for their continuous guidance, encouragement, prayers, love and support throughout my life.

I would like to thank Anand k Chamakura, my fellow M.S. student without whose help I would still be toiling trying to solve some complex design problems. I would like to thank all my friends especially Inhyouk Song, Tinghui Xin, Kopparthi Sunitha, Yernagula Jagdish, Ripan Das and Chuang Zhang for their helpful discussions and suggestions. There are countless other people whose names and faces pass through my mind as I ruminate about this period at LSU. So, I would have to include all of them saying that it was really a pleasure knowing them and that aspect, as much as anything else, made this whole journey worthwhile.

My gratitude to the Department of Electrical and Computer Engineering for providing partial support to me throughout my stay at LSU as teaching assistant. Last, but not the least, I gratefully acknowledge the partial support as research assistant, from the NSF and Louisiana Board of Regents through the EPSCoR research grant # 0092001.

# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# ABSTRACT

Power to bio-implantable devices is usually supplied through a battery implanted with the system or through wires extending to an outside power source. The latter case with wires protruding out of the body can be unaesthetic in appearance and can cause infection. In this research, we consider an alternative way to power a bio-implantable microsystem. It involves using rechargeable lithium batteries. Here, power is delivered remotely to charge implanted battery or batteries. This approach avoids periodic surgery necessary for battery replacement. It also does not tie a person to an external power source at all times. This improves patient's quality of life.

The present work involves design and fabrication of signal conditioning circuit for a remotely rechargeable, bio-implantable, Battery-powered Electrical Stimulation System (BESS). A rechargeable lithium ion battery with a voltage of 3.7 V powers the proposed circuit. The desired output, which goes directly to the electrodes, is a series of 10 V, 15 mA pulses with a duty cycle of 4.5 %. A second rechargeable lithium ion battery serves as back-up. A lithium ion charging chip is included which is connected to the designed IC through a logic interface. The two batteries work in tandem i.e. when one battery powers the IC the other gets recharged and vice versa thereby providing an uninterruptible output. The IC uses a series of charge pumps to get the required boost in voltage. The IC also includes voltage detector circuits to detect battery voltages, voltage regulator, pulse generator circuits, logic circuits and necessary switches.

Individual subsystems of the IC were designed, simulated and fabricated using standard CMOS technology. Individual subsystem circuits were found to work satisfactorily except for the charge pump. A revised design is now under fabrication.

The microsystem utilizes a hybrid approach. Experiments done with a bench-top circuit model to simulate the proposed IC showed that a 3 V battery with a capacity of 190 mAh could power the IC for 15 hrs and needed 4 hrs for recharging.

# 1. INTRODUCTION

## 1.1 Need for Current Work

Use of electrical stimulation system for the purpose of controlling a nerve or muscle is well known. Today, electric stimulation has many uses in the medical field and is often called Functional Electrical Stimulation (FES) or Functional Neuromuscular Stimulation (FNS). The basic principle behind stimulation is use of small electric signals to excite nerves or muscles that either no longer function or need excitation to perform some useful function. This technology can be used in many applications. The application most commonly associated with FES is the controlled stimulation of muscles in order to return some level of function. This technology is most often used for patients with spinal cord or head injuries, multiple sclerosis, or cerebral palsy. FES can be used to strengthen muscles or to create motion [1].

The first successful use of FNS was in the decade of 1960 [2]. These systems were placed entirely external to the body and stimulation currents were passed through the skin by directly placing the electrodes on the skin. Apart from being large and bulky, these systems required exact electrode placement each time the system was used. In the next decade, FNS systems were improved by incorporating percutaneous electrodes with leads running out through the skin. This improved the range of stimulation and eliminated the need for continuous repositioning of skin electrodes, but lead breakage, system bulkiness, and infection still made these systems problematic [2].

Implantable electrical stimulation systems replaced these older systems. Power to implantable systems is generally supplied from a battery source implanted inside the body or from an externally wearable power source, either via a direct electrical or via a

wireless electromagnetic coupling such as radio frequency (RF) link. In the latter case, an antenna transmits energy through the patient's skin to a subcutaneous receiver. The receiver end must also have circuitry to condition and transmit the energy received to electrodes implanted to stimulate nerve or muscle tissues [3].

If the receiver is powered through a battery implanted with the system then the battery will need periodic replacement. This will entail surgical procedure. If the receiver is connected to the outside power source by wires, then wires protruding from the skin give not only an unaesthetic appearance but can also be a source of infection. The receiver can also be powered directly by the energy derived from an external wireless transmitter but in most cases it restricts the person to being in a close proximity to the transmitter at all times. The other alternative is to have the person carry the transmitter at all times. These options are either not always practical or inconvenient.

Although many systems using implanted batteries have been developed over the years, these prior systems suffer from many problems. First the stimulating circuitry has a number of discrete devices on separate circuit boards making it large and bulky. Second, some stimulations especially muscle stimulation need high energy that require larger capacity implanted battery or require placing batteries in series, making the system large and sometimes unfeasible for implantation. Third, there is a need for periodic surgery for replacing the batteries. Fourth, the system is application specific making it difficult to adopt for other applications [4]. In order to overcome the above shortcomings, the system should be as compact as possible even if hybrid techniques are used. There should also be some built-in flexibility in the circuit design. The battery should be made as small as possible to reduce the system size. These issues are addressed in this research.

In this research, we consider an alternative way to power a bio-implanted micro-system. It involves using rechargeable lithium batteries. Here, power is delivered remotely to charge implanted battery or batteries. This approach avoids the use of a continuous external power source. External remote source is used only for the time needed to recharge the batteries. This approach also avoids periodic surgery necessary for battery replacement. This freedom is important in improving quality of life of the patient.

**1.2 Review of Past Research**

There is evidence that ancient Egyptians used electrogenic fish to treat ailments in 2500 B.C. although the Roman physician Scribonius Largus is credited with the first documented report of the use of electrogenic fish in medicine in 46 A.D.

The use of electricity in medicine increased with the development of electrostatic generators in the eighteenth century. However its popularity declined in the nineteenth and early twentieth century due to variable clinical results and the development of alternative treatments. In 1965, Melzack and Wall [5] reawakened interest in the use of electricity to relieve pain by providing a physiological rationale for electro-analgesic effects. In 1967, Wall and Sweet [6] used high-frequency percutaneous electrical stimulation to artificially activate nerves that conduct impulses from the periphery of the body to the brain or spinal cord and found that this relieved chronic pain in patients. In the same year Shealy, Mortimer and Reswick [7] found that electrical stimulation of the dorsal columns, which form the central transmission pathway from the periphery of the body to the brain or spinal cord, also produced pain relief. Pain relief was also demonstrated by Reynolds in 1969 [8] when electrical currents were used to stimulate the periaqueductal grey (PAG) region of the midbrain.

A great technological break through occurred in 1947 with the invention of the transistor at bell laboratories. This was followed by the development of integrated circuits that was critical in the development of compact, portable, implantable prosthetic devices. With these new techniques, fabrication of a variety of neural prosthetic devices was made practical.

In the area of telemetry powered implantable devices, Loucks, Chaffee and Light in 1935 [9] independently investigated the possibility of transferring power and data to an implanted device via an inductively coupled transformer link, which greatly reduced the infection and discomfort associated with the use of percutaneous electrodes [10].

During the last decade, significant work has been done in the development of RF-powered electronics to stimulate the nerves and retinas of those with certain diseases. Ziaie (1994) presented a single channel micro stimulator for FNS used to restore function in disabled individuals. The micro stimulator was a hybrid integrated circuit chip consisting of a receiver-electrode package to be implanted through a hypodermic needle and a transmitter to supply power and data to the receiver through an inductively coupled link [4]. In 1998, Von Arx presented a fully integrated neuromuscular stimulation system, called FINESS, used to stimulate nerves in patients with paralysis. Von Arx used a wireless system, which eliminated leads. The latter tend to break off or damage nerves when implanted [2]. Separately, Mark Clements (1999) at North Carolina State University described a retinal stimulator being developed with the Wilmer Eye Institute at John Hopkins University. The idea is to restore eyesight lost due to macular degeneration or retinal pigmentosa, two common conditions that cause failure in the rods and cones that act as the eye's photoreceptors. The system consists of an extraocular unit

and an intraocular unit that are coupled together via a wireless inductive telemetry link. The extraocular unit provides for image acquisition and processing and consists therefore of an external camera, image processor, telemetry encoder, RF amplifier and a primary coil. The intraocular unit receives power and data from the extraocular unit [11].

The research reported in this thesis also deals with the design of a wireless stimulator but unlike the other stimulator systems where power is supplied from an externally wearable source, the system in this work uses internal rechargeable batteries as a source of power and uses an external transmitter to recharge these batteries. This approach does not require the use of external powering source at all times but employs it only for a relatively short duration needed to recharge the batteries.

**1.3 Stimulator System Overview**

This thesis describes the development of hybrid circuitry for a remotely powered bio-implantable nerve stimulation system. Rechargeable batteries are used to power the bio-implanted stimulation system. A remote external transmitter supplies power to recharge the batteries. The most important requirements for the stimulator system design are power consumption and overall dimensions of the stimulator circuitry. The aim is to make the system as fully integrated and hence as compact as possible. The stimulator circuitry should be able to deliver sufficiently high amount of charge for gastric nerve pacing. As discussed in chapter 3, this necessitates use of external capacitors and hence a hybrid approach is undertaken in this work. For a lower power requirement case, the system can be fully integrated. The stimulator circuit also includes a battery charging circuit, which is a hybrid component of the system as well.

Remotely rechargeable, bio-implantable, battery-powered electrical stimulation

system developed in this work is called BESS. The block diagram of a remotely powered implantable stimulator is shown in the figure 1.1. As shown in the figure, the system consists of an external transmitter for signal and power. The implantable receiver system usually consists of a signal and power receiver antenna followed by a signal conditioning block with a pulse generator for stimulation. The receiver picks up the signal and power from the external transmitter via a telemetry link. The signal conditioning block and the pulse generator function according to the signals received and deliver the desired output, which is a series of pulses to electrodes placed adjacent to nerves or muscles to be stimulated. Development of pulse generator and signal conditioning block is the main focus of this thesis.

A bio-implantable system which has rechargeable batteries can be recharged externally from outside the body. This has a number of advantages. First, there is no need to have periodic surgery for battery replacement as the battery can be recharged repeatedly. Second, there is no need for an external transmitter except for during the time necessary for recharging the battery. Third, a smaller size battery can be used, which is an advantage in all bio-implantable systems. A larger battery means longer time between recharging or replacement but requires a bulkier system. Figure 1.2 shows the general overview of BESS. As seen in the figure 1.2, the implanted system for BESS has a receiver, a battery charging chip and a signal conditioning IC. The receiver antenna is usually a coil, which is used to receive power from an external transmitter through mutual inductive coupling. This coupled power is then used at the receiver end to recharge the implanted local batteries. Two rechargeable lithium ion batteries are used here to power the receiver. The second rechargeable lithium ion battery serves as back up

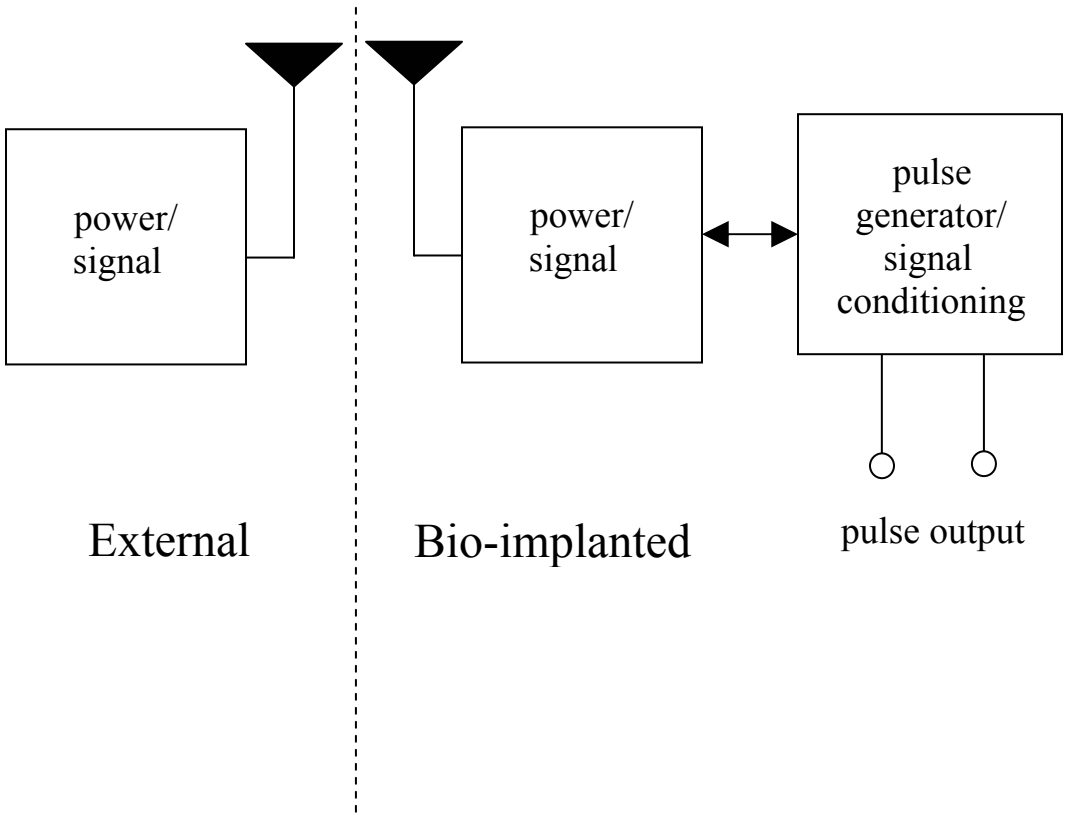



Figure 1.1: Block diagram of a remotely powered stimulator system.

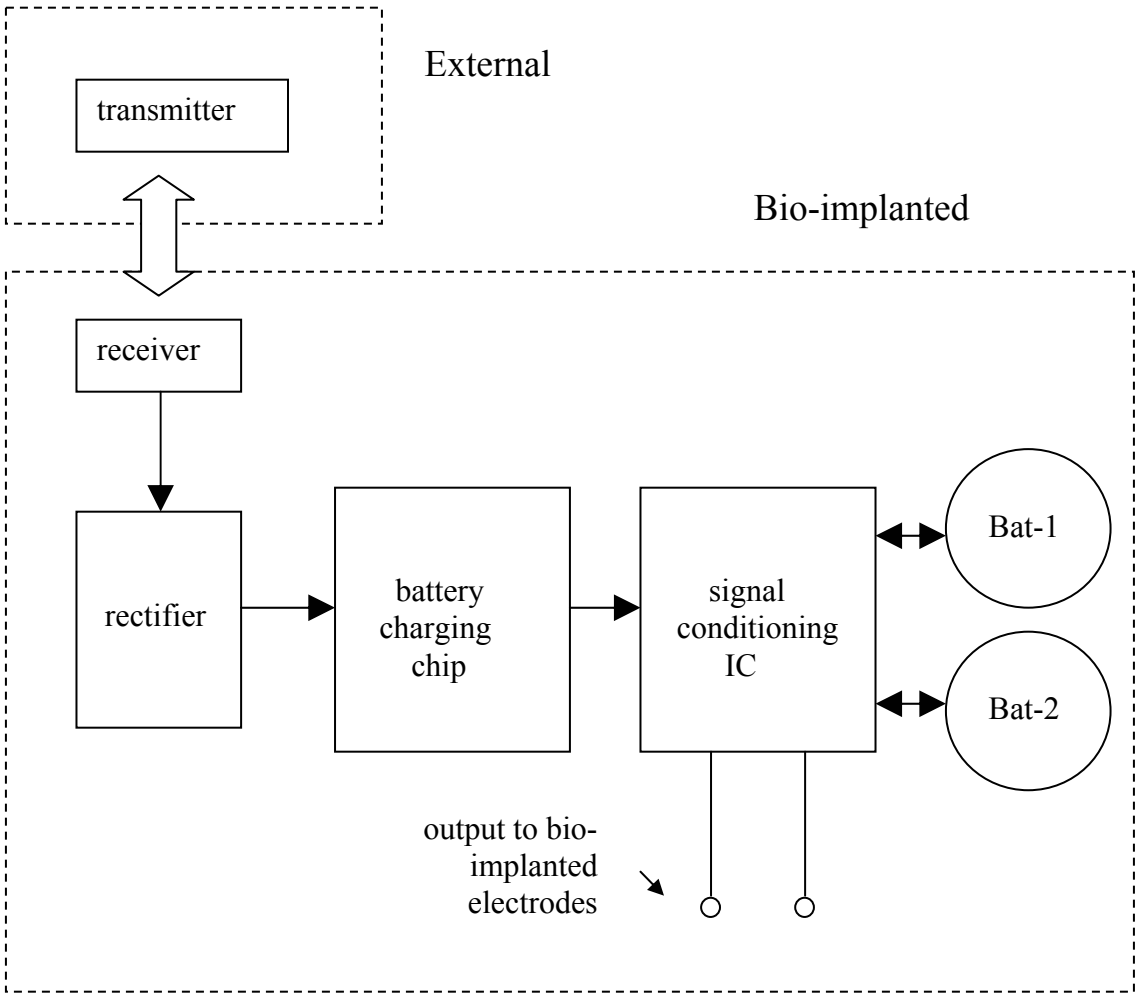



Figure 1.2: Operation overview of BESS.

whilst the first battery is in use. Using two batteries also helps in increasing the life time of the bio-implanted device.

### 1.4 Research Objectives and Organization of Thesis

This research aims at overcoming some of the limitations and shortcomings of the present nerve stimulation systems that use wires protruding out of the body or need constant external transmitter. In particular the goals of this thesis are:

- Develop circuitry for a fully implantable battery powered stimulator, which requires external transmitter only for recharging the batteries.
- To design the system so that it can be made as compact as possible.
- To design robust system with back up power arrangement.
- To make the circuit design flexible so that it can be adopted for other applications with simple modifications.

Chapter 2 of this thesis gives the general background and describes the principles of nerve stimulation. Various power sources in implantable devices are also considered along with the role of rechargeable batteries as power sources. Chapter 3 deals with the architecture of the stimulator circuitry followed by circuit design and simulation results. Chapter 4 gives experimental results on the fabricated chip. Chapter 5 gives conclusions and suggestions for further work.

# 2. BACKGROUND

Human body is an electrical wonder. Tiny electrical currents and charges are found in all tissues at the cellular level throughout the body. The most basic bio-chemical functions that occur in cells are directed, in part by their electrical or ionic charges; either positive or negative. This knowledge has allowed researchers to learn and develop more ways to apply electrical stimulation to the body to regulate and to enhance functions such as heart, muscle/movement, soft tissue healing, and bone growth/healing and pain. This understanding of the body's use of electrical signals has allowed science to develop ways to aid and heal debilitating human physical conditions [12].

The first electrical stimulators used surface electrodes, which were simply placed on the skin surface, to activate the muscles. External stimulation, however, did not succeed in achieving the expected results. This failure was primarily due to the discomfort suffered by patients when high levels of stimuli were applied. The other problem was that the stimulation could only be done in offices or hospitals, which resulted in inadequate stimulation of the muscles. Implantable electrical stimulation systems can replace these older systems. Functional electrical stimulation technology is improving, and newer devices that are more compact and efficient to solve a particular problem are being developed by refining older devices. As technology improves, newer stimulators with improved controls which perform complex tasks will be made to help individuals with nerve injuries [13].

## 2.1 Principles of Nerve Stimulation

Tissues can be excited by a wide range of stimuli. The kind of stimuli can range from mechanical trauma to intense magnetic fields. When stimulus is applied to a membrane,

temporary unbalance takes place between the electric charges of the membrane. And when the membrane is depolarized to a threshold voltage level, the regenerative mechanisms of the action potential take over. In the commonest method of stimulation, a pair of wire electrodes is placed on or near a nerve and pulses of electric current are passed between the electrodes, under control of an electric stimulator [14].

Neurons, commonly known as nerve cells, largely constitute the nervous systems. They enable multi-celled organisms to react to their environment and respond to their ever-changing conditions. Neurons have long, specialized outgrown tissues called axons, which digitize data for local transmission, and for transmitting data over long distances. A coat of extra-cellular fluid surrounds a single axon. During the stimulus, an axon is mounted on a pair of perfect electrodes (non polarizable and of zero resistance) and a constant current I flow between the electrodes as indicated in figure 2.1. The arrows indicate the vector current flux of the stimulation current. Here the trans-membrane current is assumed to flow between the anode and the cathode. Ignoring capacitive effects, the axon may be represented by a resistive network shown in figure 2.2. Here $R_o$ is the shunt resistance of the external fluid, $R_i$ is the longitudinal resistance of the axoplasm, and $R_m$ is the trans-membrane resistance under the cathode or the anode. Stimulation will occur when the trans-membrane potential at the cathode achieves a depolarizing threshold potential change $E_c$. From figure 2.2, $E_c = (I. R_m. R_O)/ (R_i+ R_O+2 R_m)$. Several important results are evident. Stimulation of nerves with external electrodes is possible only if a longitudinal intracellular current $I_i$ is caused to flow in the axon. This means the electrode orientation is critical. Second, the effectiveness of the stimulus is greatly affected by the shunt resistance $R_O$. Also, the effectiveness of a stimulus is nearly

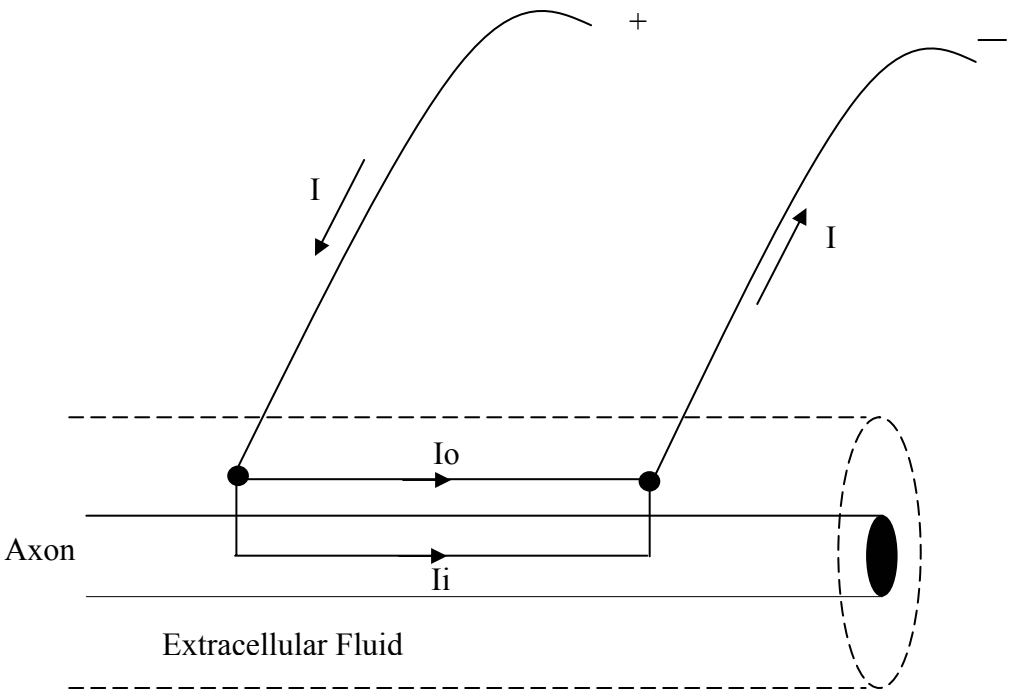



Figure 2.1: Simplified current flow between electrodes. After reference [15].

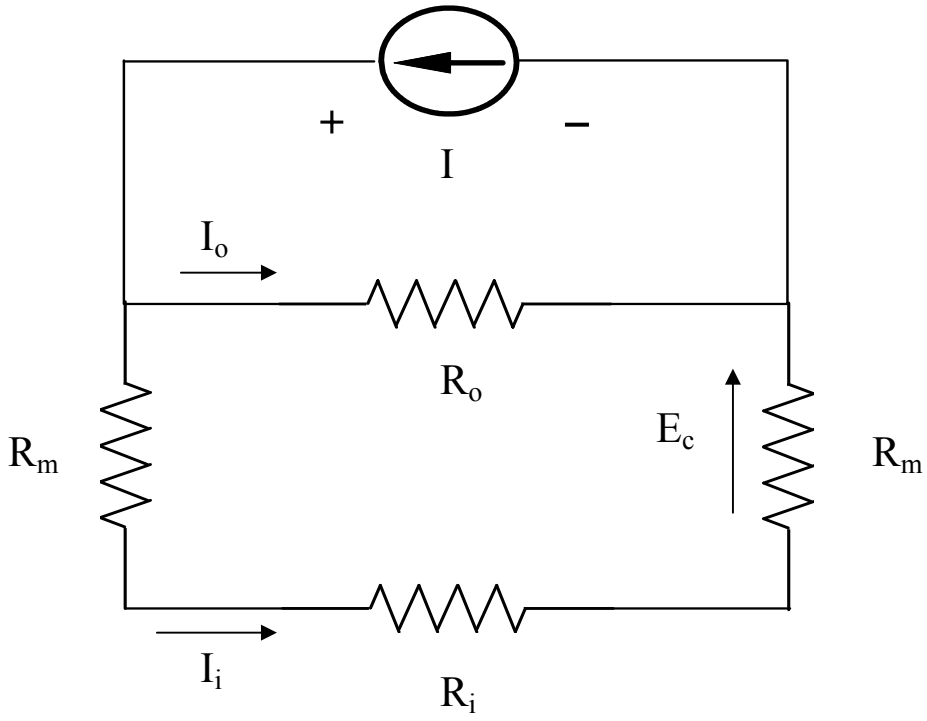



Figure 2.2: Equivalent circuit of Figure 2.1. After reference [15].

proportional to the stimulus current I. When time dependence effects such as capacitance are considered, the duration of a stimulus pulse also becomes important.

Table 2.1 shows approximate current magnitudes required for stimulation under various conditions. The actual values also depend on the pulse width and the fiber type to be stimulated.

Table 2.1: Current required for stimulation. After reference [15].

| | |
|---|---|
| intracellular | 1 nA – 10 nA |
| grease gap, sucrose gap | 0.01 μA – 1 μA |
| suction electrode | 10 μA – 1 mA |
| monopolar with small cathode pushed amongst the fibres | 50 μA – 1 mA |
| bipolar stimulation under paraffin oil | 50 μA – 2 mA |
| bipolar stimulation in volume conductor (saline or tissue ) | 1 mA – 20 mA |
| transcutaneous stimulation | 2 mA – 20 mA |
| field stimulation | 50 mA – 500 mA |

The strength duration curve for excitation is shown in figure 2.3. The curve indicates that the stimulus current and the duration of the pulse width can be mutually traded off over a certain range. Over this range, the product of current and duration, i.e. the amount of electric charge delivered, characterizes the effectiveness of a stimulus. For very short pulses, the relation breaks down because of the capacitance of the lead wires.

The relation also breaks down for long pulses, as the current approaches the nerve's minimum effective current value called the rheobase current.

However, over a range extending roughly from 50 μs to 1 ms, changes in duration have a similar effect to changes in current. For example, if the maximum current for a particular stimulator is just too small to evoke a particular response, an increase in the pulse time may well be effective [15].

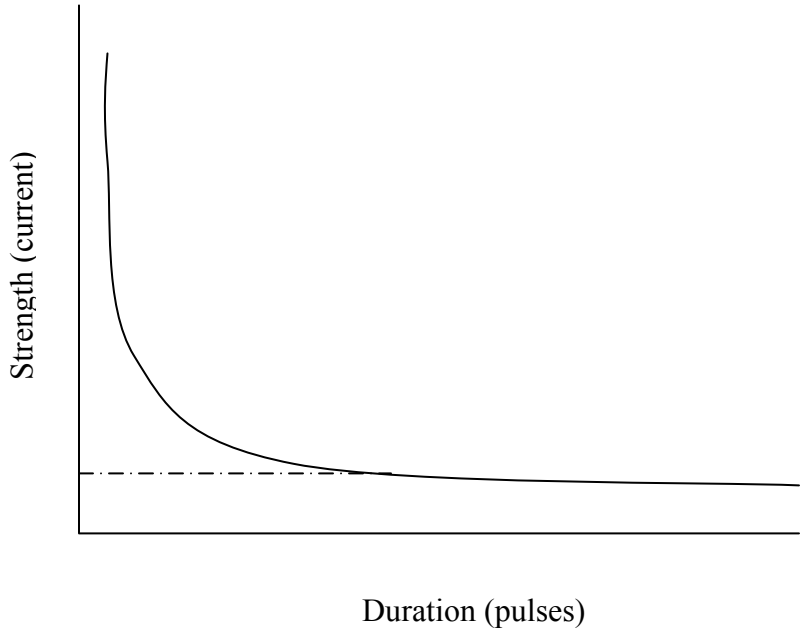



Figure 2.3: Strength duration curve for stimulation (dashed line indicates minimum effective current for stimulation). After reference [15].

**2.2 Power in Implantable Devices**

Power can be supplied to implantable devices either by an external power source or by integrating internal batteries into the implanted device. With an external power source, for wireless transmission, the implanted device may lose power when the transmitting antenna moves away from the receiver. This can cause an interruption in the receiver output. This restricts the mobility of the patient. There also may be intervening heating of

the body tissues by the transmitted RF power, which depends on the RF frequency and power. In the case when power is supplied by a wired source, the latter must be worn continuously by the patient and this has its own disadvantages. It has low cosmetic acceptance and its effectiveness depends on patient compliance. Also with electrodes penetrating into the skin from outside is a source of infection. These and other disadvantages associated with external power sources make an implantable device with batteries integrated into the system an attractive alternative. Rechargeable batteries are preferable as they do not require surgery for battery replacement.

High reliability and high energy density are the most important requirements for batteries in implantable systems. They should be hermetically sealed and should have no gaseous discharge. Nickel cadmium, nickel metal hydride and lithium ion are the most commonly used rechargeable batteries for implantable medical devices. Table 2.2 shows the technical specifications for three different types of rechargeable batteries. Nickel cadmium is the most commonly used rechargeable battery because of its superior life cycle. Lithium ion and nickel metal hydride are also used with implantable medical devices due to their higher specific energy (watt-hours per kilogram) and energy density (watt-hours per liter).

Lithium iodine batteries are exclusively used by modern pacemakers. Lithium side is oxidized while iodine side is reduced within the cell making lithium the battery anode and iodine the battery cathode. As the battery is used, its internal impedance increases. The state of the battery can be monitored by the battery discharge curve and the internal resistance data given by the battery manufacturer. These curves are a plot of battery capacity (mAhr) versus battery voltage at a given battery current. Given a specific

battery current, which is a function of the operating conditions of the device; one can calculate the longevity of the battery for a given cut-off value for the battery voltage. An increase in current drain I will increase the discharge rate and hence decrease the discharge time T for the battery as T = C/I where I = battery current and, C is battery capacity. Clearly lower current requirement for the circuit is desirable.

Table 2.2: Technical specifications for three different types of rechargeable batteries.

| Specifications | Nickel Cadmium | Nickel metal hydride | Lithium ion |
|---|---|---|---|
| Specific energy (watt –hour/kg) | 30 | 50 | 80 |
| Energy density (watt-hour/liter) | 100 | 180 | 200 |
| Cycle life (number of charges) | 1,500 | 500 | 300 - 500 |
| Nominal cell voltage | 1.25 V | 1.25 V | 3.7 V |

Batteries in implantable devices cannot be replaced easily. This makes reliability an important factor for an implantable battery. From the point the battery is integrated into the system, it is expected to power the device during final testing and throughout the useful life of the device. Currently, implanted batteries are required to power the device from five to eight years, with a minimal drop in the output voltage and without any undesirable effects such as swelling due to gas generation.

There is growing demand for smaller implantable devices. Hence, the integrated batteries must be as small as possible. Either in a cardiac pacemaker which takes up about

20 m1 of space or in an implantable defibrillator which takes up a space of 60-80 ml, half of the occupied space is consumed by the internal battery. Therefore, the energy density (energy/volume) and specific energy (energy/mass) are important considerations for implantable batteries [16].

Implantable device shapes are usually circular or elliptical to avoid having sharp corners that might penetrate internal organs or the skin or damage surrounding tissues. Therefore, the batteries are often approximated to a semicircle to conform to the overall device geometry. Generally the battery itself is hermetically sealed inside the device with the metal case, usually stainless steel, constituting one of the electrodes.

Different types of implantable devices may have radically different power requirements. Devices with low power consumption and those with infrequent high power usage can utilize batteries internal to the implantable device itself. For example, a cardiac pacemaker uses half of its battery power for cardiac stimulation and the other for housekeeping tasks such as monitoring and data logging. None of these tasks require high power. Therefore, a 1 amp-hour battery built using lithium iodine technology provides nominally five years of operation in addition to approximately six months of shelf life. Compared with lead batteries, the same volume of lithium battery provides eight times as much electricity, at one-thirtieth of the weight.

Implantable defibrillators, on the other hand, are capable of providing electrical shocks six orders of magnitude larger than a pacemaker's pulses, but are needed and used much less frequently. Since the battery alone cannot produce the shock pulse all at once, energy is drained from the battery for a period of about 20 seconds and stored in an internal capacitor before being delivered to the heart. During the capacitor charging

period, an implantable defibrillator drains 1-2 A current, which can be supplied by lithium silver vanadium oxide batteries.

Lithium ion rechargeable batteries have the highest energy density among the commercially available batteries. In addition, they have the lowest rate of self-discharge. Nevertheless, due to the relatively higher cost in comparison with nickel cadmium batteries, penetration of lithium ion rechargeable batteries into the consumer market has been slow. However with the necessary emphasis on size and function, the implantable medical device industry may provide an ideal forum for the use of lithium ion batteries.

There are many exciting frontiers for implantable devices and the batteries that power them. Advances made in rechargeable battery technology should permit development of hybrid implantable devices powered by internal rechargeable batteries. Advances in lithium, polymer and thin-film batteries, the latter with their high energy densities, make them potential candidates to power implantable devices in the future [17].

# 3. CIRCUITRY FOR STIMULATION

Though the overall energy need of analog devices is high, they draw a predictable and steady current from the batteries. Digital devices on the other hand load the battery with short and high current bursts. The overall energy requirement of a digital device is less but increases the peak current during load pulses. Hence the battery must be capable of delivering high current pulses that are often several times that of the battery's rating. Digital devices hence place a special demand on the battery causing seemingly good batteries fail on digital equipment [18]. The design engineer needs to select a battery that meets the special demands of the device for the maximum length of time. Also, critical judgment regarding size, cost, and weight of the battery must be made. Considering the wide variety of battery chemistries, the choices often are difficult to make [19].

With the increase in number of transistors in an integrated circuit and in frequency of operation, power consumption is a major concern for VLSI designers. Battery life in portable devices is greatly reduced by high power consumption. Therefore, there is a growing emphasis on low power design for battery-powered devices. The goal is to extend the battery lifetime while meeting the performance requirement. An effective method for low power design is to reduce the supply voltage while retaining the circuit performance by a combination of architectural and circuit optimization techniques [20].

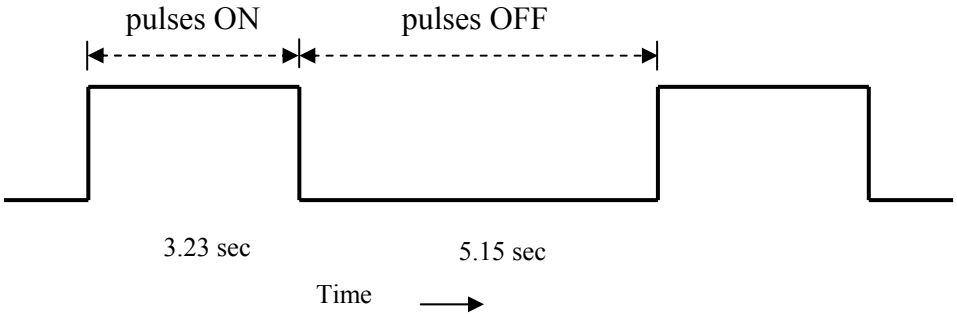
This chapter deals with design, layout and simulation results of a battery powered stimulation source. Section 3.1 discusses the general operation of the stimulator system and gives its specifications. This section also includes the specifications of battery used for the present application. The subsequent sections discuss in detail the designs, layouts and simulation results of the main components of the signal conditioning IC.

### 3.1 Design of Stimulator System

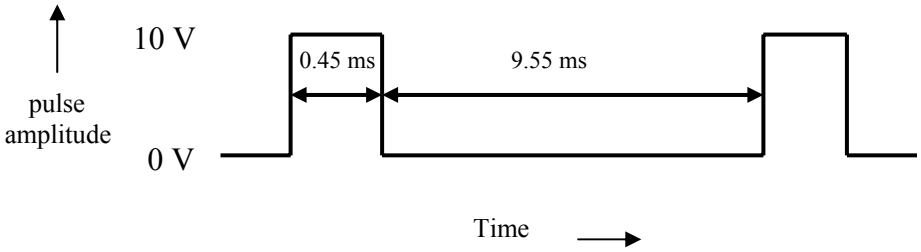
The stimulator source should deliver current pulses of up to 15 mA amplitude at a constant voltage of 10 V to the nerves or muscle tissues. Figure 3.1 shows a representative output from the stimulator. For the case considered, stimulation is provided by bursts of current pulses with an ON time of 3.23 sec and an OFF time of 5.15 sec corresponding to a duty cycle of 38.5 % as indicated in figure 3.1 a). During the pulse burst ON time of 3.23 sec, the pulses are ON for a period of 0.45 ms and OFF for 9.55 ms with a duty cycle of 4.5 % as depicted in figure 3.1 b). There are 323 pulses in the 3.23 sec pulse ON time indicated in figure 3.1 a). The stimulation pulses are of dual polarity and are alternatively applied to the two electrodes. This causes a net zero current flow in the medium. Zero net current flow may prevent the build-up of ion concentrations beneath electrodes. Polar concentration has been known to cause adverse skin reactions in animals [5].

The energy delivered during each pulse cycle of 10 ms in figure 3.1 b) is given by: Energy = 15 mA × 10 V × 0.45 ms = 67.5 μJ. Electrodes therefore deliver up to 67.5 μJ of energy during the ON period of 0.45 ms. The energy requirement from the battery for one stimulation burst cycle is 21.8 mJ every 8.38 sec or an average of 2.6 mW.

As discussed above, the power delivered during the pulse ON time of the cycle of 0.45 ms in figure 3.1 b) is 150 mW. As will be discussed in section 3.2.3.2, this power is drained from the battery for a period of 9.55 ms and stored in an storage capacitor C before being delivered to the electrodes for the next 0.45 ms. To meet such a high power requirement, the design uses capacitors external to the IC chip. For lower amount of power requirement, the system can be fully integrated with on-chip capacitors.




a) Availability of pulses as a function of time: Pulse burst ON/OFF frequency = 0.11 Hz.




b) Pulses during the ON time period shown in a) above: Pulse burst ON/OFF frequency = 100 Hz.

Figure 3.1: Representative output from the stimulator system.

Figure 3.2 gives an overview of the complete block diagram of the remotely powered stimulator system BESS developed here. It consists of a signal conditioning IC chip, a battery charging IC chip, an antenna and a rectifier. Two rechargeable lithium ion batteries are included as power sources. One battery provides the power to circuitry while the second battery serves as a back up as the first battery is being discharged. The second battery is also charged during this period. The charging requirement for the batteries is 100 mA current at 4.2 V for 2.5 hrs. The specifications of the battery are given in Table 3.1. The datasheet of the rechargeable battery is included in Appendix A [21].

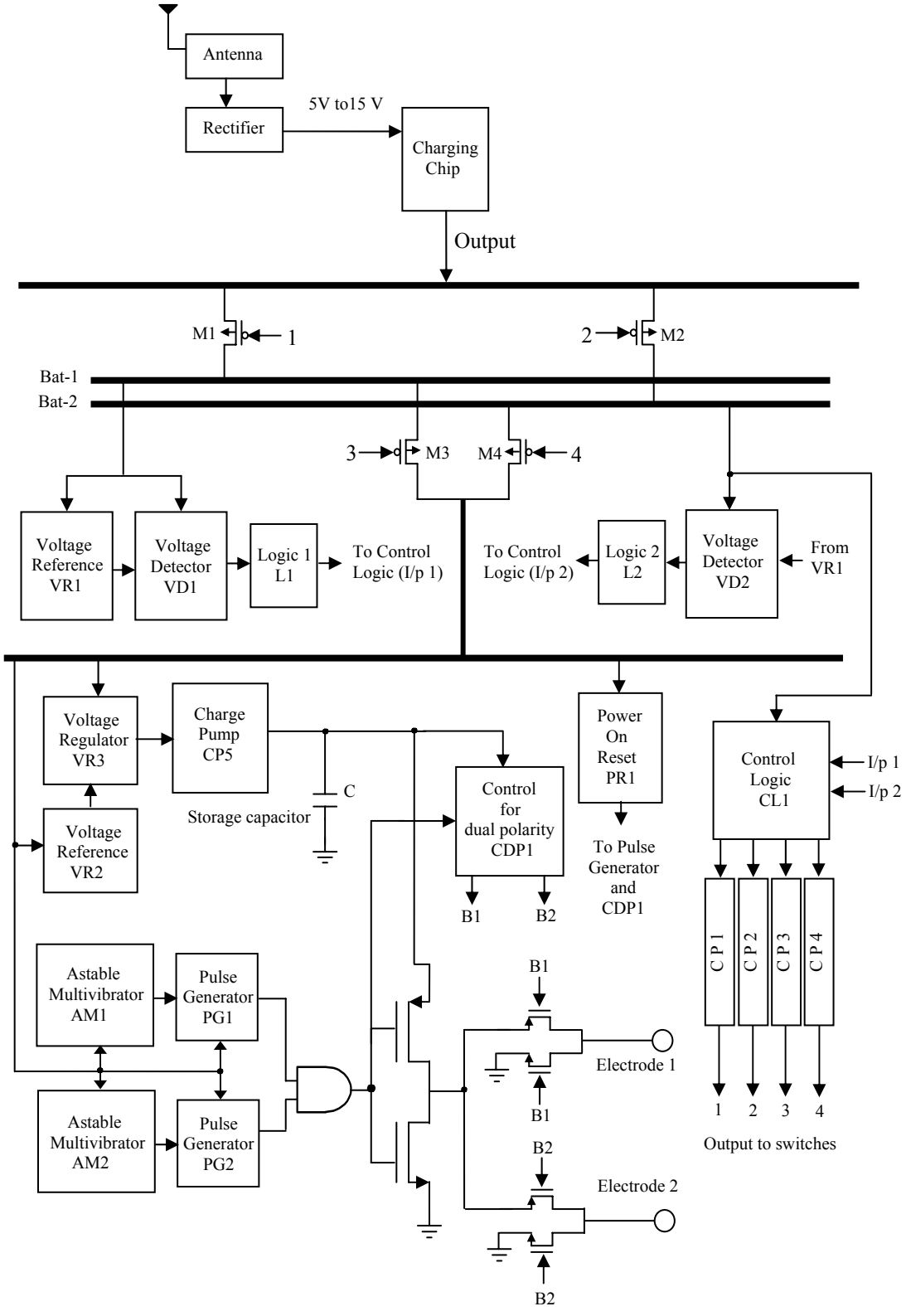



Figure 3.2: Overview of the remotely powered stimulator system (BESS).

The antenna, which is an inductive coil, couples power through wireless electro-magnetic coupling from an externally wearable power source. This power is utilized by the battery charging chip for charging the batteries. The power requirement is approximately 500 mW. The battery charging chip is included as a hybrid component.

Table 3.1: Specifications of the rechargeable batteries.

| **Property** | **Specification** |
|---|---|
| Type | Li-ion polymer rechargeable battery UBC005 |
| Operating Voltage | 4.20 V to 3.0 V |
| Nominal Capacity | 200 mAh |
| Energy | 0.7 Wh |
| Weight | 4.5 grams |
| Cycle life | > 300 cycles |
| Charging requirements | 100 mA at 4.2 V for 2.5 hrs |

The charging chip used here is a simple voltage regulator, which maintains a constant output voltage of 4.2 V and delivers a maximum charging current of 100 mA. Figure 3.3 shows the block diagram of the charging chip MIC79059, a product from Micrel semiconductor. The MIC79059 is a high accuracy, linear battery charging circuit designed for implementation as a simple single lithium-ion battery charger. It has a minimal number of external components, which makes it suitable for the present application. The datasheet of the charging chip is included in Appendix B [22]. An overview of the connection of the charging chip with the signal conditioning IC is shown in figure 3.4. As shown in the figure, two rechargeable batteries take turn to power the IC. The charging of the batteries is controlled by a control logic circuitry within the IC.

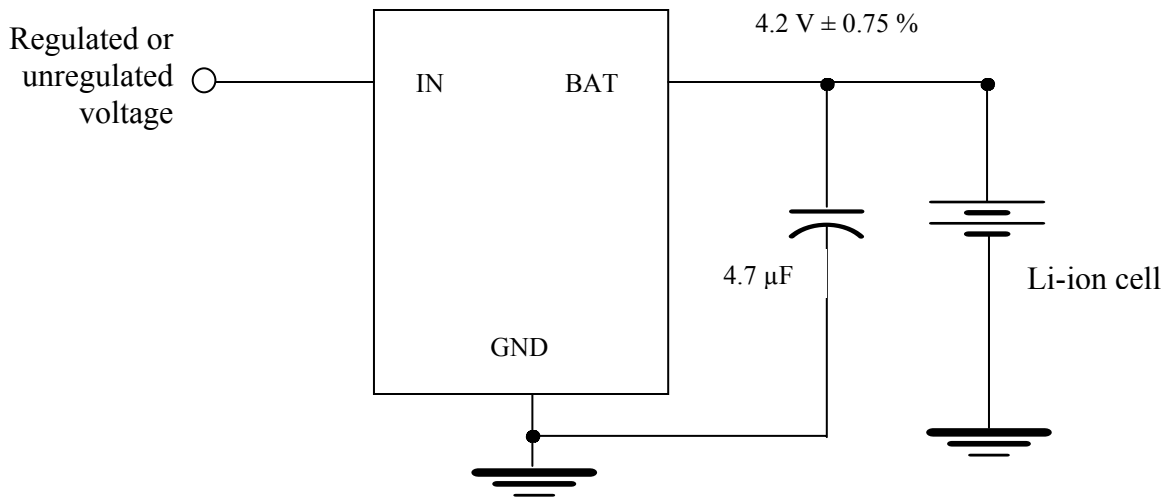



Figure 3.3: Block diagram of the charging chip MIC79059.

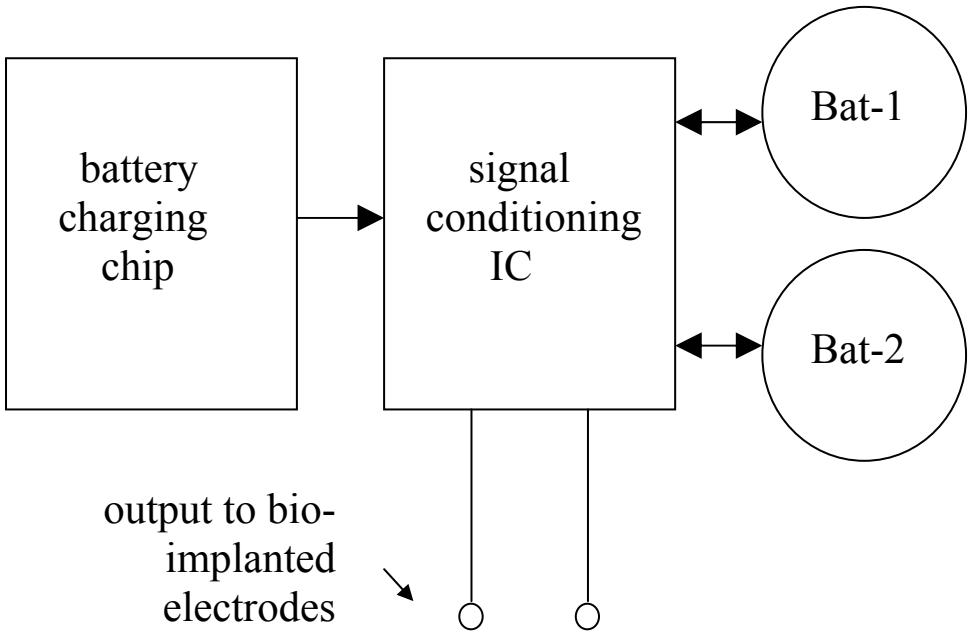



Figure 3.4: Overview of the connection of the charging chip with the signal conditioning IC.

The IC further includes a protection circuitry to prevent the batteries from over-charging, under-charging and over-discharging.

In the most basic charging technique, charge terminates as soon as the prescribed voltage level is reached. This charging technique is quicker and simpler but is inefficient as it can only charge the battery to 70 % capacity level. Li-ion battery chargers are generally comprised of a two-stage constant current/constant voltage system. The basic algorithm is to charge at a constant current until the battery reaches 4.2 V, and hold the voltage at 4.2 volts until the charge current has dropped to 10 % its initial value. Figure 3.5 gives the plot of battery voltage and charging current with time. The charge

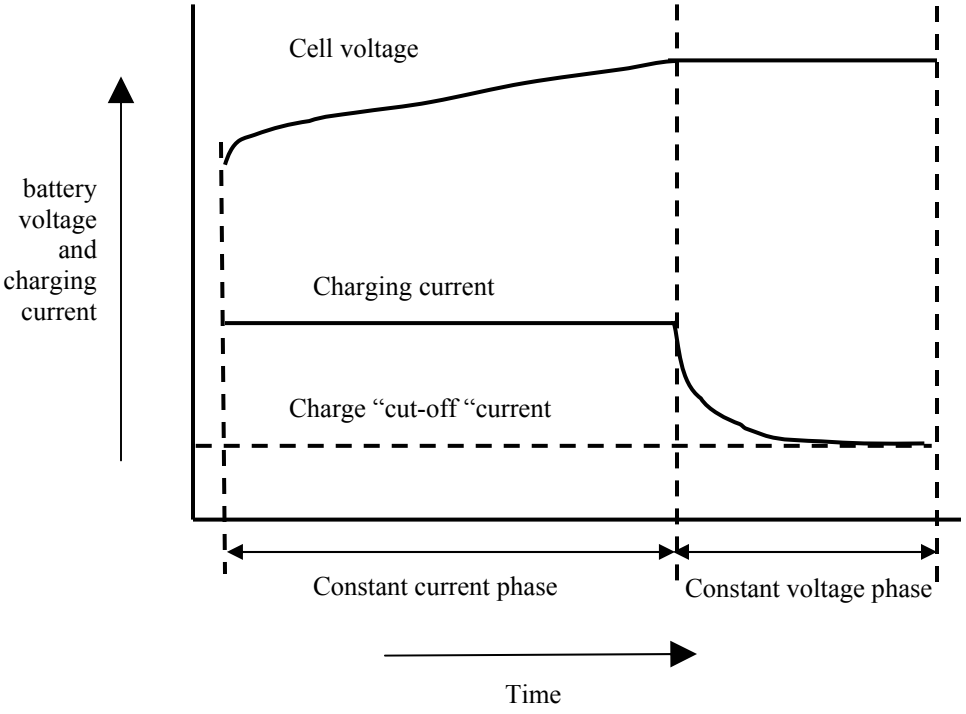



Figure 3.5: Plot of battery voltage and charging current with time.

time of the Li-ion battery is about 2.5 hours and the battery remains cool during charge Increasing the magnitude of charge current on a Li-ion battery charger does not shorten

the charge time by much. Although the voltage peak is reached quicker with high current, the topping off charge at constant voltage will take longer. The charge termination condition can be either with an internal timer or a drop in the charge current to 10 % [23]. In the present work as the battery takes 2.5 hrs to recharge, the external transmitter should be worn for a slightly longer period of approximately 3 hrs. Since the battery is charged with a regulated voltage of 4.2 V, it cannot be over-charged even though the transmitter is worn for an extended period of time.

The signal conditioning IC has two voltage detector circuits, each of which senses the change in the battery voltage and sends its output to the corresponding control logic circuit. Voltage detector compares the voltage to a reference value and reverses its output voltage if the input voltage falls below 3.05 V or exceeds 4.2 V. The control logic circuit analyzes this output from the voltage detector and decides on the state of the battery. If the voltage of the battery supplying power Bat-1 falls below 3.05 V, which is slightly above the battery cut off voltage, switch M1 is closed and switch M3 is opened in figure 3.2. At the same time switch M2 is opened and switch M4 is closed thereby connecting Bat-2 to supply power to the chip. By discharging the batteries to a voltage slightly above the battery cut off voltage of 3 V, the lifetime of the batteries is improved [24]. During recharging, switch M3 (or M4) is kept open so that the charging takes place essentially under no load conditions. This improves the charging efficiency of the batteries. Similarly, if the voltage of the battery goes above 4.2 V during recharging then the switch M1 (or M2) is opened preventing the battery from overcharging.

As seen in figure 3.2, the output of the voltage detector (VD1 or VD2) passes through logic circuit (L1 or L2) before going to the control logic circuit (CL1). This is to

prevent voltage detectors from misinterpreting the charging voltage of 4.2 V during recharging as the final battery voltage and thereby terminating the constant voltage charging cycle. This would otherwise lead to an incorrect control of the switches. The logic block (L1 or L2) has a D flip-flop and a simple logic circuitry to ensure that improper switching does not take place during the charging of the batteries. The four outputs of the control logic (CL1) go through four charge pumps before controlling the switches. This is because a voltage higher than the supply voltage is required to properly control the switches. There are two pulse generator circuits (PG1 and PG2), which generate pulses at a duty cycle of 38.5 % and 4.5 % respectively. An astable multivibrator circuit (AM1 or AM2) gives the input clocks to these pulse generators. The output of the two pulse generator circuits are then sent through an AND gate so that during the ON time of the pulse generator with 38.5 % duty cycle we have pulses with 4.5 % duty cycle.

A voltage regulator (VR3) maintains a constant voltage of 2.8 V for a change in the battery voltage from 4.2 V to 3.0 V. This constant voltage of 2.8 V then powers a series of cascaded charge pumps (CP5), which boost the voltage to the required output voltage of 10 V. The charge pump should have the capability of charging a storage capacitor to 10 V. This storage capacitor then has to deliver up to 15 mA of current to the electrodes at almost a constant voltage. Design value for the storage capacitor can be obtained as follows: Energy delivered per pulse = 67.5 μJ = $\frac{1}{2} \times C \times (V_i^2 - V_f^2)$. Here C is the storage capacitor, $V_i$ is the initial capacitor voltage and $V_f$ is the final capacitor voltage. For $V_i$ = 10 V and $V_f$ = 9 V, the value of the capacitor can be determined as 7.1 μF. Because of other losses in the system, the actual value of C should be larger than 7.1 μF. A larger capacitor will reduce the drop in the capacitor output voltage to less than 1

V. But this will increase the size of the capacitors used in charge pump circuits as they have to charge a larger capacitor to 10 V. This will increase the system size.

The output from the charge pump and the pulse generator go to an inverter, which then generates 10 V pulses at the required frequency. The output of the inverter goes to a pair of electrodes. There is also a control circuit for dual polarity stimulation (CDP1). The control circuit ensures that the electrodes are stimulated alternatively so that there is no polarization effect at the electrode tips.

The next subsections discuss in detail the designs, layouts and simulation results of the main components in the signal conditioning IC. The design of the IC can be divided into three main parts. Part 1 includes the main logic for controlling the operation of the batteries; Part 2 consists of the pulse generator circuit which generates the stimulations pulses with the required frequency and Part 3 consists of a charge pump to boost the voltage to 10 V and then charge a storage capacitor which can deliver up to 15 mA of pulse current with only a small drop in the pulse voltage.

### 3.1.1 Part 1: Design of Control Circuitry for Battery Recharging

Part 1 includes two voltage detector circuits (VD1 and VD2), a voltage reference circuit (VR1), two logic blocks (L1 and L2), a control logic block (CL1), four charge pumps (CP1-CP4) and four switches (M1, M2, M3 and M4) as shown in figure 3.2. The design, layouts and simulation results of these components are discussed below.

#### 3.1.1.1 Design of Voltage Reference Circuit

Voltage reference circuit (VR1) in figure 3.2 provides a precise output voltage value, independent of the supply voltage value. The output voltage of the voltage reference is then compared to other voltages in the system. Its purpose is to provide a voltage

reference for the system for comparison purposes under large changes in supply voltage and temperature values. Voltage reference circuits are similar to voltage regulators in how they function, but unlike regulators, which are used to deliver power to a load, voltage references are normally used with no load to preserve their precise values.

The voltage reference circuit designed here is based on threshold voltage referenced biasing scheme [25]. Figure 3.6 gives the functional circuit diagram of the voltage reference circuit. The aspect ratio $\left(\frac{W}{L}\right)$ with values of channel width W and channel length L in μm is indicated next to each transistor. The operation of the circuit is as follows: MOSFET's M3 and M4 force the same current I to flow through M1 and M2. The gate source voltage $V_{gs1}$ of M1 is equal to I×R1. Neglecting the output resistance of the MOSFET's and the body effect, $I \times R1 = Vgs1 = Vthn + \sqrt{\frac{2I}{\beta 1}}$ where $\beta_1$ and $V_{thn}$ are the conductance parameter and threshold voltage of transistor M1 respectively. The conductance parameter $\beta_1 = \mu_c \times C_{ox'} \times \left(\frac{W}{L}\right)$ where $\mu_c$ is the channel mobility and $C_{ox'}$ is the gate oxide capacitance per unit area. If $\beta_1$ is made large by choosing a high aspect ratio for M1, the current I can be approximated by $I \cong \frac{Vthn}{R1}$. Practical values of $V_{gs1}$ are 1.0 to 1.2 V. The circuit operates on the principle that by choosing a high aspect ratio for transistor M1 and a large value for resistor R1, the gate source voltage $V_{gs1}$ and hence the current I can be made almost constant with respect to changes in the supply voltage. The constant current I can then be used to get an accurate voltage reference. The accuracy of the current I, is also limited by the threshold voltage accuracy, which may vary by 20

percent. This constant current I is mirrored using transistor M6. The drop across resistor R2 is taken as the reference voltage. By varying the aspect ratio of the transistor M6 or by varying the resistance R2, the desired reference voltages can be obtained.

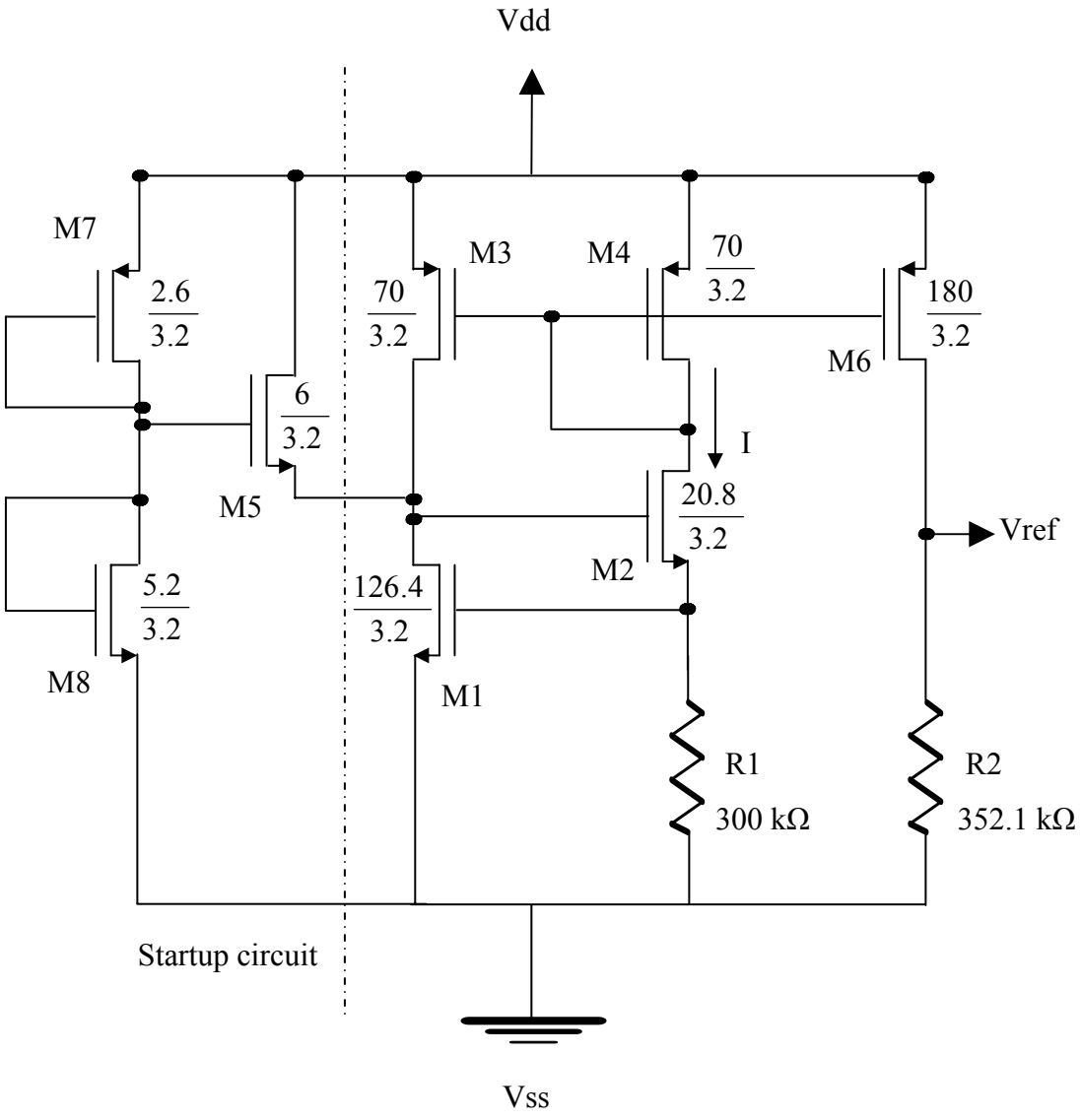



Figure 3.6: Functional circuit diagram of the voltage reference circuit (VR1). Transistor aspect ratios are shown in μm.

Since this is a self biased circuit there is a possibility that the current I is zero. This happens when the gates of M3 and M4 are at Vdd and the gate of M2 is at Vss. To prevent this, a start up circuit is employed as shown in figure 3.6. If the gate of M2 is

close to Vss, then M5 turns on and pulls the voltage at the node high enough for M2 to conduct resulting in equal but non-zero currents in M1 and M2.The gate of M5 is at 2.6 V due to voltage divider M7 and M8.

Voltage reference circuit in the present application is required for both voltage detectors (VD1 and VD2) and the voltage regulator (VR3) circuit. Each requires a different value of voltage reference. In order to have flexibility, the resistance R2 in figure 3.6 is externally connected in this design. Depending on the required voltage reference, the value of the resistance R2 can be changed. The value of resistance R1 should be chosen as high as possible so that the current I is small and hence essentially remain constant. The value of the resistance R1 is chosen as 300 kΩ and this causes a variation of 0.09 μA in current I for a change in the supply voltage Vdd from 3 V to 4.2 V. Figure 3.7 shows the layout of the voltage reference circuit in L-EDIT and figure 3.8 gives the simulation results. The simulations were done with a resistance R2 of 352.1 kΩ. The supply voltage is varied from 3 to 4.2 V over some finite interval of time. As seen in the simulation results, the reference voltage is a constant 1.87 V.

**3.1.1.2 Design of Voltage Detector Circuit**

Voltage detector (VD1 or VD2) senses battery supply voltage and reverses its output voltage if the input sense voltage falls below or exceeds a set voltage. The voltage detection level set in this design is different for the case when the power supply voltage changes from a low to a high value than when it changes from a high to a low value. In other words, the detection voltage level differs with the direction of change of the input voltage. The high detection voltage is called $V_{det+}$ and the lower detection voltage is called $V_{det}$-. The difference between $V_{det+}$ and $V_{det}$- is the hysteresis width. The voltage

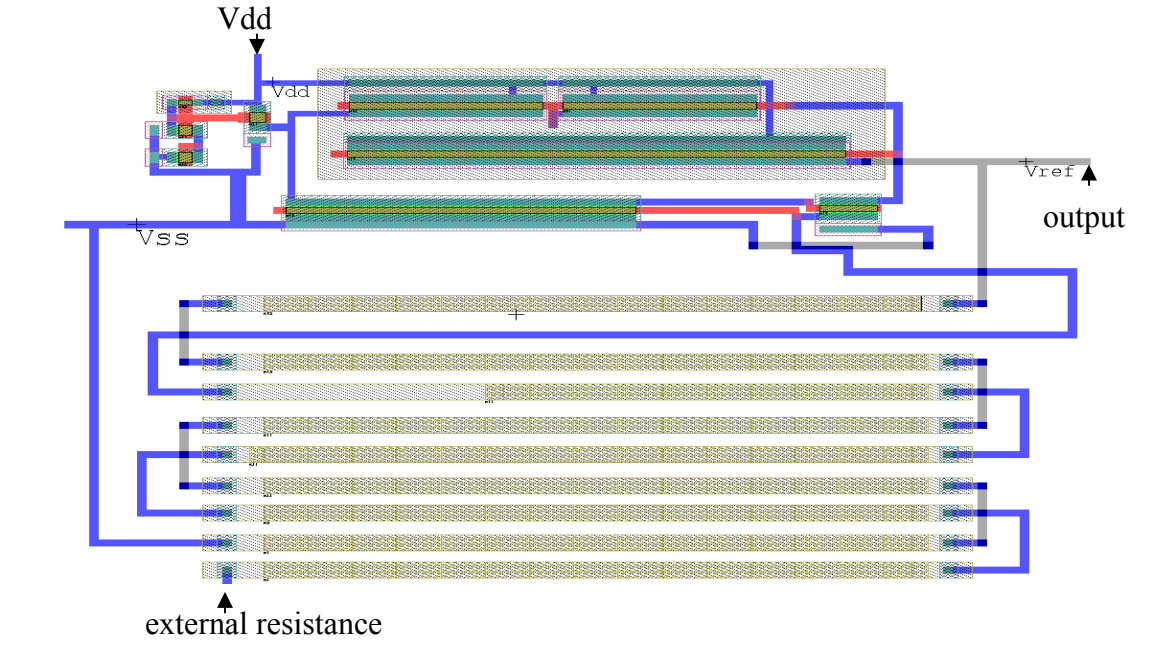



Figure 3.7: Layout of the voltage reference circuit (VR1) in L-EDIT.

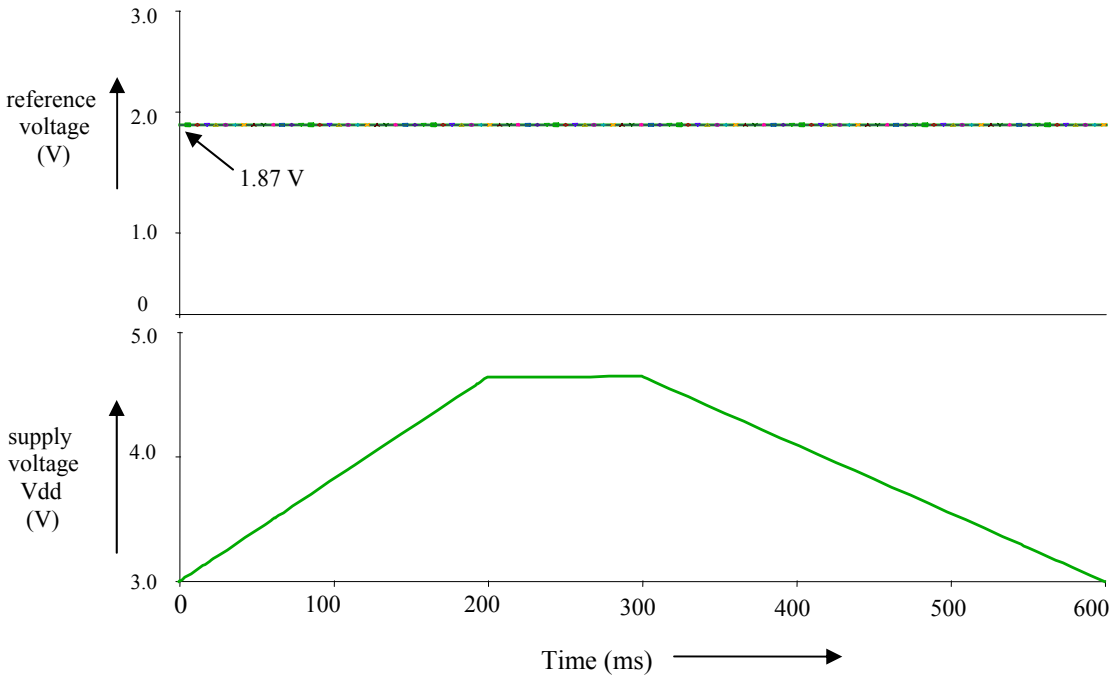



Figure 3.8: Simulated output of the voltage reference circuit (VR1) as a function of variation in power supply voltage Vdd for R2 = 352.1 kΩ.

detector can be used in a battery charging circuit to detect over-charge or over-discharge of battery being charged [26].

A CMOS voltage detector circuit is shown in figure 3.9. The circuit consists of a reference voltage circuit, a voltage divider circuit comprising of resistors R1, R2 and Rh, hysteresis transistor M1, operational amplifier circuit and a CMOS output circuit (M2 and M3). The design of the operational amplifier is discussed in Appendix C. The circuit compares the R1, R2 and Rh divison voltage at point X1 with Vref, and reverses the output voltage if the input voltage reaches the detection voltage. The difference in the detection level for the case when the power supply voltage changes from a low to a high value and when it changes from a high to a low value is due to the presence of the hysteresis transistor M1. When the power supply Vdd is above the lower detection voltage $V_{det}$-, the output voltage Vout is high and hence the transistor M1 is off. The lower detection voltage $V_{det}$- of the voltage detector during incursion from a high to low voltage can therefore be expressed by $V_{\det -} = \frac{R1 + R2 + Rh}{R2 + Rh} \times Vref$ . When Vdd falls below $V_{det}$-, Vout changes from high to low. Similarly when the power supply Vdd is below the high detection voltage $V_{det+}$, the output voltage Vout is low and hence the transistor M1 is on. The higher detection voltage $V_{det+}$ of the voltage detector during incursion from a low to high voltage can therefore be expressed by $V_{\det +} = \frac{R1 + R2}{R2} \times Vref$ . When Vdd rises above $V_{det+}$, Vout changes from low to high. $V_{det}$- and $V_{det+}$ can be adjusted by the ratio of resistances R1, R2 and Rh.

In the present application the voltage detector has to detect the battery voltage when it falls below 3.05 V or when it rises above 4.2 V. The voltage reference circuit

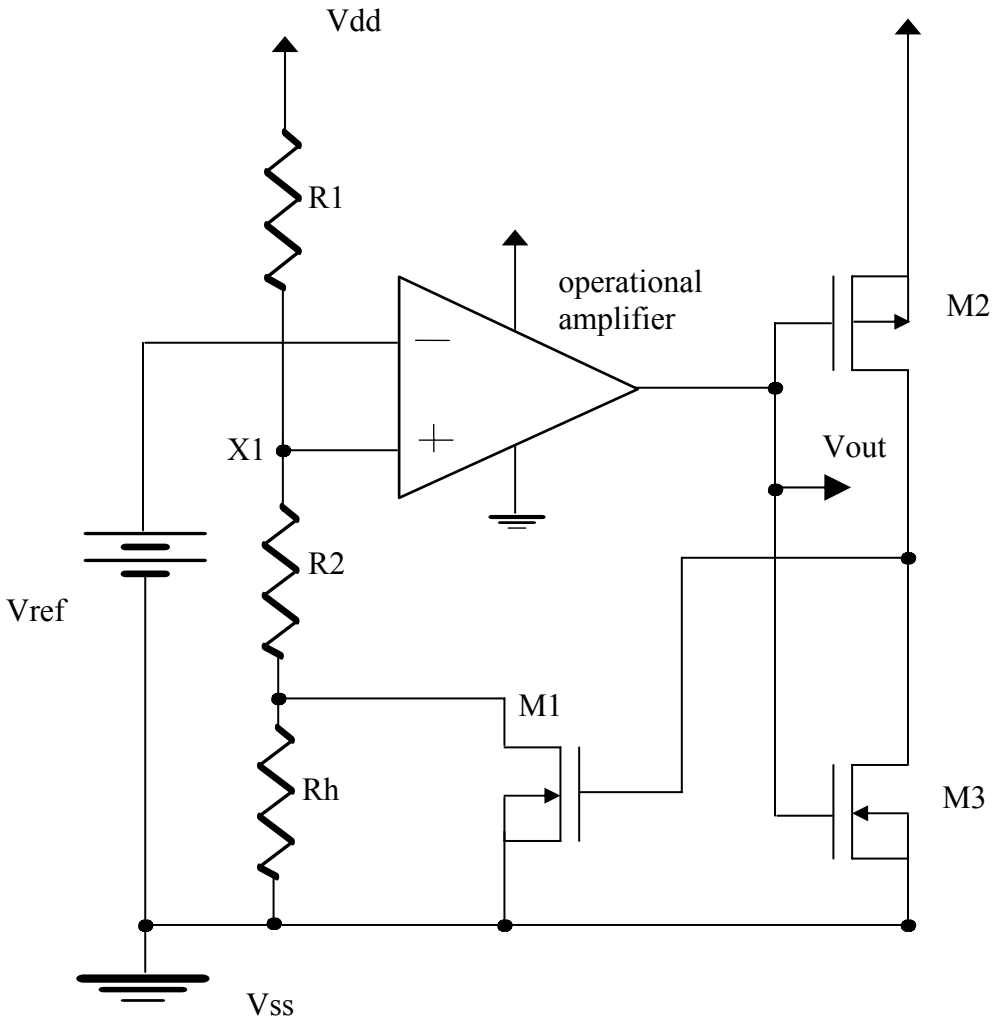



Figure 3.9: Functional circuit diagram of the CMOS voltage detector circuit (VD1 or VD2).

gives a constant reference voltage of 1.75 V. Therefore using the above equations for $V_{det-}$ and $V_{det+}$ we choose the values of R1, R2 and Rh as 18.48 kΩ, 13.2 kΩ and 12 kΩ respectively.

Figure 3.10 shows the layout of the voltage detector circuit in L-EDIT and figure 3.11 shows the simulated output of the voltage detector over some finite interval of time. As seen from the simulated results, the detector output goes high when input voltage goes above 4.2 V and output goes low when input voltage goes below 3.05 V.

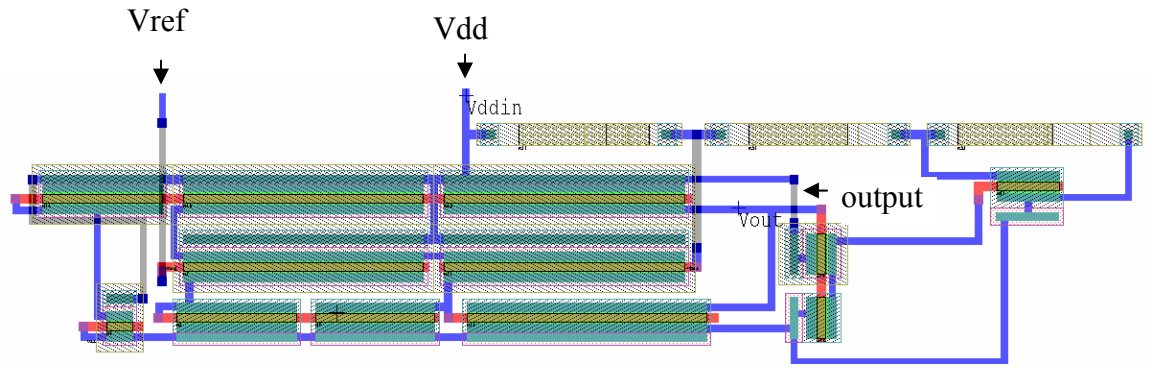



Figure 3.10: Layout of the CMOS voltage detector circuit (VD1 or VD2) in L-EDIT.

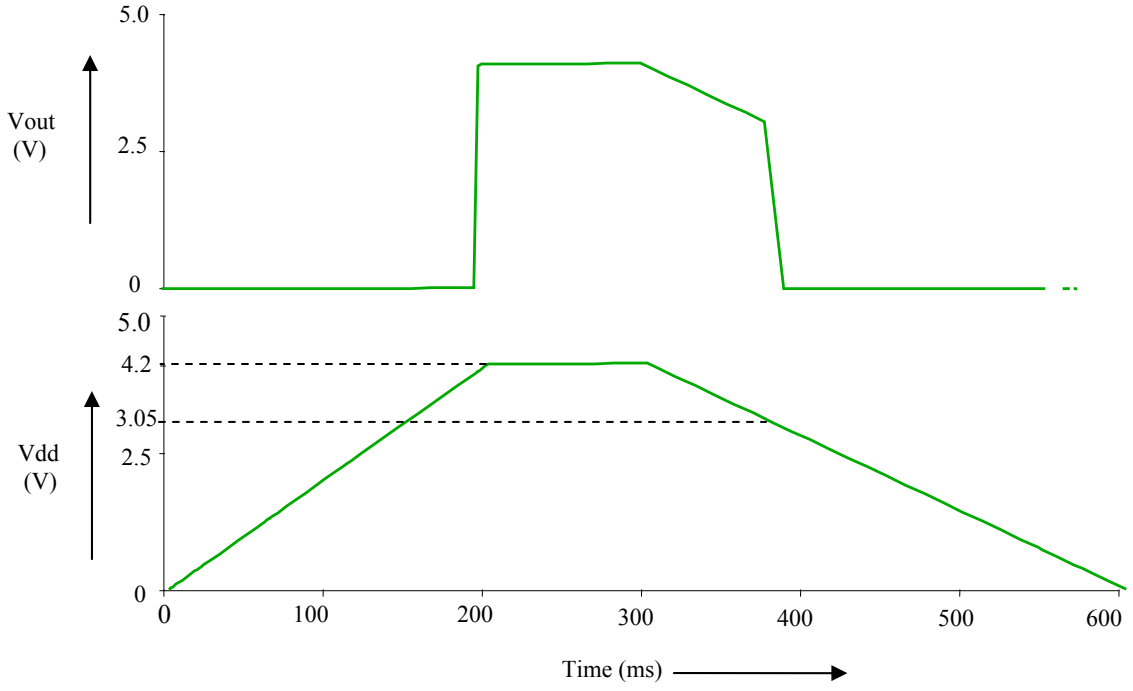



Figure 3.11: Simulated output of the CMOS voltage detector circuit (VD1 or VD2) as a function of the input voltage Vdd.

### 3.1.1.3 Design of Charge Pump Circuit

Charge pumps are circuits that generate a voltage larger than the supply voltage from which they operate. They are a convenient choice for battery operated systems where declining value of voltage from a discharging battery may not be acceptable or where optimal number of batteries cannot be included in series because of lack of space or other considerations. Charge pumps use capacitors to store and transfer charge. Capacitive voltage boost is achieved by switching a capacitor periodically. The switching can be done either by diodes or transistors.

Efficient charge pumps are required in analog circuitry to augment internal voltage supplies. This greatly simplifies the circuit design and increases the dynamic range of operation. The efficiency can be increased by using large capacitors but this is not feasible in integrated circuits where chip area is a major constraint. In the present design, good power efficiency is obtained by choosing higher clock frequencies and small size capacitors [27]. Figure 3.12 shows functional circuit diagram of a single stage charge pump. The operation of the circuit is as follows: During the first half cycle of the input clock when CLK = VDD and CLKNEG = 0, M0 and M3 are turned on, M1 and M2 are off. As a result C1, is charged to the input voltage and the node at C0 connected to M1 and M3 is raised to the previous voltage existing on it plus Vdd. During the second half cycle of the input clock when CLK = 0 and CLKNEG = Vdd, M0 and M3 are off, and M1 and M2 are turned on. As a result C1 is raised to the previous half cycle input voltage plus Vdd and this is transferred to the output. If the input voltage is equal to Vdd then the output voltage will be twice the input voltage. The voltage gain $\Delta V$ = (output voltage – input voltage) for input Vdd is approximated as:

$$\Delta V = Vdd \times \frac{C}{C + Cpar} - Rout \times Iout \quad (1)$$

and $$Rout = \frac{1}{f.C} + Rswitch \quad (2)$$

where C = C0 = C1, Cpar is the parasitic capacitance on the internal nodes of the stage, Rout is the charge pump equivalent resistance, Rswitch is the on-resistance of the transistor switches and f is the frequency of the input clock.

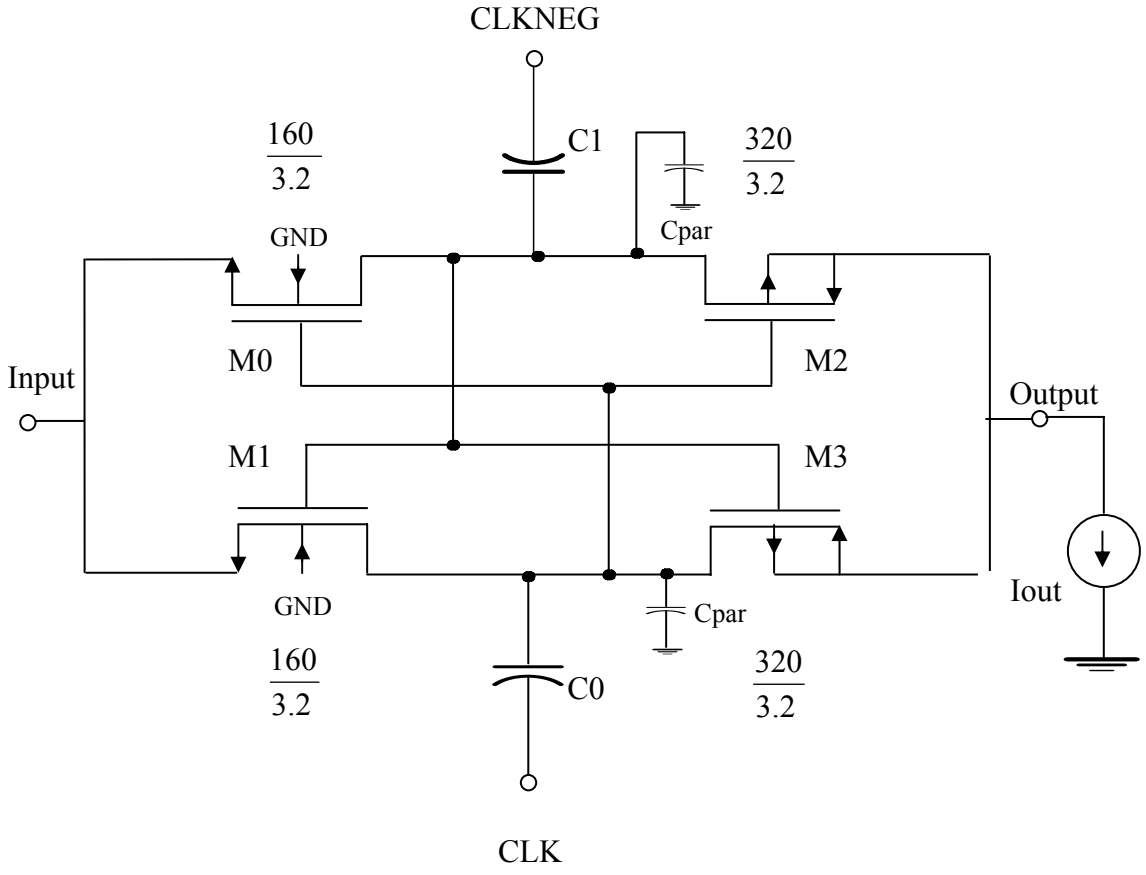



Figure 3.12: Functional circuit diagram of a single stage charge pump circuit (CP1 – CP4). Transistor aspect ratios are shown in μm.

Equation (1) shows that the charge pump equivalent resistance Rout should be small to increase the voltage gain ΔV. The resistance Rout can be decreased by either using a

higher clock frequency or by using large value capacitors or by decreasing the ON resistance of the switches. In the present design, the charge pumps (CP1 - CP4 in figure 3.2) use 4 pf capacitors for C0 and C1, a high clock frequency f of 5 MHz and a high aspect ratio for transistors M1, M2, M3 and M4 to decrease the ON resistance of the switches. Such high aspect ratio transistors are within the capability of the foundry where this IC will be fabricated. The output of the charge pump goes to the gate of a switch and therefore is hence essentially under no load condition (Iout = 0) eliminating the second term in equation (1). A gain ΔV of approximately equal to Vdd is hence obtained. Figure 3.13 shows the layout of a single stage charge pump and figure 3.14 gives the simulated results with a 3 V input voltage. The output voltage of the charge pump should ideally be double the input voltage but the simulation results show a value of 5.5 V, which is a slightly lower value. This is attributed to parasitic capacitances.

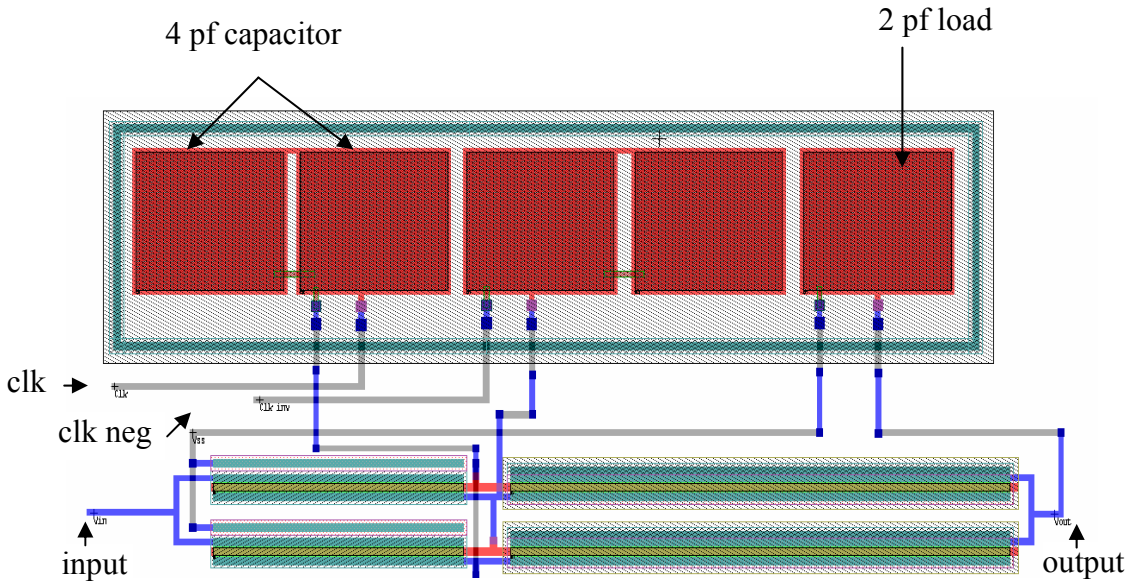



Figure 3.13: Layout of a single stage charge pump circuit (CP1 - CP4) with C = C0 = C1 = 4 pf in L-EDIT.

in L-EDIT.

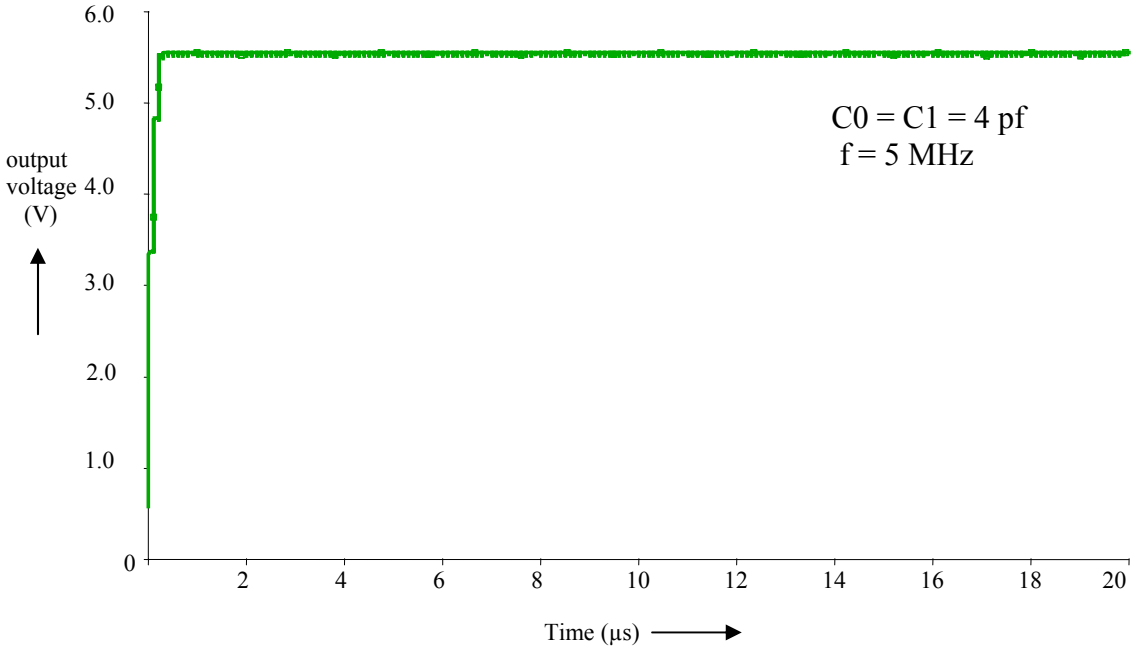



Figure 3.14: Simulated output of the single stage charge pump circuit (CP1 – CP4) with an input voltage of 3 V.

### 3.1.1.4 Design of Logic Block

The recharging of the lithium battery used in this work is done by passing a constant current of 100 mA at 4.2 V through the batteries. Under these conditions the lithium battery will take just over 2.5 hrs to recharge. The charging chip automatically adjusts for the charging cycle requirements described in figure 3.5. The voltage detector circuit (VD1 or VD2) is constantly connected to the recharging battery and changes its output whenever the battery voltage falls below 3.05 V or goes above 4.2 V. During recharging, the voltage detector may misinterpret the voltage of 4.2 V from the charging IC chip as the final battery voltage. The output of the voltage detector will go high as soon as the charging voltage is applied. The control logic block controls the switches depending on the voltage detector output. So when the detector output goes high, the control block will

improperly close the switch just as the charging has just begun. In order to prevent this, output of the voltage detector is applied to a logic block (L1 or L2) prior to being fed to the main control logic block (CL1). Figure 3.15 shows the functional circuit diagram of the logic block (L1 or L2) and figure 3.16 gives the layout of the logic block.

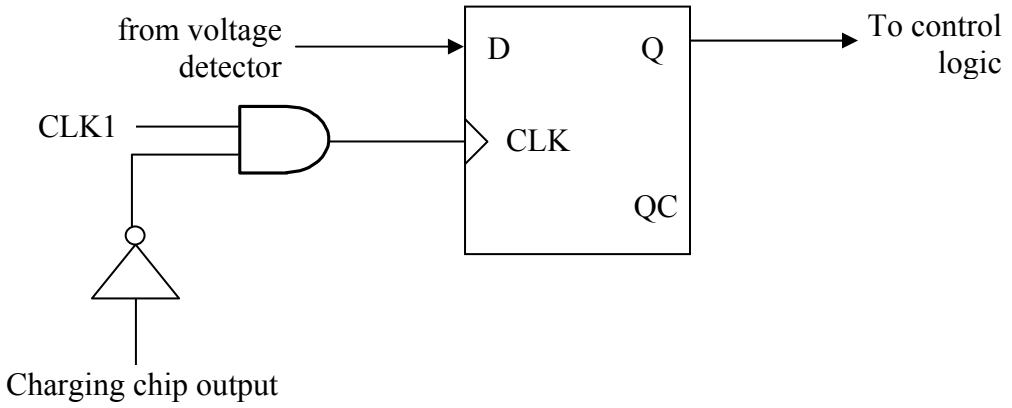



Figure 3.15: Functional circuit diagram of the logic block (L1or L2).

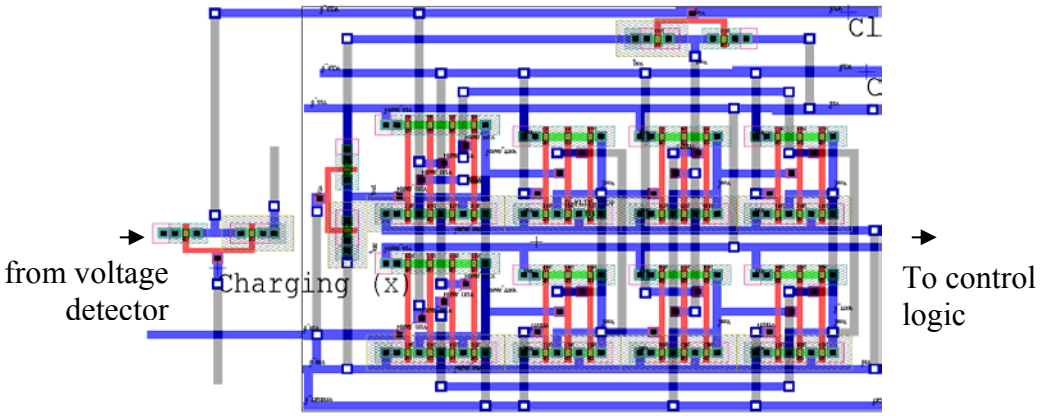



Figure 3.16: Layout of the logic block (L1 or L2) in L-EDIT.

The logic block is a simple D flip-flop and acts as a memory element. The clock CLK of the D flip-flop is controlled by a simple logic. Whenever the input is given to the

charging chip, the clock of the logic block goes to zero and it holds its previous value [28]. Any change in the output of the voltage detector will not get to the main control logic block when charging is being done. The clock CLK1 to the D flip flop can be given from either AM1 or AM2 astable multivibrator discussed later in section 3.2.2.1.

**3.1.1.5 Design of Control Logic Block**

As seen in figure 3.2, the function of the control logic block (CL1) is to control the four PMOS switches M1, M2, M3 and M4 depending on the outputs of the voltage detector circuits. The control logic block has four outputs 1, 2, 3 and 4 and they respectively go to the gates of the four PMOS transistors as shown in figure 3.2. The inputs to the control logic block are the two outputs from the voltage detector circuits (VD1 and VD2) through logic blocks (L1 and L2). Table 3.2 shows the truth table of the control logic block (CL1).

Table 3.2 Truth table for the control logic block (CL1).

| I/p 1 from L1 | I/p 2 from L2 | Switch outputs | | | | Battery Conditions |
|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | |
| 0 | 0 | 0 | 1 | 1 | 1 | Bat-1 charging<br>Bat-2 disconnected<br>(no pulses to electrodes) |
| 0 | 1 | 0 | 1 | 1 | 0 | Bat-1 charging<br>Bat-2 supply power |
| 1 | 0 | 1 | 0 | 0 | 1 | Bat-1 supply power<br>Bat-2 charging |
| 1 | 1 | 1 | 1 | 0 | 1 | Bat-1 supply power<br>Bat-2 disconnected |

If Bat-1 and Bat-2 are both discharged then Bat-1 is charged first. If both batteries are fully charged, then Bat-1 will first power the circuit. The operation of the control logic is as follows: If the Bat-1 needs recharging then output 1 goes low and output 3

goes high so that the transistor switch M1 closes and transistor switch M3 opens and the Bat-1 is charged. During this time Bat-2 supplies power to the circuit. Once Bat-1 is charged, the control logic block will connect Bat-1 to supply the power to the circuit leaving Bat-2 partially discharged. This is a drawback because the battery is not recharged until it is completely discharged. Also, the lifetime of the back-up battery (Bat-2) will be decreased slightly. Alternating the operation evenly between the batteries will increase the total lifetime of the implanted device. Figure 3.17 shows the functional circuit diagram of the control logic block and figure 3.18 gives the layout of the control logic block.

### 3.1.2 Part 2: Design of Pulse Generator Circuitry

Part 2 includes two astable multivibrator circuits (AM1 and AM2), two pulse conditioning circuits (PG1 and PG2) and a power on reset circuit (PR1). The design details, layouts and simulations of these components are described below.

#### 3.1.2.1 Design of Astable Multivibrator Circuit

Astable multivibrator circuits employ positive feedback which results in oscillations. Of the three types of multivibrators namely astable, bistable and monostable, the astable multivibrator is the simplest one and is commonly used as a clock. The astable multivibrator has no stable state and thus oscillates. Figure 3.19 gives the functional circuit diagram of an astable multivibrator circuit. In order to analyze the behavior of this multivibrator, delay time through the gates is neglected and it is assumed that the output voltage of gates change voltage levels instantaneously when the input voltage crosses the threshold level $V_T$. Because of the inverting action of the inverter INV2, V2 is the complement of V1. So that when $Vx = V_T$, inverter INV1 turns on, INV2 turns off, and

V2 goes from 0 V to Vdd. This change of voltage is coupled through C so that Vx changes from $V_T$ to $V_T$ + Vdd. Since the output V1 is at 0 V and V2 is at Vdd, C discharges through R towards 0 V.

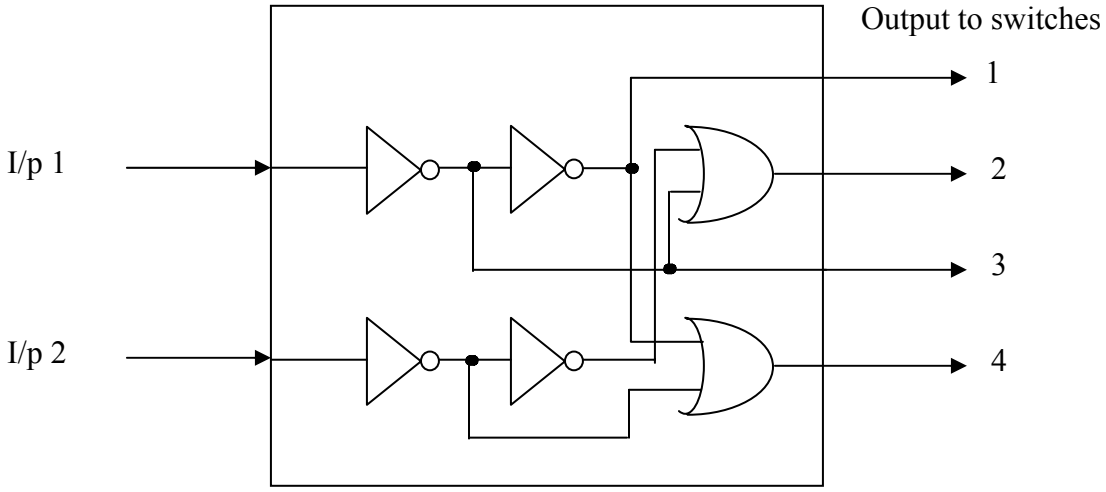



Figure 3.17: Functional circuit diagram of the control logic block (CL1).

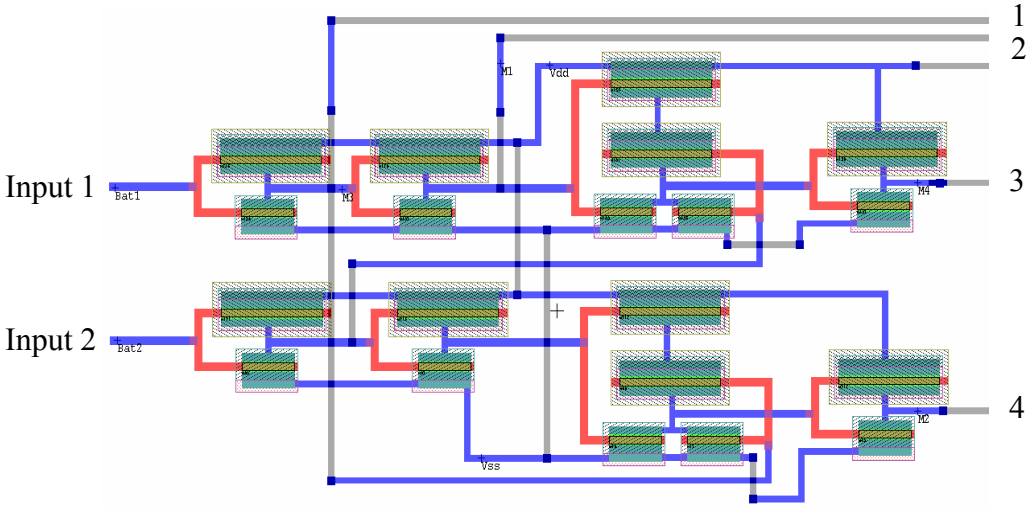



Figure 3.18: Layout of the control logic block (CL1) in L-EDIT.

But when Vx goes below $V_T$, INV1 turns off and INV2 turns on. That is, V1 goes to Vdd, and V2 goes to 0 V. The timing capacitor C now charges through R toward V1, which is at VDD; and when Vx crosses $V_T$, the whole cycle repeats itself. In this circuit there are no stable states, but the output voltages switch from one level to the other at a period determined by the passive components R and C and the threshold voltage $V_T$. With $V_T$ = Vdd/2, the output waveform is symmetrical and the frequency of oscillation is given by $f = \frac{1}{2.2\tau}$ where $\tau$ = RC [29].

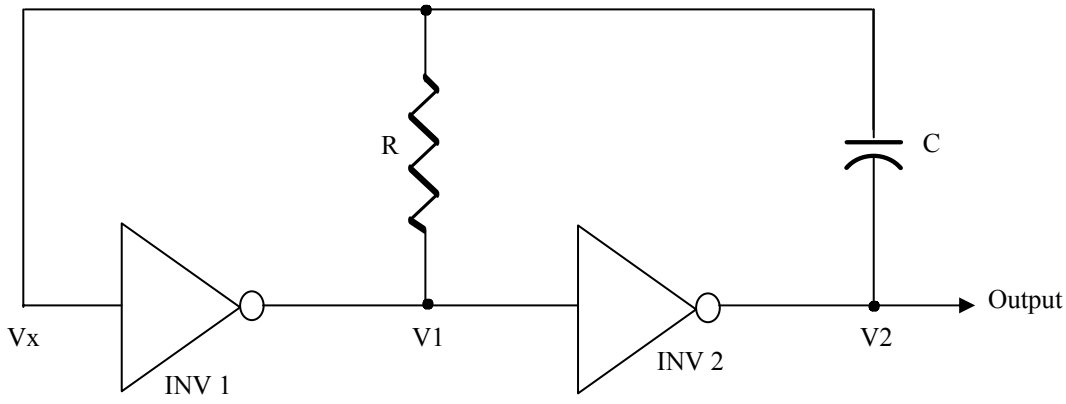



Figure 3.19: Functional circuit diagram of the astable multivibrator circuit (AM1 or AM2).

In order to get the stimulation pulses of the required duty cycle, two clocks are generated one with a pulse width of 0.21 ms and the other with a pulse width of 3.23 sec. The clock with a pulse width of 0.21 ms is the input to the pulse conditioning circuit (PG1). The output of PG1 is a series of pulses with an ON time of 0.45 ms and OFF time of 9.55 ms. Similarly the input to the pulse conditioning circuit (PG2) is the clock with a pulse width of 3.23 sec. The output of PG2 is a series of pulses with an ON time of 3.23 sec and OFF time of 5.15 sec. The resistors and the capacitors are externally connected so

as to give flexibility in the adjustment of pulse width. The resistor value was chosen as 200 kΩ and the capacitor values were determined. For the clock with pulse width of 0.21 ms, C = 0.95 nF and for the clock with the pulse width of 3.23 sec, C = 14.7 µF. Figure 3.20 shows the layout of the astable multivibrator circuit and figure 3.21 shows the simulated results with a resistance of 200 kΩ and a capacitor of 0.95 nF.

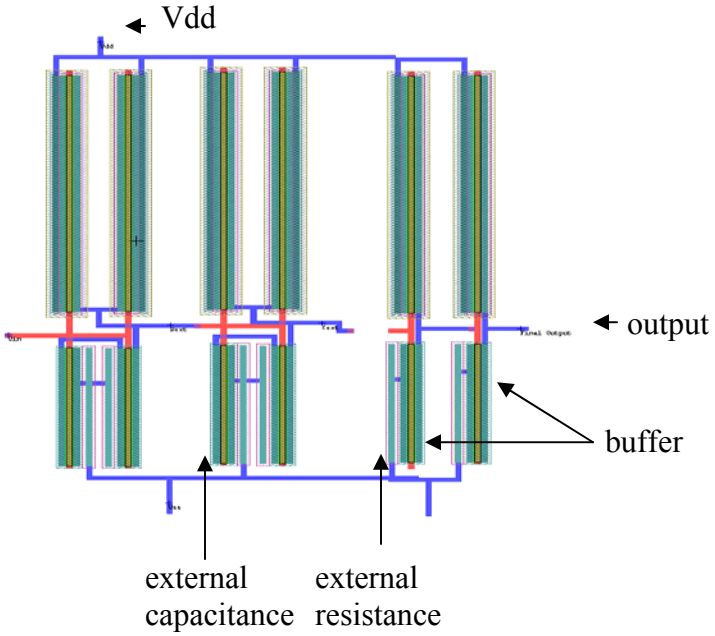



Figure 3.20: Layout of the astable multivibrator circuit (AM1 or AM2) in L-EDIT.

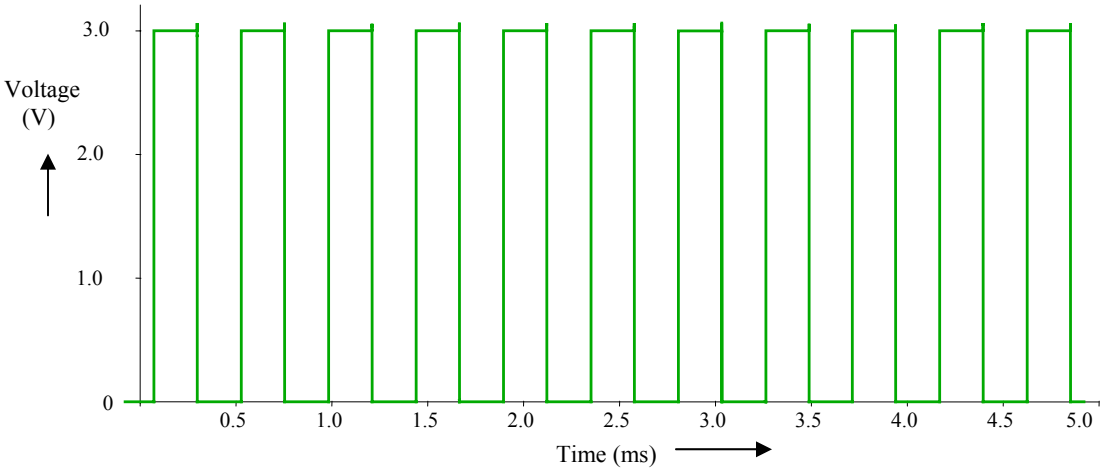



Figure 3.21: Simulated output of the astable multivibrator circuit (AM1) with C = 0.95 nF and R = 200 kΩ.

### 3.1.2.2 Design of Pulse Conditioning Circuit

The pacing parameters for stimulation are not symmetrical. The stimulation pulse bursts have a duty cycle of 38.5 % with pulse ON time of 3.23 sec and pulse OFF time of 5.15 sec. During the ON time of 3.23 sec, the pulses have a frequency of 100 Hz with a duty cycle of 4.5 % (ON time of 0.45 ms and OFF time of 9.55 ms). The pulse conditioning circuits (PG1 and PG2) receive symmetric input clocks from their respective astable multivibrator. The outputs of the pulse conditioning circuits are pulses with the required duty cycle. The pulse conditioning circuits consist of a series of JK flip-flops connected as circular shift register with the complement output of the last flip flop connected to the input of the first flip flop. This is the configuration of a Johnson counter. At each stage of the JK flip-flop in a Johnson counter there is an incremental delay. The total delay can be increased by increasing the number of stages. Using these delays, the selected outputs of the Johnson counter are passed through appropriate logic gates to get output pulses with the required duty cycle.

The pulse generator with an output with a duty cycle of 4.5 % uses a six stage Johnson counter and the outputs of the last three stages pass through four NAND gates, four inverters and a JK flip-flop to get the required output. Figure 3.22 gives the functional circuit diagram of pulse conditioning circuit (PG1). Figure 3.23 shows the layout and figure 3.24 gives the simulation results of the pulse generator with 4.5 % duty cycle. As seen from the simulation results the output pulse has a duty cycle of 4.27 % which is very close to the required duty cycle. Still finer adjustments need to be made to get the exact required duty cycle. Similarly the pulse generator with an output with duty cycle of 38.5 % uses two JK flip-flops, an inverter and an XOR gate to get the required

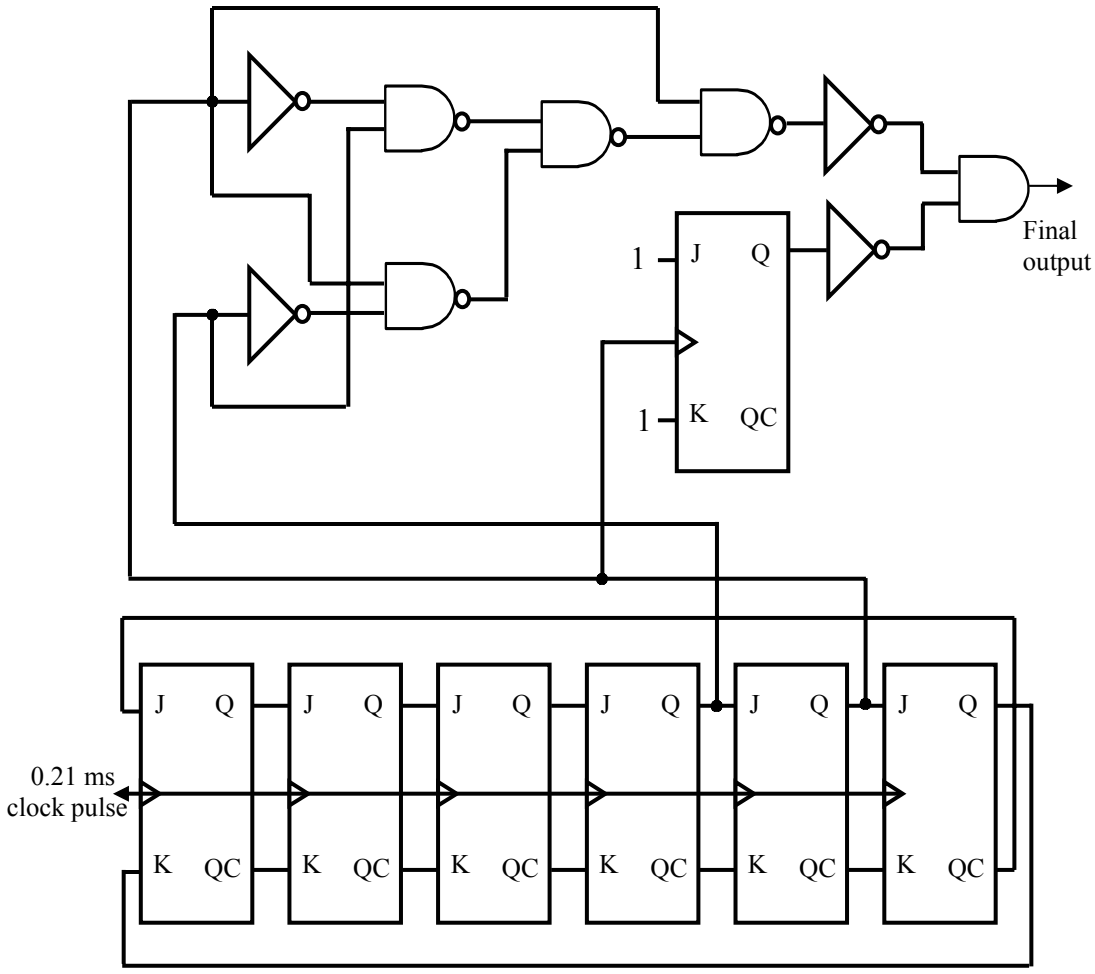



Figure 3.22: Functional circuit diagram of the pulse conditioning circuit (PG1).

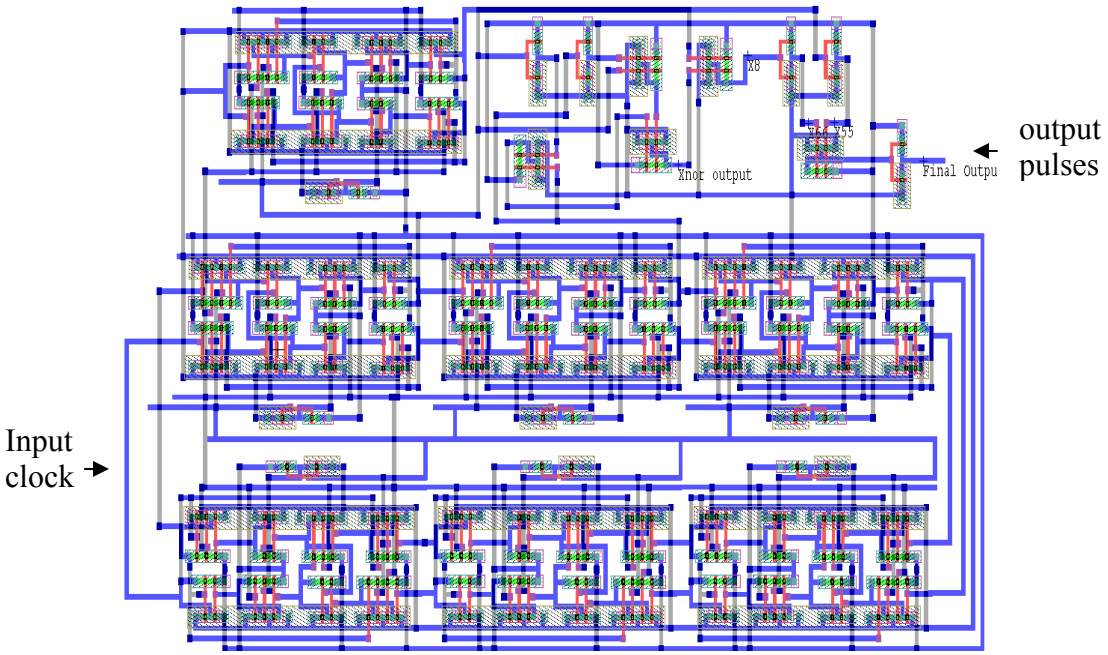



Figure 3.23: Layout of the pulse conditioning circuit (PG1) in L-EDIT.

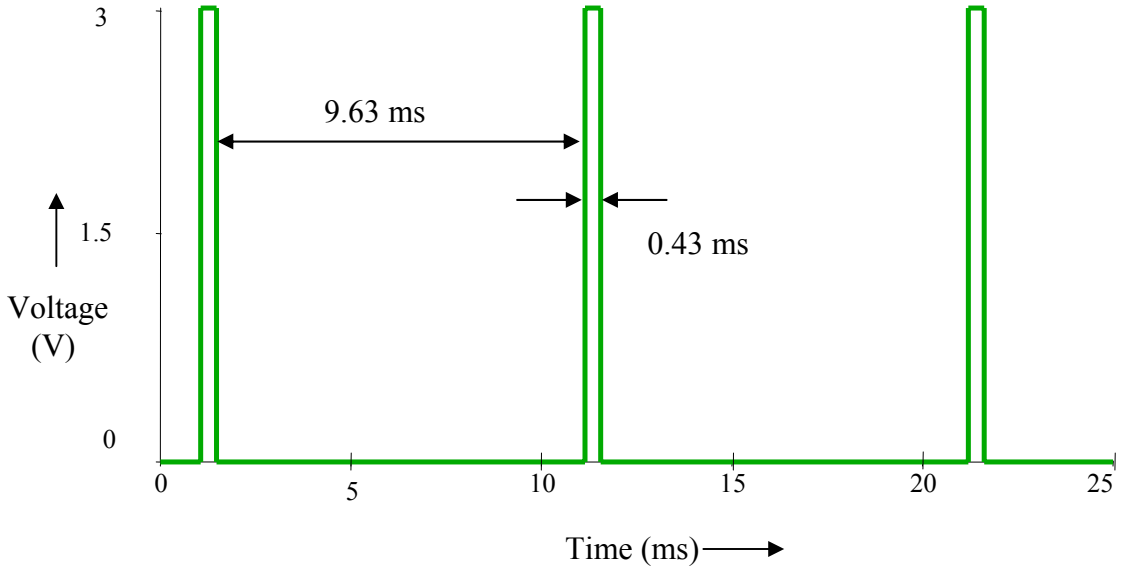



Figure 3.24: Simulated output of the pulse conditioning circuit (PG1).

output. This circuit is more efficient in generating pulses with 33 % duty cycle. Fine adjustments are made to get close to the required duty cycle of 38.5 %. Figure 3.25 gives the functional circuit diagram of pulse conditioning circuit PG2. Figure 3.26 shows the layout and figure 3.27 gives the simulation results of this pulse generator. As seen from the simulation results the output pulse has a duty cycle of 35.2 % which is close to the required duty cycle.

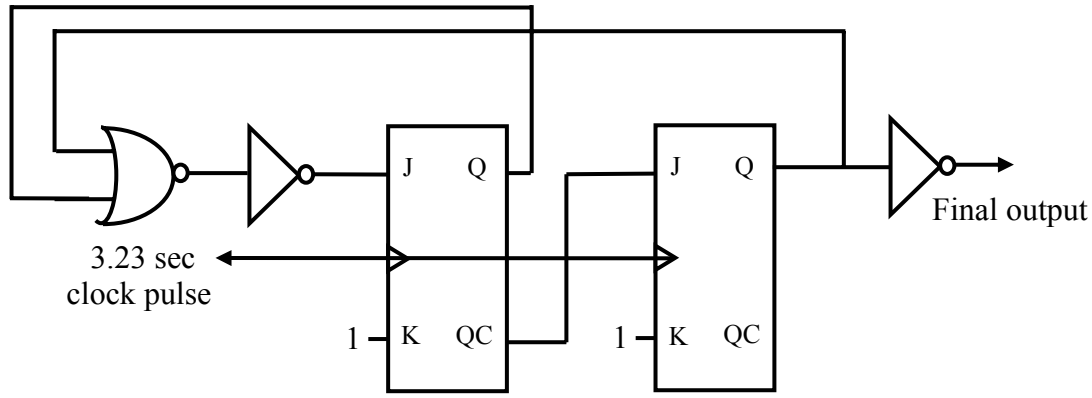



Figure 3.25: Functional circuit diagram of the pulse conditioning circuit (PG2).

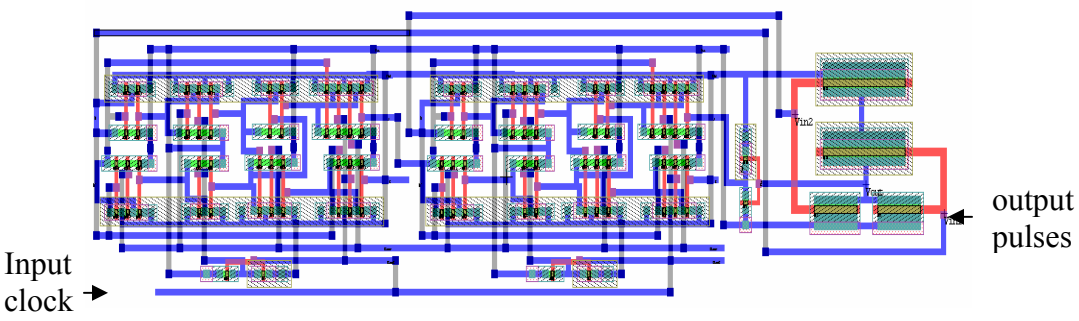



Figure 3.26: Layout of the pulse conditioning circuit (PG2) in L-EDIT.

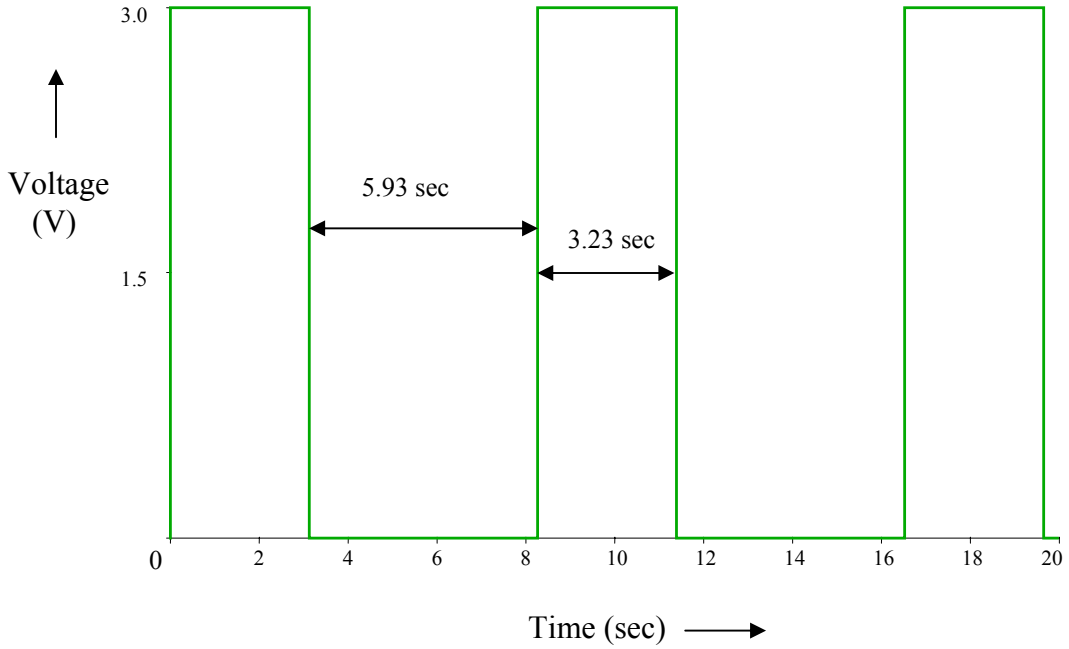



Figure 3.27: Simulated output of the pulse conditioning circuit (PG2).

### 3.1.2.3 Design of Power-On-Reset Circuit

The function of the power-on-reset circuit (PR1) is to initialize the pulse generator as soon as the power is applied. The circuit acts as a clear input to the pulse generator and initializes the output of the pulse generator to zero. It is important for the pulse generator to deliver the right output. As shown in figure 3.28, the power-on-reset circuit is composed of a high pass filter and a Schmitt trigger. The Schmitt trigger senses the input voltage and changes it output voltage if the input voltage falls below or exceeds a set voltage. Capacitor C1 and NMOS MN0, which is biased through MPbias and MNbias, form the high pass filter. Initially when the circuit is powered, capacitor C1 takes some time to get charged which depends on the capacitor value and the charging current. During this time the voltage at point X1 is above the set voltage and hence the output of the Schmitt trigger is high. As soon as the capacitor is charged and the voltage at point

X1 goes below the set voltage, the output of the Schmitt trigger goes low and stays there till the power supply remains connected. In other words, at the time of power-on, the output of the power-on-reset rises to the high state and stays there for short time, then returning to the low state when C1 is charged [30].

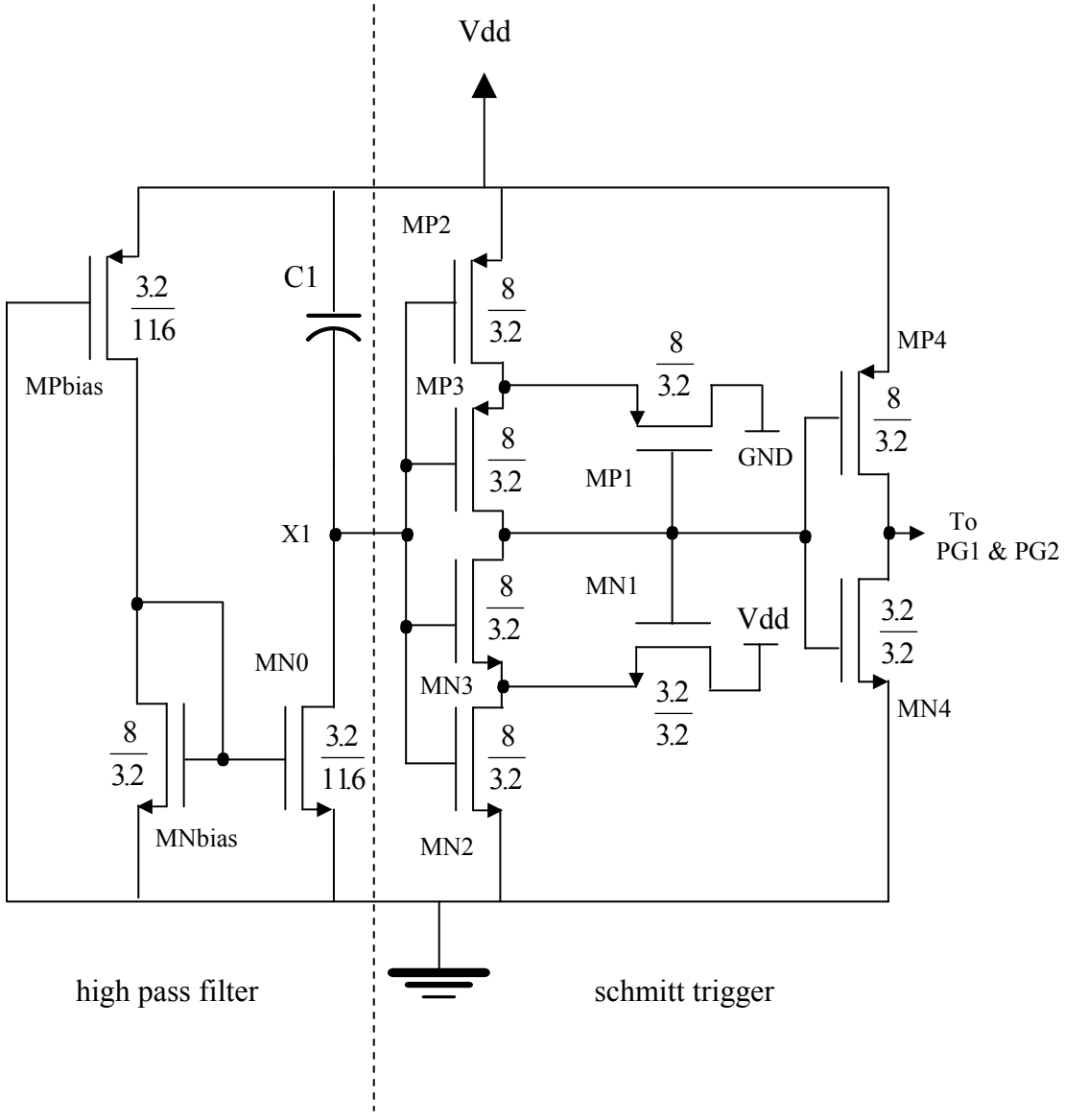



Figure 3.28: Functional circuit diagram of the power-on-reset circuit (PR1). Transistor aspect ratios are shown in μm.

The size C1 was chosen to be 8 pf to set the width of the high output voltage to about 90 µs. Figure 3.29 gives the layout and figure 3.30 gives the simulated result of the power-on-reset circuit.

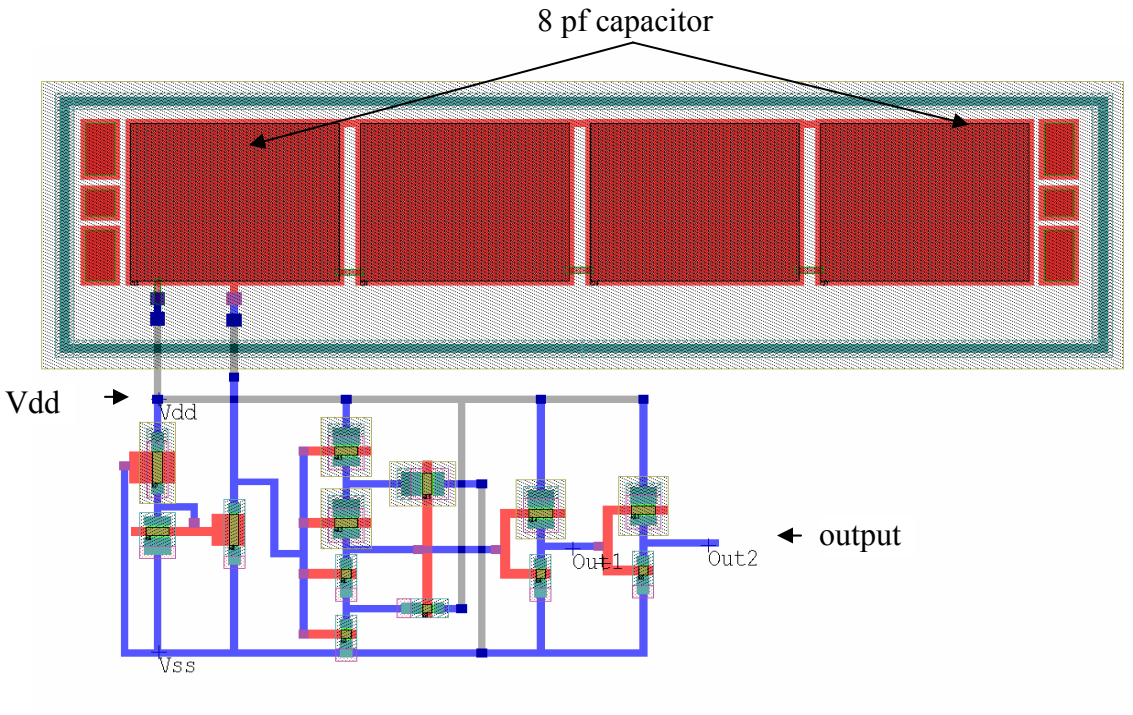



Figure 3.29: Layout of the power-on-reset circuit (PR1) in L-EDIT.

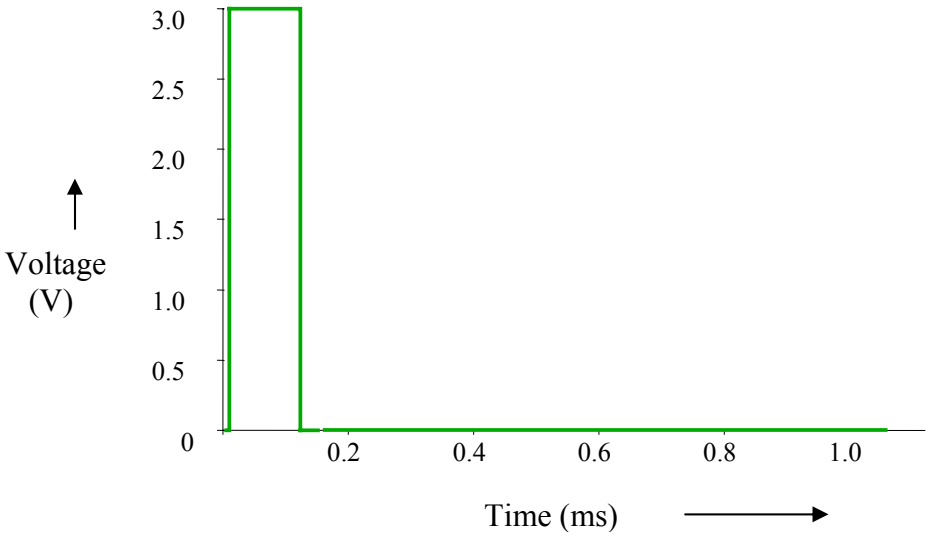



Figure 3.30: Simulated output of the power-on-reset circuit (PR1).

### 3.1.3 Part 3: Design of Pulse Output Conditioning Circuitry

Part 3 includes a voltage regulator circuit (VR3), a charge pump (CP5) and control circuitry for dual polarity pulse stimulations (CDP1). The design, layouts and simulation results of these components are discussed below.

#### 3.1.3.1 Design of Voltage Regulator Circuit

A voltage regulator (VR3) is a power supply device that provides a constant output voltage to a load for a change in the input voltage. For operating an IC, an accurate constant voltage is required making voltage regulator indispensable for battery-powered circuits. Figure 3.31 shows the functional circuit diagram of a typical voltage regulator. The voltage regulator consists of a reference voltage circuit, a voltage divider comprising of R1 and R2, an operational amplifier circuit and a PMOS output transistor M1. The output resistance of the output transistor M1 is controlled so that the voltage at point X1 is equal to Vref. The input voltage Vdd can be changed but the output voltage Vout remains constant. The circuit has a simple configuration and can be designed easily to provide a high quality constant output voltage. The energy conversion efficiency however is low because of the power loss in transistor M1. The output voltage Vout of the regulator shown in Fig. 3.31 is expressed as: $Vout = \left[1 + \frac{R1}{R2}\right] \times Vref$. Therefore, the output voltage of the voltage regulator can be adjusted by setting the resistance ratio.

The difference between the input and the output voltage, Vdif = Vdd-Vout is the voltage required to supply an output current. Transient response characteristics are also important for the performance of the voltage regulator. When Vdd is applied or when output current changes, an overshoot or undershoot of the output voltage occurs. This is undesirable. In order to improve the transient response, the CMOS operational amplifier

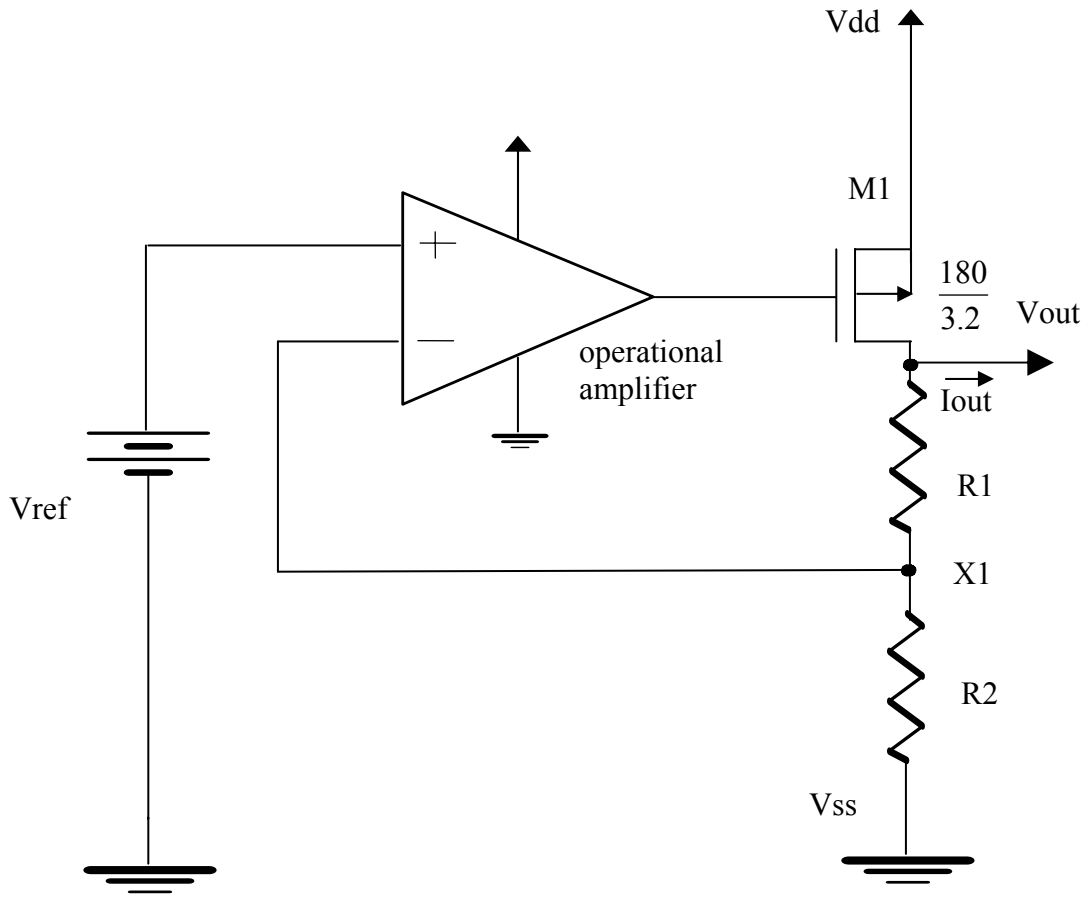



Figure 3.31: Functional circuit diagram of the voltage regulator circuit (VR3). Transistor aspect ratio is shown in μm.

bias current is increased to increase its response speed [24].

In the present application we need to maintain a constant output voltage of 2.8 V for change in the battery voltage from 3 V to 4.2 V. The voltage regulator uses the same operational amplifier as discussed in Appendix C. The voltage reference circuit is designed to maintain a constant reference voltage of 1.65 V. Therefore the ratio of R1 and R2 can be calculated from the above equation of Vout as 0.7. The values of R1 and R2 are chosen as 3 kΩ and 4.3 kΩ respectively.

Figure 3.32 shows the layout and figure 3.33 shows the simulated result of the

voltage regulator for the change in the input voltage from 3 to 4.2 V. The simulations are done for the change in the input battery voltage in ms. However the actual change in the battery voltage will be over several hours.

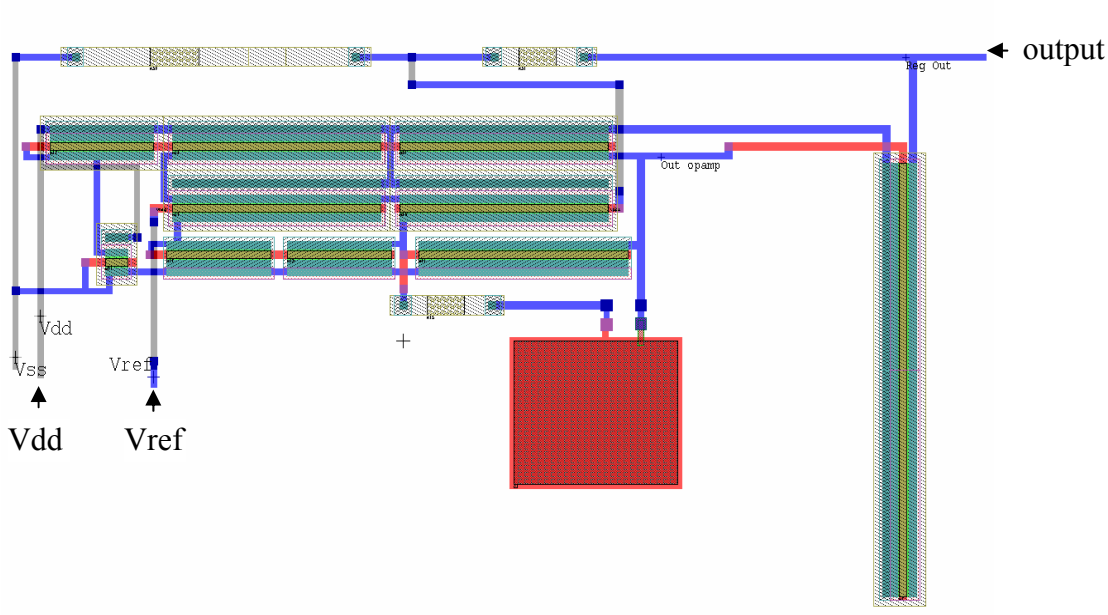



Figure 3.32: Layout of the voltage regulator circuit (VR3) in L-EDIT.

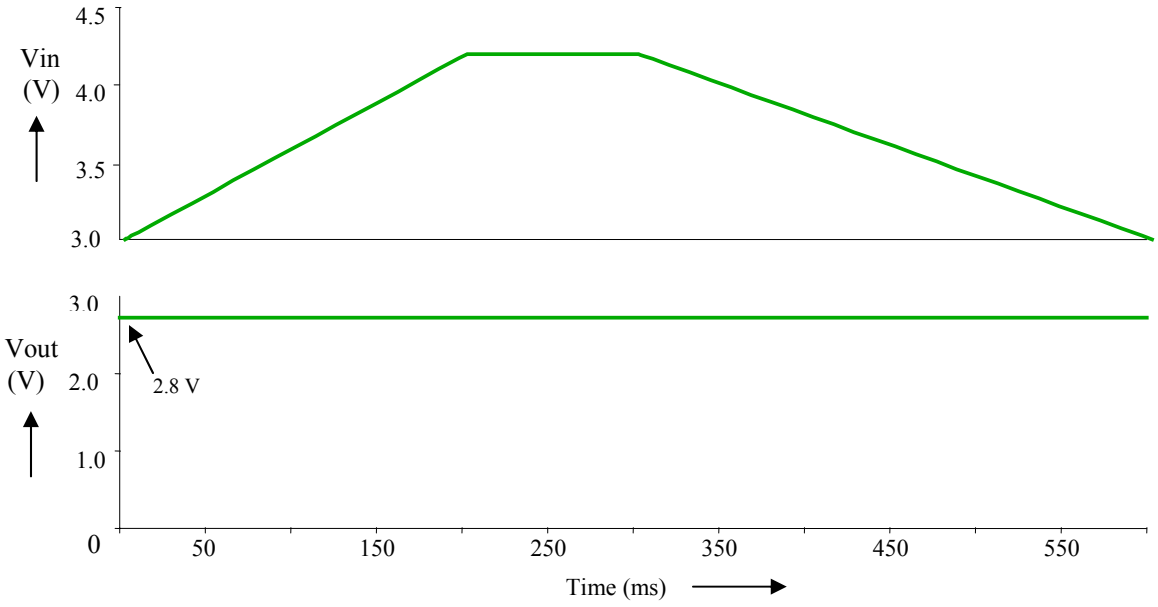



Figure 3.33: Simulated output of the voltage regulator circuit (VR3).

### 3.1.3.2 Design of Charge Pump Circuit

The design of the charge pumps in section 3.1.1.3 was simple as they are operated under no load conditions and require a boost in voltage which was only twice the input voltage. But the design of the charge pump CP5 here requires a boost in voltage to 10 V from a 2.8 V supply. As discussed previously in section 3.1, the stimulation pulses are given for a period of 0.45 ms after being OFF for 9.55 ms. The designed drop in the voltage of the 7.1 μF storage capacitor after pulse ON time in this work is taken to be 1 V. The charge pump should be capable of restoring this charge in the OFF duration of 9.55 ms. This is a constraint for the design of the charge pump (CP5). The charge pump has a regulated output voltage of 10 V. The maximum voltage across the storage capacitor hence is 10 V.

The required boost in voltage in this charge pump is obtained by cascading four single stage charge pumps. If n is the number of stages cascaded together then the total boost in voltage at the output is given by $n\Delta V = Vout - Vin$. Here Vin = Vdd and ΔV is given by equation (1). In a cascaded charge pump, each stage loads the previous stage and hence the gain per each stage ΔV is less than Vdd. This can be seen from equation (1) where the term Rout × Iout is not negligible. Since the charge pump should be capable of charging a 7.1 μF load capacitor, the charge pump capacitors were chosen in the nF range. Though there is flexibility in choosing capacitor values, the output current requirement often dictates the choice of capacitors. As discussed in section 3.1.1.3, the input clock frequency should be chosen as high as possible so that charge is restored in the charge pump capacitors as soon as it is drained out by the load. After simulations a frequency of 5 MHz was found to be optimum. There is however a constraint in the choice of the clock frequency and the capacitors. As the clocks are directly driving these

capacitors, a very large value for capacitors or a very high frequency clock is not desirable as it will increase the number of buffers stages required by the clock to drive the capacitive load. The transistors used in the charge pump (CP5) have the same aspect ratio as discussed in section 3.1.1.3. Figure 3.34 gives the circuit of the cascaded charge pump with capacitors used for each stage. Figure 3.35 gives the layout and figure 3.36 gives the simulated results with a 7.1 μF load capacitor. The simulation shows the charging of 7.1 μF capacitor from 9 V to 10 V in a period of 9.55 ms.

**3.1.3.3 Design of Circuit for Control for Dual Polarity Pacing**

The function of the control for dual polarity pulsing (CDP1) is to alternate the stimulation polarity between the two electrodes. Figure 3.37 shows the functional circuit diagram of the output circuitry with control for dual polarity pacing, output switches and electrodes. A PMOS switch connects each electrode to the stimulation pulses and an NMOS switch connects it to the ground. The outputs B1 and B2 from the control circuit for bipolar pacing are always complement to each other. As seen form figure 3.38 the control block for dual polarity pacing has a JK flip flop with simple logic. Figure 3.39 gives the layout of the circuit for dual polarity pacing and figure 3.40 shows the simulated results done on the functional circuit diagram of the output circuitry for dual polarity pacing.The input clock is the stimulation pulses from PG1 and the input supply voltage is from the cascaded charge pump (CP5).

The control for dual polarity pacing is described below: Initially the output B1 of the JK flip-flop is cleared to zero by giving a clear input from power-on-reset circuit. At the positive edge of the first stimulation pulse, the output B1 goes high and B2 goes low. As a result Electrode 2 is grounded and Electrode 1 is connected to the stimualtion pulse.

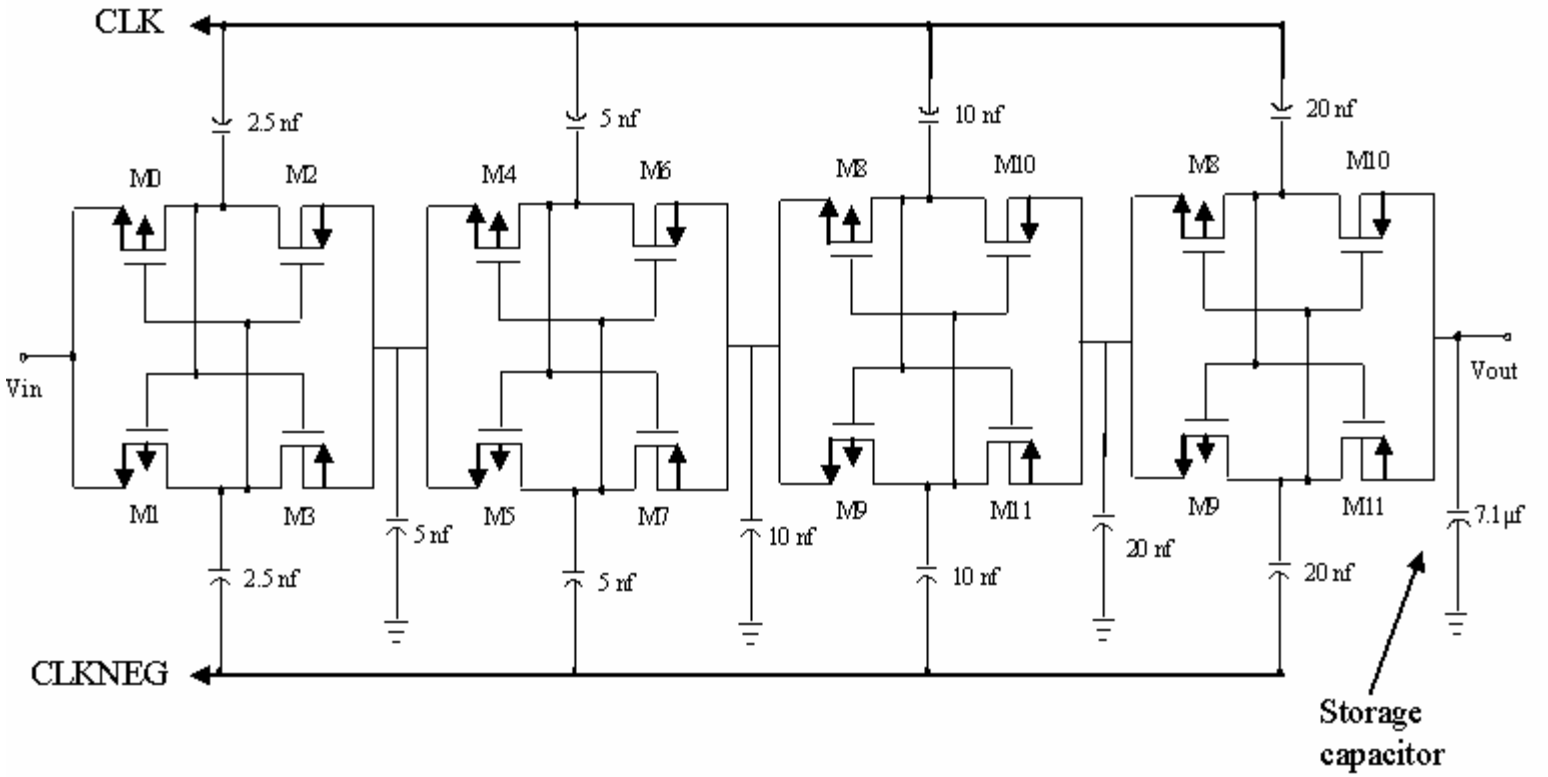



Figure 3.34: Functional circuit diagram of the cascaded charge pump circuit (CP5).

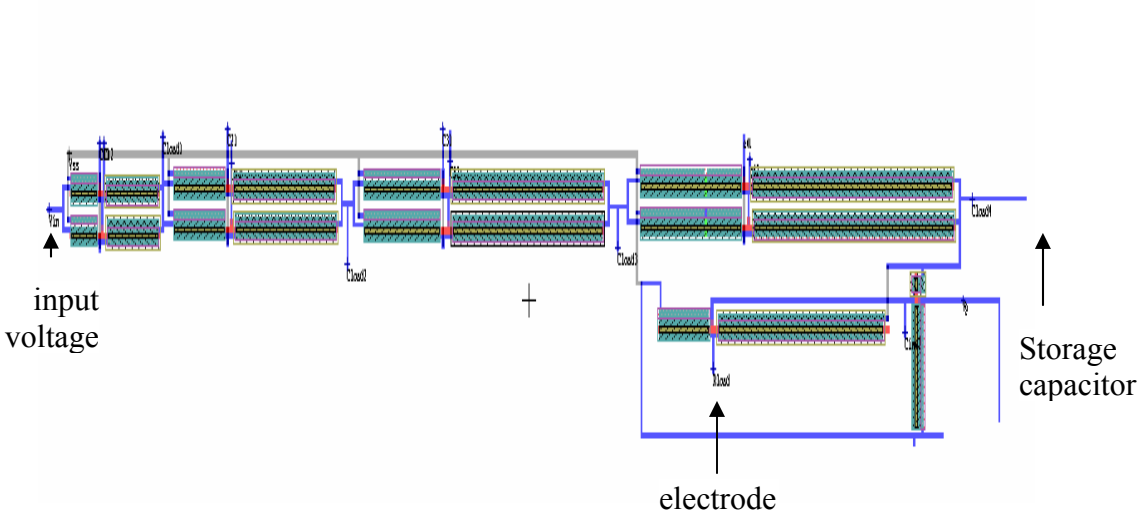



Figure 3.35: Layout of the charge pump circuit (CP5) in L-EDIT.

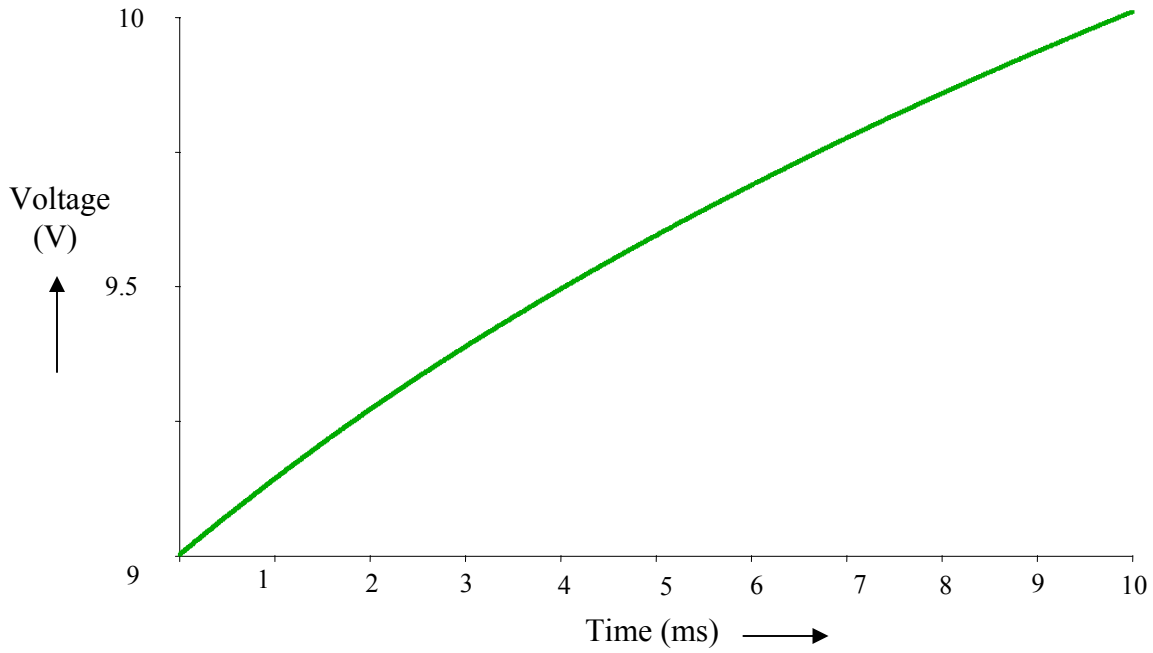



Figure 3.36: Simulated results of the charge pump circuit (CP5) with a load of 7.1 µF.

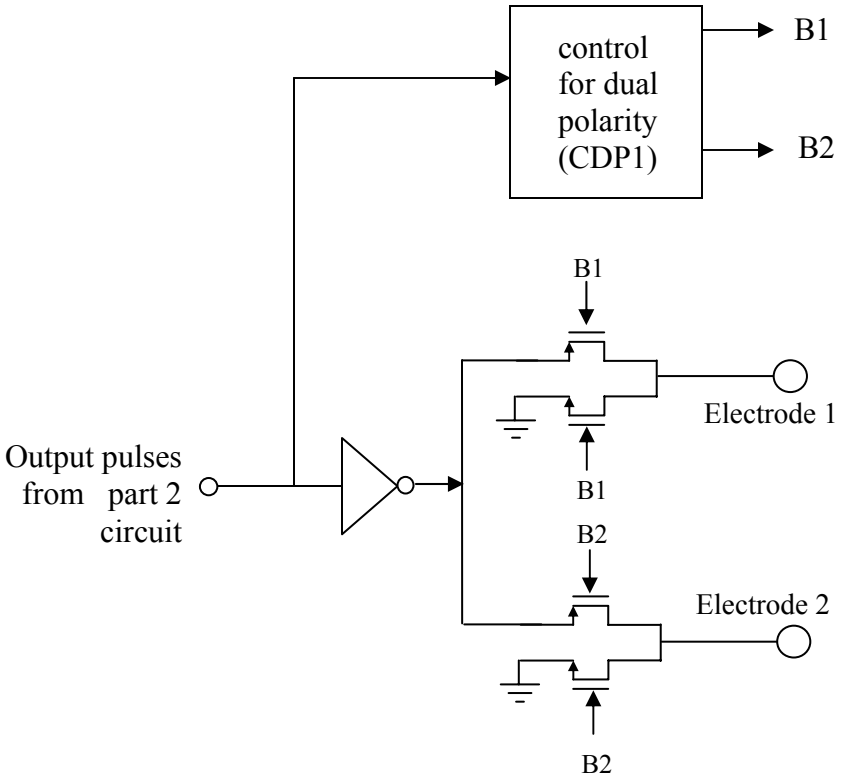



Figure 3.37: Functional circuit diagram of the output circuitry for dual polarity pacing.

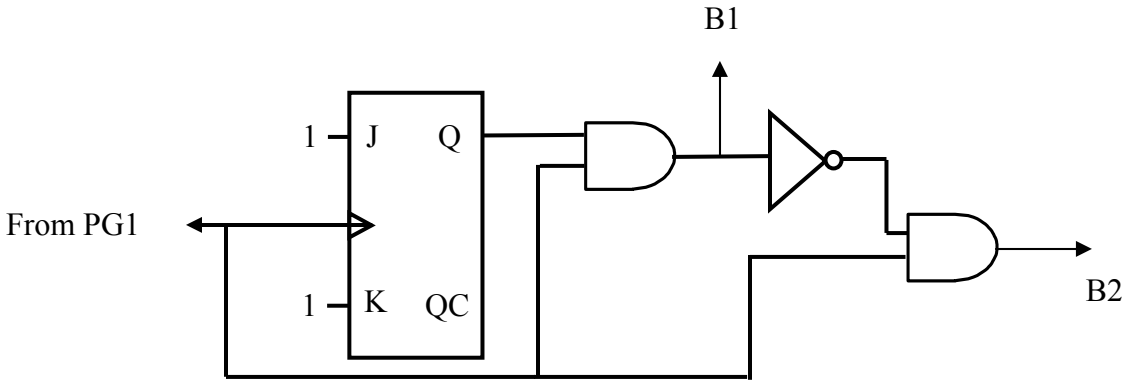



Figure 3.38: Functional circuit diagram for the control block for dual polarity pacing (CDP1).

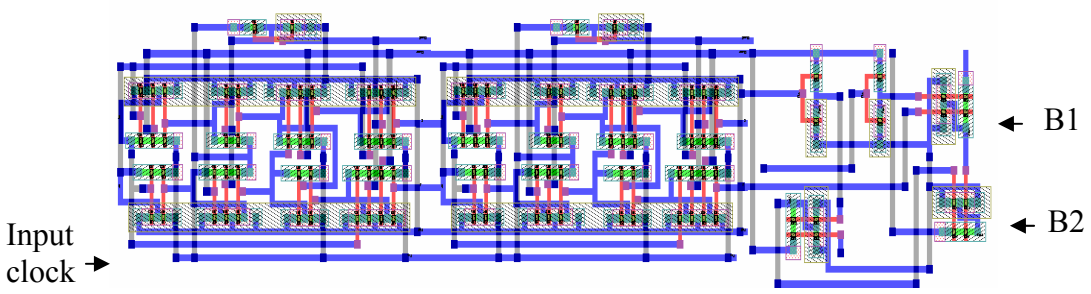



Figure 3.39: Layout of the control circuitry for dual polarity pacing in L-EDIT.

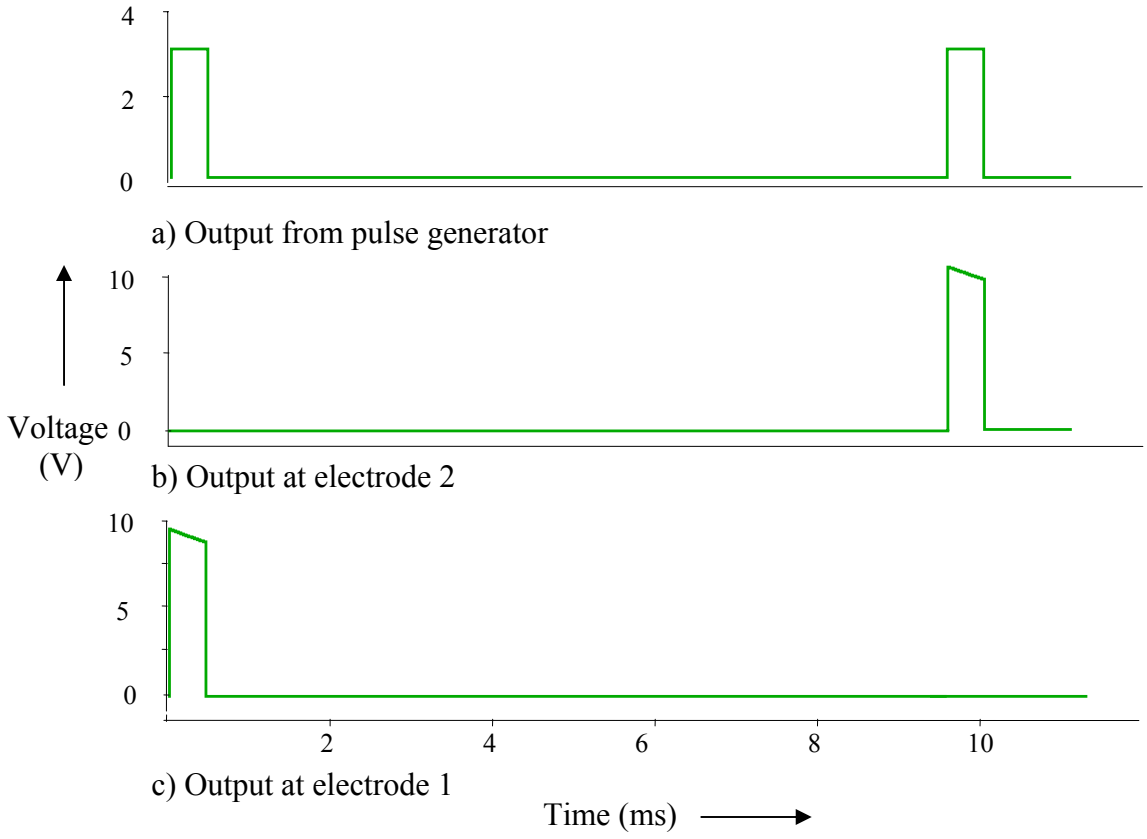



Figure 3.40: Simulated results of the pulse outputs at electrodes 1 and 2.

During the positive edge of the next stimulation pulse, the output B1 goes low and hence B2 goes high.Therfore during the second pulse Electrode 1 is grounded and Electrode 2 is connected to the stimualtion pulses. So at each stimulation pulse the electrodes are alternated.

**3.2 System Simulation**

The complete layout of the signal conditioning IC was done in LEDIT and sent for fabrication. Figure 3.41 shows the chip layout with the padframe. The simulation was done with a 666 Ω resistance as the load. Figure 3.42 shows the simulated result of the IC for the maximum current requirement of 15 mA. There is a slight drop in the voltage and current in the simulated waveforms. This is because of the discharge of the storage capacitor. The maximum power consumption as obtained from the spice simulations was found to be 18 mW. At this rate the energy requirement of the system = 18 mW × 3600 = 64.8 J/hr. The rechargeable battery used in the present application has an energy density of 2.52 kJ. Therefore the energy stored in the battery will last for $\left(\frac{2520}{64.8}\right) = 38.88\ hours$.

So based on the above data, the battery should power the IC close to one and a half day before it needs recharging. The recharging can be done in just about 2.5 hrs.

Earlier experiments were done to simulate the proposed IC on the breadboard with discrete components. The battery could power the system for 15 hrs before it needed recharging. Appendix D shows the setup and results obtained from these experiments. The above results indicate that this approach to avoid periodic surgery for battery replacement has potential for practical applications. This technique does not continuously tie a person to an external power source. This freedom is important in improving quality of life of the patient.

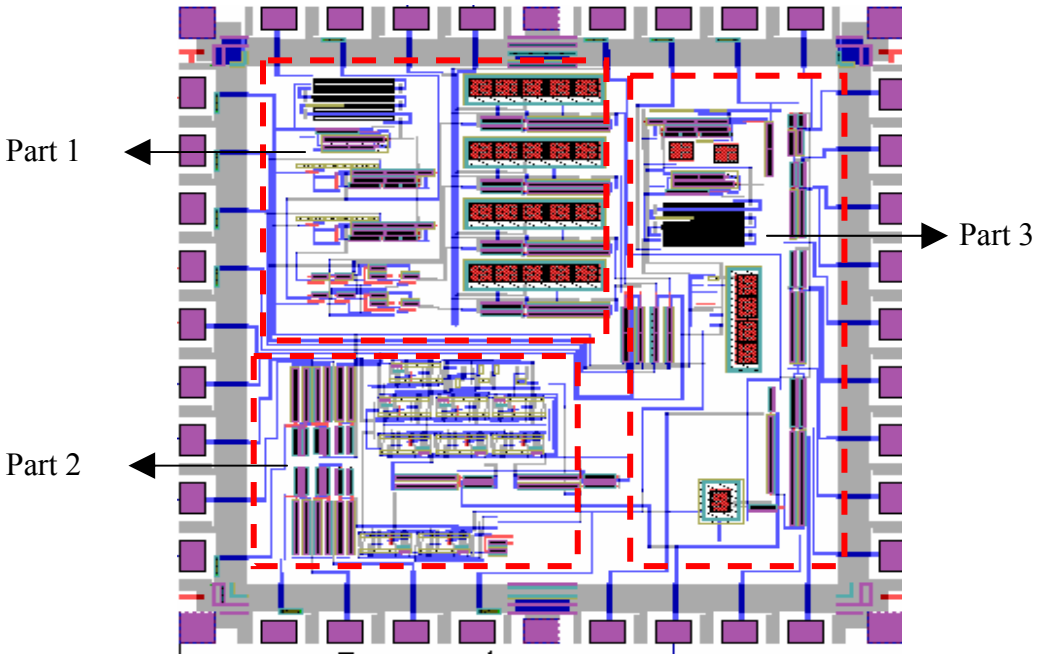



Figure 3.41: Complete layout in the padframe.

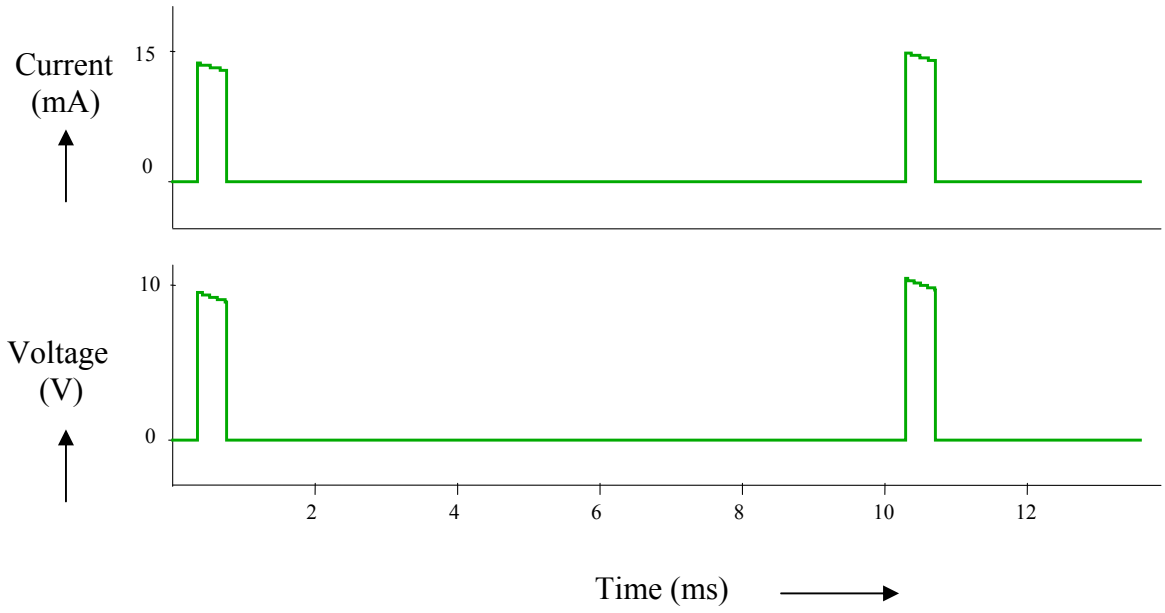



Figure 3.42: Simulated results for output pulses from the chip with a 666 Ω load.

# 4. BESS CHIP TEST RESULTS

## 4.1 Test Results

The BESS chip was designed, fabricated and subsequently tested for functionality. The first version of the designed chip sent to foundry was to demonstrate the functionality of each individual subsystem and to obtain a measure of the power handling capability of the fully integrated chip. The fabricated chip contained all system circuitry except the capacitors to be attached externally. The individual subsystem blocks were then externally connected to demonstrate the functionality of the entire chip. Figure 4.1 shows the microphotograph of the fabricated chip.

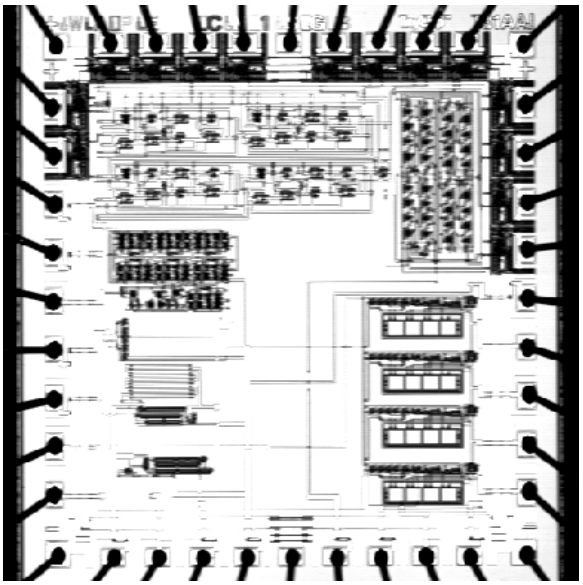


Figure 4.1: Microphotograph of the fabricated chip (2 mm × 2 mm).

Each of the individual blocks sent for fabrication was found to be fully functional. The desired output however slightly deviated from the simulated results from SPICE. This is mainly attributed to the difference in the model parameter values used for simulations and those appropriate for the actual fabrication process used. The model

parameters given in Appendix E show the differences between the values used for simulation and those appropriate for the fabrication process used by the foundry [31].

Figure 4.2 shows the microphotograph of the pulse generator (PG2). The pulse generator was designed to generate pulses of 4.5 % duty cycle with an ON time of 0.45 ms and an OFF time of 9.55 ms. The pulse generator is fully functional and generates pulses with an ON time of 0.43 ms and an OFF time of 9.63 ms. Figure 4.3 shows the output of the pulse generator as seen on the oscilloscope.

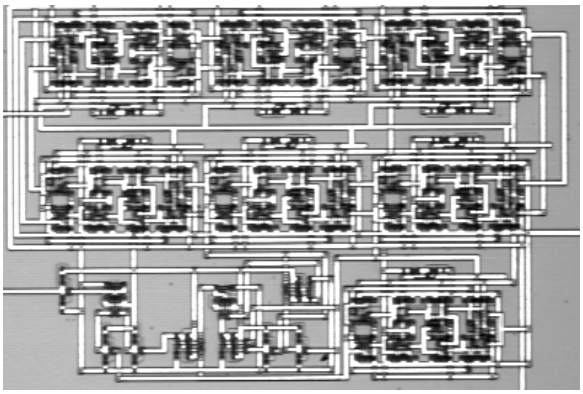


Figure 4.2: Microphotograph of the pulse generator circuit (PG1).

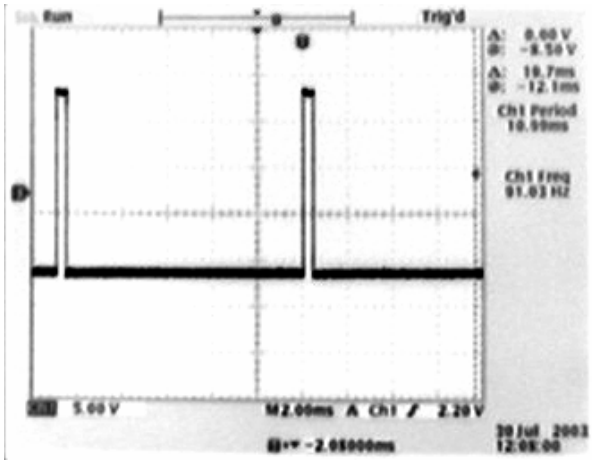



Figure 4.3: Output of the pulse generator circuit (PG1) as seen on oscilloscope.

Figure 4.4 shows the microphotograph of the fabricated charge pump (CP5). The charge pump was designed to boost the voltage to 12 V with an input voltage of 2.8 V. The charge pump is fully integrated with on chip capacitors and clock generators. The on chip clock generators did not work properly. The reason behind this was attributed to the fewer number of inverter stages used for the ring oscillator. However the charge pump was tested using an external clock and was found to be fully functional generating 12 V from a 2.8 V supply. Figure 4.5 shows the output of the charge pump as seen on the oscilloscope.

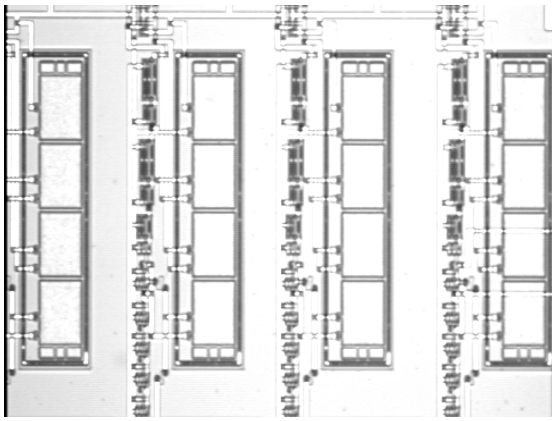


Figure 4.4: Microphotograph of the charge pump circuit (CP5).

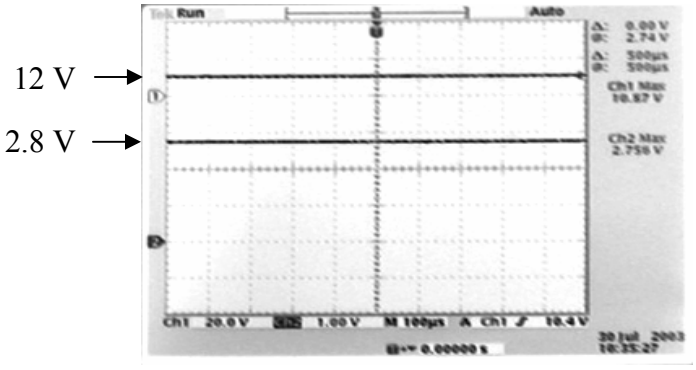



Figure 4.5: Output of the charge pump circuit (CP5) as seen on oscilloscope.

Figure 4.6 shows the microphotograph of the voltage detector circuit (VD1). The voltage detector output was designed to go high when the battery voltage went above 3 V during recharging and go low when the battery discharged below 2 V. The measured output on the fabricated chip however showed that the detector output varied at 1.8 V and at 2.7 V. This was attributed to the differences in the SPICE model parameters used for design simulations and the ones appropriate for the fabrication process used by the foundry.

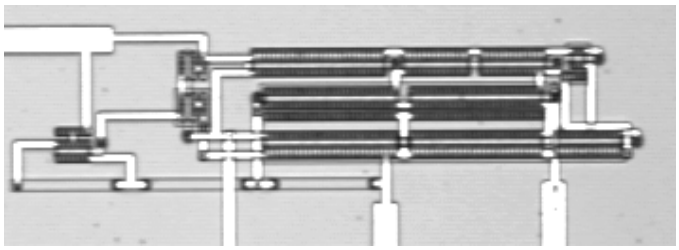


Figure 4.6: Microphotograph of the voltage detector circuit (VD1).

Figure 4.7 shows the microphotograph of the voltage reference circuit block (VR1). The voltage reference was designed to give a standard reference voltage of 1.65 V for a variation in the input voltage. The measured results on the fabricated chip gave a standard reference voltage of 1.33 V. This was again attributed to differences in the SPICE model parameters used for design simulations and the ones appropriate for the fabrication process used by the foundry.

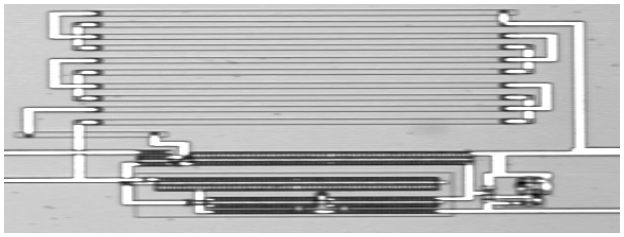


Figure 4.7: Microphotograph of the voltage reference circuit (VR1).

### 4.2 Results on Fabricated Chip at System Level

The charge pump and the pulse generator decide the magnitude and duration of the stimulation pulses. They were connected through external connections and measurements were taken. The system had a maximum capability of 0.9 mA of current at 10 V. This is attributed to the use of on chip capacitors for the charge pump (CP5). The capacitors had a magnitude of 2 pf and hence were not capable of handling high current requirements. Therefore this work indicates that for stimulations which require less than 1 mA of current at 10 V, the system can be monolithically integrated. However, the requirement for the present application is 15 mA of current at 10 V necessitating use of external components and a hybrid integration approach.

### 4.3 BESS Version 2 - Redesign

The BESS chip has been redesigned. This redesigned chip (version 2) has been sent for fabrication. The following modifications were done on the redesigned chip:

1) This chip has all the blocks connected internally and uses external capacitors for the charge pump (CP5) to deliver stimulation up to 15 mA of current at 10 V.
2) The circuits in the redesigned chip were simulated over a wide range of process parameters so that there will not be much variation between the simulation and experimental results.
3) The clock for the charge pump is given externally using a 5 MHz clock generator.

Testing and eventual operation on the second version chip will be carried out under future research by my group members.

# 5. CONCLUSIONS AND SUGGESTIONS FOR FURTHER RESEARCH

## 5.1 Conclusions

A novel, bio implantable chip has been designed and simulated as part of this thesis. This chip, which is part of a Battery-powered Electrical Stimulation System called BESS, provides electrical pulses to nerve or muscle stimulating electrodes. The output can be used for dual polarity pacing. Each output pulse is capable of having maximum amplitude of up to 15 mA current at 10 V. The BESS chip is powered by two rechargeable batteries one of which serves as a reserve back up. The chip receives its power for recharging the batteries through inductive coupling from an external transmitter. The result is a bio-implantable system which requires an external transmitter only for recharging the batteries. The recharging is done only for about 2.5 hours after which the system can operate for over 1.5 days without any external transmitter.

The major contribution of this research is the development of a low power circuitry for use in battery powered implantable microsystems. The circuitry for BESS includes a voltage detector, a voltage reference source, a voltage regulator, a pulse generator, a charge pump, an astable multivibrator, a power-on reset circuit, control switches and a logic block for overall control. All of this circuitry is fully functional and can be easily modified for use with other similar microsystems. The circuitry for BESS designed in this work consumes 18 mW of power from a 3.7 V battery supply. The required power for recharging the batteries is approximately 500 mW and needs to be provided by an external transmitter. Power savings were obtained by reducing bias currents in the analog circuitry, and by running the entire circuit from a single 3.7 V

supply instead of a 10 V battery. The power efficiency of the designed chip is obtained as: $\frac{useful\ power\ to\ electrodes}{power\ consumption} = \frac{6.75\ mW}{18\ mW} = 37.8\ \%$.

## 5.2 Suggestions for Further Research

There are several areas in which the signal conditioning IC can be improved. A few of these are mentioned below.

### 5.2.1 Low Power Consumption

The battery life in portable devices is greatly reduced by high power consumption. An effective method for low power design is to reduce the operating voltage. Therefore smaller capacity batteries can be chosen for the implantable system and by increasing the number of charge pump stages to get the required boost in voltage if and where necessary.

### 5.2.2 Equal Usage of the Two Rechargeable Batteries

The mixed signal IC designed for the present work does not use the two rechargeable batteries equally. If Bat-1 is charging and then finishes charging before Bat-2 is discharged then the control logic block will connect Bat-1 to the supply power and this will leave Bat-2 partially discharged. The reason for this is that the control logic block has only two control inputs and therefore only four possible output configurations. Therefore a better control logic is to be designed which evenly alternates the operation of the batteries. This will increase the total operating life of the implanted device.

### 5.2.3 State of the Battery

The BESS has unidirectional operation; that is power can be sent to the chip from the external transmitter, but it is not possible to communicate in the other direction. It is highly desirable to externally monitor the state of the battery. It enables the user to know

when the battery needs recharging. This information can be transmitted from the implant at a different frequency from the incoming signal or through a code developed for this purpose.

### 5.2.4 Programmable IC

The designed signal conditioning IC is not programmable and can deliver only one type of stimulation signal to the electrodes. Specifically, in the event that the chosen signal does not provide appropriate treatment, another surgical procedure must be performed to implant a unit which can provide a different stimulation signal. Making the IC externally programmable will enable the user to externally change stimulation parameters according to patient's need.

### 5.2.5 Implantable Rechargeable Batteries

The lithium batteries currently used in many implantable medical devices are too big, cannot be recharged, and last only 3 years at most. It is therefore desirable to use micro-miniature, rechargeable, and inherently safe lithium batteries that will last for as many as 10 years. No existing lithium battery technology meets these requirements. Size is a particular challenge, because the implants are very compact in size, and typically batteries require significant fraction of the total volume. The implantable rechargeable micro batteries for BION micro stimulators will be of great interest for such type of works [11]. The micro batteries weigh less than 0.2 g and have a dimension of 2.9 mm × 13 mm.

### 5.2.6 Fully Integrated System

The implant should be miniaturized as far as possible. The challenges in miniaturizing these systems include development of a highly efficient on-chip telemetry coil, and

careful power management to eliminate the need for discrete capacitors. Further lowering circuit losses will also help in reducing volume.

### 5.2.7 Biomedical Issues

There are several biomedical areas that require further investigation before systems such as BESS can find widespread use in humans. Issues such as reliability of batteries, effect of transmitted power on tissues and optimal stimulation parameters need to be examined. Optimal stimulation parameters may vary from one individual to next. Hence, a feedback mechanism to vary the pulse parameters externally is desirable. Biocompatibility of the materials used in the microsystem is also a serious issue that needs to be addressed. It is hoped that the BESS chip will give a start and provide insight into more exciting implantable devices to come.

# REFERENCES


1. Gerald E. Loeb, M.D. and Frances J.R. Richmond, Ph.D. "BION™ implants for therapeutic and functional electrical stimulation", chapter in press in neural prostheses for restoration of sensor and motor function eds. J.K. Chapin, K.A. Moxon and G. Gaal CRC Press, Boca Raton, FL, 2000.

2. Jeffery A. Von Arx "A fully integrated neuromuscular stimulation system-FINESS", doctoral thesis, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, 1998.

3. William N. Borkan "Non-invasive multi programmable tissue stimulator", United States Patent # 4,612,934, September 23, 1986.

4. Babak Ziaie "A single channel micro stimulator for functional neuromuscular stimulation", doctoral thesis, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, 1994.

5. Melzach and Wall "Pain mechanism, a new theory", science, vol. 150, 171-179, 1965.

6. Wall PD and Sweet WH "Temporary abolition of pain in man", science, vol.155, 108-109, 1967.

7. Shealy CN, Mortimer JT and Reswick JB "Electrical inhibition of pain by stimulation of the dorsal columns", preliminary clinical report, Anesth Analg, vol. 46, 489-491, 1967.

8. Reynolds, D.V. "Surgery in the rat during electrical analgesia induced by focal brain stimulation" science, vol. 164, 444-445, 1969.

9. Chaffee, E.L. & Light, R.U. "Supplementary notes on the remote control of electrical stimulation of the nervous system", Yale J. Biol. Med., vol. 7, 441-450, 1935.

10. Mark I. Johnson "The clinical effectiveness of TENS in pain management", electrotherapy – clinical effectiveness, safety and quality assurance, Queen Elizabeth Hospital, Birmingham, 17th May, 2001.

11. Wentai Liu, Kasin Vichienchom, Mark Clements, Stephen C. DeMarco, Chris Hughes, Elliot McGucken, Mark S. Humayun, Eugene de Juan, James D. Weiland, and Robert Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device", IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000.

12. Technical Notes on "Electro-stimulation", Current Technology Corporation, Canada, 2002.

13. Technical Notes on "Electrical stimulation and muscle nerves", Turk Gaonnwe Bio-Medical Engineering, North Carolina State University, Raleigh, NC, 2002.

14. Mokwa, U. Schnakenberg "Implantable microdevices", Techn. Dig. EUROSENSORS XIII, 13th European Conference on Solid State Transducers, Den Hague, The Netherlands, September 12-15, 1999.

15. Application notes on "Principles of nerve stimulation", Staff of ADInstruments, document number # ALB17d, Colorado Springs, CO, 2003.

16. Khalil Amine "Implantable, rechargeable microbatteries for BION™ microstimulators", Chemical Technology Division, Argonne National Laboratory, 2002.

17. Orhan Soykan "Power sources for implantable devices", Business Briefing: Medical Device Manufacturing & Technology, London, 2002.

18. Technical Paper on "The battery and the digital load", Isidor Buchmann, Cadex Electronics Inc., Canada, April 2001.

19. Technical Paper on "The secrets of battery run time", Isidor Buchmann, Cadex Electronics Inc., Canada, April 2001.

20. Massoud Pedram, Qing Wu "Design considerations for battery powered electronics", 36th Design Automation Conference, DAC99, 861-866, New Orleans, LA, June 1999.

21. http://www.ulbi.com/techsheets/UBI-5113_UBC641730.pdf

22. http://www.micrel.com/_PDF/mic79050.pdf.

23. Technical Paper on "Charging lithium-ion batteries", Isidor Buchmann, Cadex Electronics Inc., Canada, April 2001.

24. Xicor Application notes on "Smart battery primer", Carlos Martinez, Yossi Drori and Joe Ciancio, Milpitas, CA, October 1999.

25. R. Jacob Baker, Harry W. Li, David E. Boyce "CMOS circuit design, layout, and simulation", IEEE Press Series on Microelectronic Systems, N.Y., U.S.A., 1998.

26. Application notes on "Applications of battery power supply devices and battery drive circuit design", note number # 104, Seiko Instruments Inc, Torrance, CA.

27. R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, P. L. Rolandi "Power efficient charge pump in deep submicron standard CMOS technology", in Proc. 27th European Solid-State Circuits Conference (ESSCIRC), Villach, Austria, September 2001.

28. M. Morris Mano “Digital logic and computer design”, by Prentice-Hall Inc., Englewood Cliffs, N.J., U.S.A., 1979.

29. D. Hodges, H. Jackson “Analysis and design of digital integrated circuits”, McGraw-Hill, N.Y., U.S.A., 1988.

30. Application notes on “A Power-On Reset (POR) Circuit for Actel Devices”, by Actel Corporation, Mountain View, CA, 1997.

31. http://www.mosis.org/Technical/Testdata/ami-abn-prm.html

32. Prasanna, Seshagiri Venkatesh “Design and implementation of low noise readout electronics in CMOS for a fast timing charge couple device”, master thesis, Department of Electrical and Computer Engineering, Louisiana State University, Baton Rouge, LA, 1997.

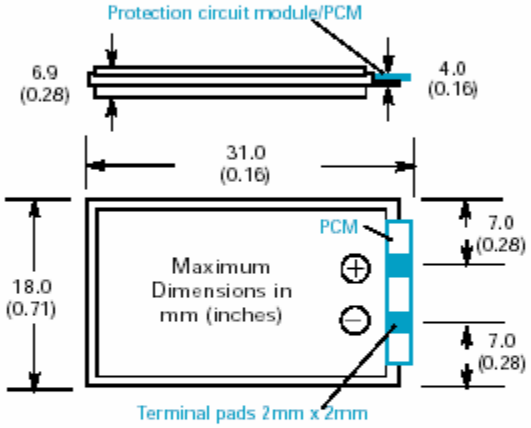
# APPENDIX A: DATASHEET OF THE RECHARGEABLE BATTERY

ULTRALIFE BATTERIES INC

## TECHNICAL DATA

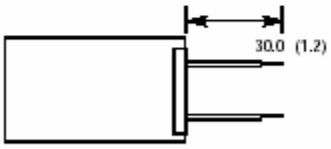
### Polymer Rechargeable System


UBC641730/PCM




**Options:**

A. PCM W/Wires




Contact UBI for availability and for other termination options

### UBC641730/PCM

| | |
|---|---|
| System: | Lithium Polymer Rechargeable |
| Part No. | UBC005 |
| Voltage Range: | 4.20 to 3.0 Volts |
| Average Voltage: | 3.7 Volts |
| Nominal Capacity: | 200 mAh @ C/5 Rate @ 23°C |
| Max. Discharge: | 2C Continuous |
| Energy: | 0.7 Wh |
| Energy Density: | 156 Wh/kg 296 Wh/l |
| Weight: | 4.5 grams |
| Cycle Life: | >300 Cycles @C/5 to 80% of initial capacity |
| Memory: | No Memory Effect |
| Operating Temp.: | –20°C to 60°C |
| Storage Temp.: | –20°C to 60°C |
| Self-Discharge: | <10% Per Month |
| Jacket: | Laminated Foil |
| Wire Gage: | 30 AWG |
| Transportation: | Excepted From Regulations (1) See reverse for further details |

**PROTECTION CIRCUIT MODULE (PCM)**

| | |
|---|---|
| Over Voltage limit: | 4.275 +/- 0.025 volts |
| Under voltage limit: | 2.3 ± 0.07 V |
| Maximum Current: | 1.5 A @ RT |
| Quiescent Current: | 10 µA |

CHARGING: Maximum charge rate at C/2 to 4.20V in a temperature range of 0-45°C. Hold at 4.20V until current declines to C/10. Refer also to Safety Guide UBI-5112.

Other termination options are available. Please contact Ultralife for details.

Apr 01 '03 • UBI-5113 Rev. B.

www.ultralifebatteries.com

# APPENDIX B: DATASHEET OF THE BATTERY CHARGING CHIP

## MIC79050

**Simple Lithium-Ion Battery Charger**

**Final Information**

### General Description

The MIC79050 is a simple single-cell lithium-ion battery charger. It includes an on-chip pass transistor for high precision charging. Featuring ultrahigh precision (±0.75% over the Li-ion battery charging temperature range) and "zero" off mode current, the MIC79050 provides a very simple, cost effective solution for charging lithium-ion battery.

Other features of the MIC79050 include current limit and thermal shutdown protection. In the event the input voltage to the charger is disconnected, the MIC79050 also provides minimal reverse-current and reversed-battery protection.

The MIC79050 is a fixed 4.2V device and comes in the thermally-enhanced MSO-8, SO-8, and SOT-223 packages. The 8-pin versions also come equipped with enable and feedback inputs. All versions are specified over the temperature range of –40°C to +125°C.

### Features

- High accuracy charge voltage:
  ±0.75% over -5°C to + 60°C (Li-ion charging temperature range)
- "Zero" off-mode current
- 10µA reverse leakage
- Ultralow 380mV dropout at 500mA
- Wide input voltage range
- Logic controlled enable input (8-pin devices only)
- Thermal shutdown and current limit protection
- Power MSOP-8, Power SOP-8, and SOT-223
- Pulse charging capability

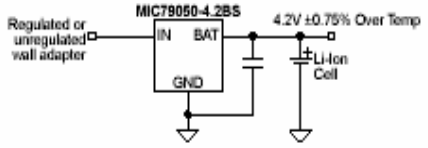
### Applications

- Li-ion battery charger
- Celluar phones
- Palmtop computers
- PDAs
- Self charging battery packs

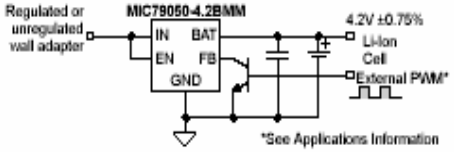
### Ordering Information

| Part Number | Voltage | Junct. Temp. Range | Package |
|---|---|---|---|
| MIC79050-4.2BS | 4.2V | –40°C to +125°C | SOT-223 |
| MIC79050-4.2BM | 4.2V | –40°C to +125°C | SOP-8 |
| MIC79050-4.2BMM | 4.2V | –40°C to +125°C | MSOP-8 |

### Typical Applications




**Simplest Battery Charging Solution**




**Pulse-Charging Application**

## Absolute Maximum Ratings (Note 1)

Supply Input Voltage ($V_{IN}$) ..... –20V to +20V
Power Dissipation ($P_D$) ..... Internally Limited, **Note 3**
Junction Temperature ($T_J$) ..... –40°C to +125°C
Lead Temperature (soldering, 5 sec.) ..... 260°C
Storage Temperature ($T_S$) ..... –65°C to +150°C

## Operating Ratings (Note 2)

Supply Input Voltage ($V_{IN}$) ..... +2.5V to +16V
Enable Input Voltage ($V_{EN}$) ..... 0V to $V_{IN}$
Junction Temperature ($T_J$) ..... –40°C to +125°C
Package Thermal Resistance (Note 3) .....
MSOP-8 ($\theta_{JA}$) ..... 80°C/W
SOP-8($\theta_{JA}$) ..... 63°C/W
SOT-223($\theta_{JC}$) ..... 15°C/W

## Electrical Characteristics

$V_{IN} = V_{BAT} + 1.0V$; $C_{OUT} = 4.7\mu F$; $I_{OUT} = 100\mu A$; $T_J = 25°C$, **bold** values indicate $–40°C \le T_J \le +125°C$; unless noted.

| Symbol | Parameter | Conditions | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | Battery Voltage Accuracy | variation from nominal $V_{OUT}$ –5°C to +60°C | –0.75 | | +0.75 | % |
| $\Delta V_{BAT}/\Delta T$ | Battery Voltage Temperature Coefficient | **Note 4** | | **40** | | ppm/°C |
| $\Delta V_{BAT}/V_{BAT}$ | Line Regulation | $V_{IN} = V_{BAT} + 1V$ to 16V | | 0.009 | 0.05<br>**0.1** | %/V<br>%/V |
| $\Delta V_{BAT}/V_{BAT}$ | Load Regulation | $I_{OUT}$ = 100µA to 500mA, **Note 5** | | 0.05 | 0.5<br>**0.7** | %<br>% |
| $V_{IN} – V_{BAT}$ | Dropout Voltage, **Note 6** | $I_{OUT}$ = 500mA | | 380 | 500<br>**600** | mV<br>mV |
| $I_{GND}$ | Ground Pin Current, **Notes 7, 8** | $V_{EN} \ge 3.0V$, $I_{OUT}$ = 100µA | | 85 | 130<br>**170** | µA<br>µA |
| | | $V_{EN} \ge 3.0V$, $I_{OUT}$ = 500mA | | 11 | 20<br>**25** | mA<br>mA |
| $I_{GND}$ | Ground Pin Quiescent Current, **Note 8** | $V_{EN} \le 0.4V$ (shutdown) | | 0.05 | **3** | µA |
| | | $V_{EN} \le 0.18V$ (shutdown) | | 0.10 | **8** | µA |
| PSRR | Ripple Rejection | f = 120Hz | | 75 | | dB |
| $I_{LIMIT}$ | Current Limit | $V_{BAT}$ = 0V | | 750 | 900<br>**1000** | mA<br>mA |
| $\Delta V_{BAT}/\Delta P_D$ | Thermal Regulation | **Note 9** | | 0.05 | | %/W |
| **ENABLE Input** | | | | | | |
| $V_{ENL}$ | Enable Input Logic-Low Voltage | $V_{EN}$ = logic low (shutdown) | | 0.4 | <br>**0.18** | V<br>V |
| | | $V_{EN}$ = logic high (enabled) | **2.0** | | | V |
| $I_{ENL}$ | Enable Input Current | $V_{ENL} \le 0.4V$ (shutdown) | | 0.01 | –1 | µA |
| | | $V_{ENL} \le 0.18V$ (shutdown) | | **0.01** | **–2** | µA |
| $I_{ENH}$ | | $V_{ENH} \ge 2.0V$ (enabled) | | 5 | 20<br>**25** | µA<br>µA |

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** The maximum allowable power dissipation at any $T_A$ (ambient temperature) is calculated using: $P_{D(max)} = (T_{J(max)} – T_A) \div \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

**Note 4.** Battery voltage temperature coefficient is the worst case voltage change divided by the total temperature range.

**Note 5.** Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 100µA to 500mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

**Note 6.** Dropout voltage is defined as the input to battery output differential at which the battery voltage drops 2% below its nominal value measured at 1V differential.

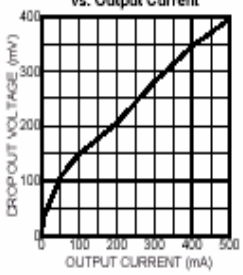
**Note 7:** Ground pin current is the charger quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

**Note 8:** $V_{EN}$ is the voltage externally applied to devices with the EN (enable) input pin. [MSO-8(MM) and SO-8 (M) packages only.]

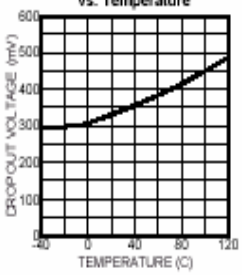
**Note 9:** Thermal regulation is the change in battery voltage at a time 't' after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 500mA load pulse at $V_{IN}$ = 16V for t = 10ms.

## Typical Characteristics

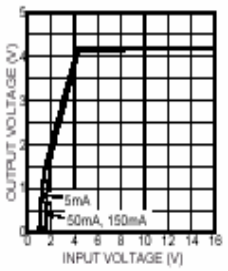
Dropout Voltage vs. Output Current



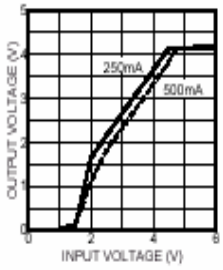

Dropout Voltage vs. Temperature



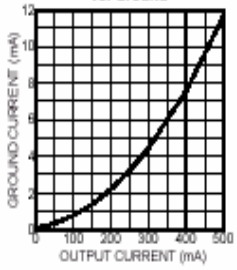

Dropout Characteristics



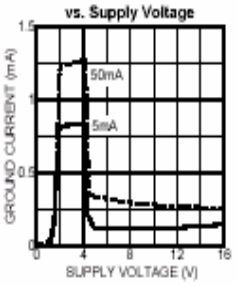

Dropout Characteristics



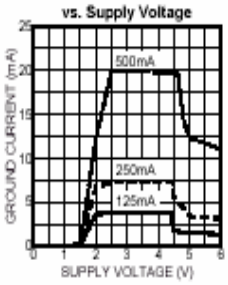

Output Current vs. Ground



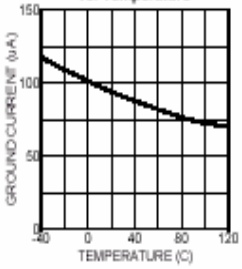

Ground Current vs. Supply Voltage



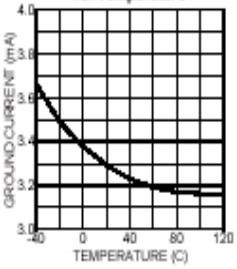

Ground Current vs. Supply Voltage



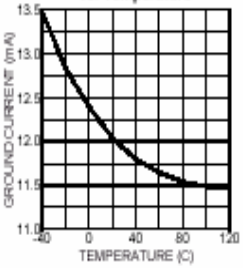

Ground Current vs. Temperature



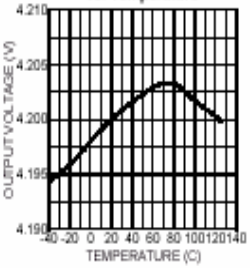

Ground Current vs. Temperature



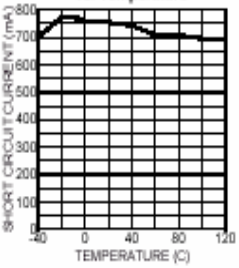

Ground Current vs. Temperature



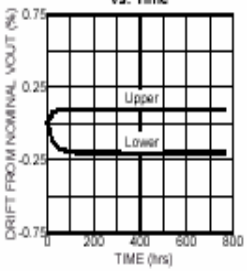

Battery Voltage vs. Temperature



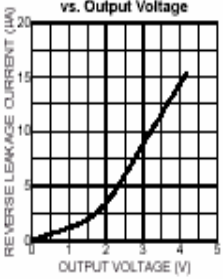

Short Circuit Current vs. Temperature



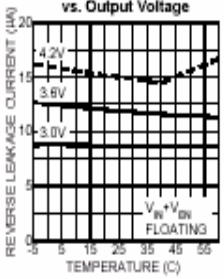
**Typical Voltage Drift Limits vs. Time**



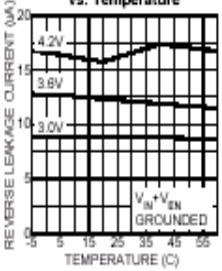

**Reverse Leakage Current vs. Output Voltage**




**Reverse Leakage Current vs. Output Voltage**




**Reverse Leakage Current vs. Temperature**



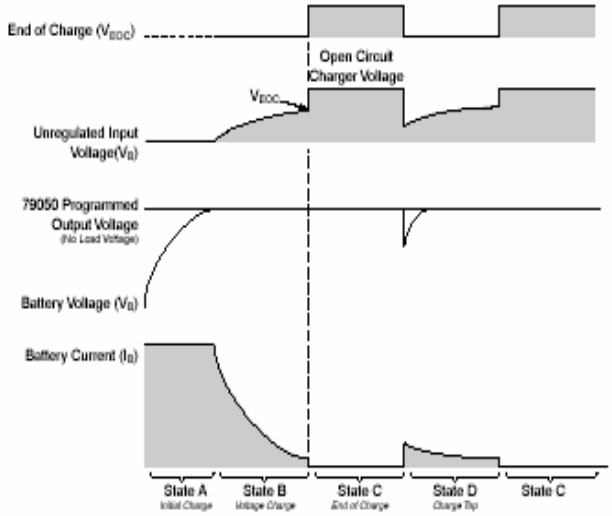



**Figure 1C. Charging Cycles**

**The Charging Cycle (See Figure 1C.)**

1. State A: Initial charge. Here the battery's charging current is limited by the wall adapter's natural impedance. The battery voltage approaches 4.2V.
2. State B: Constant voltage charge. Here the battery voltage is at 4.2V ± 0.75% and the current is decaying in the battery. When the battery has reached approximately 1/10th of its 1C rating, the battery is considered to have reached full charge. Because of the natural characteristic impedance of the cheap wall adapters, as the battery voltage decreases so the input voltage increases. The MIC6270 and the LM4041 are configured as a simple voltage monitor, indicating when the input voltage has reached such a level so the current in the battery is low, indicating full charge.
3. State C: End of charge cycle. When the input voltage, $V_S$ reaches $V_{EOC}$ an end of charge signal is indicated.
4. State D: Top up charge. As soon as enough current is drawn out of the input source, which pulls the voltage lower than the $V_{EOC}$, the end of charge flag will be pulled low and charging will initiate.

Variations on this scheme can be implemented, such as the circuit shown in Figure 2.

For those designs that have a zero impedance source , see Figure 3.

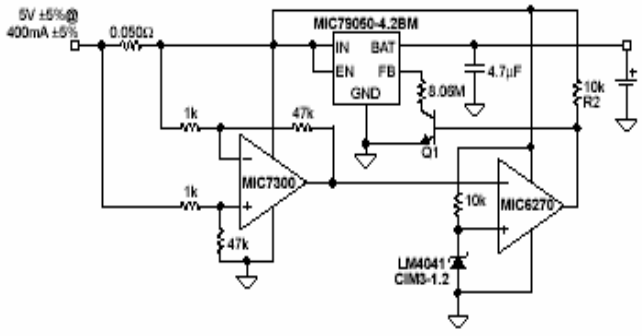
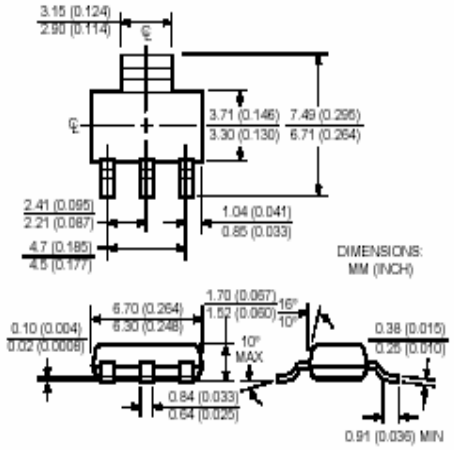
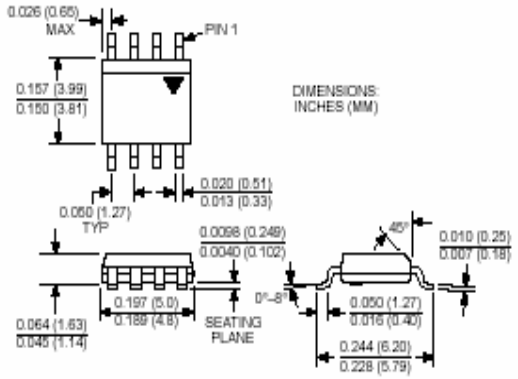



**Figure 2. Protected Constant-Current Charger**

## Package Information




**SOT-223 (S)**




**8-Pin SOP (M)**

# APPENDIX C: DESIGN OF THE OPERATIONAL AMPLIFIER

The voltage regulator circuit (VR1) and the voltage detector circuits (VD1 and VD2) use the same operational amplifier. The operational amplifiers used in these circuits are in a feedback loop and have DC inputs. Hence the main design considerations for the operational amplifiers are large gain, slew rate and stability. The circuits use the operational amplifier shown in figure C.1.

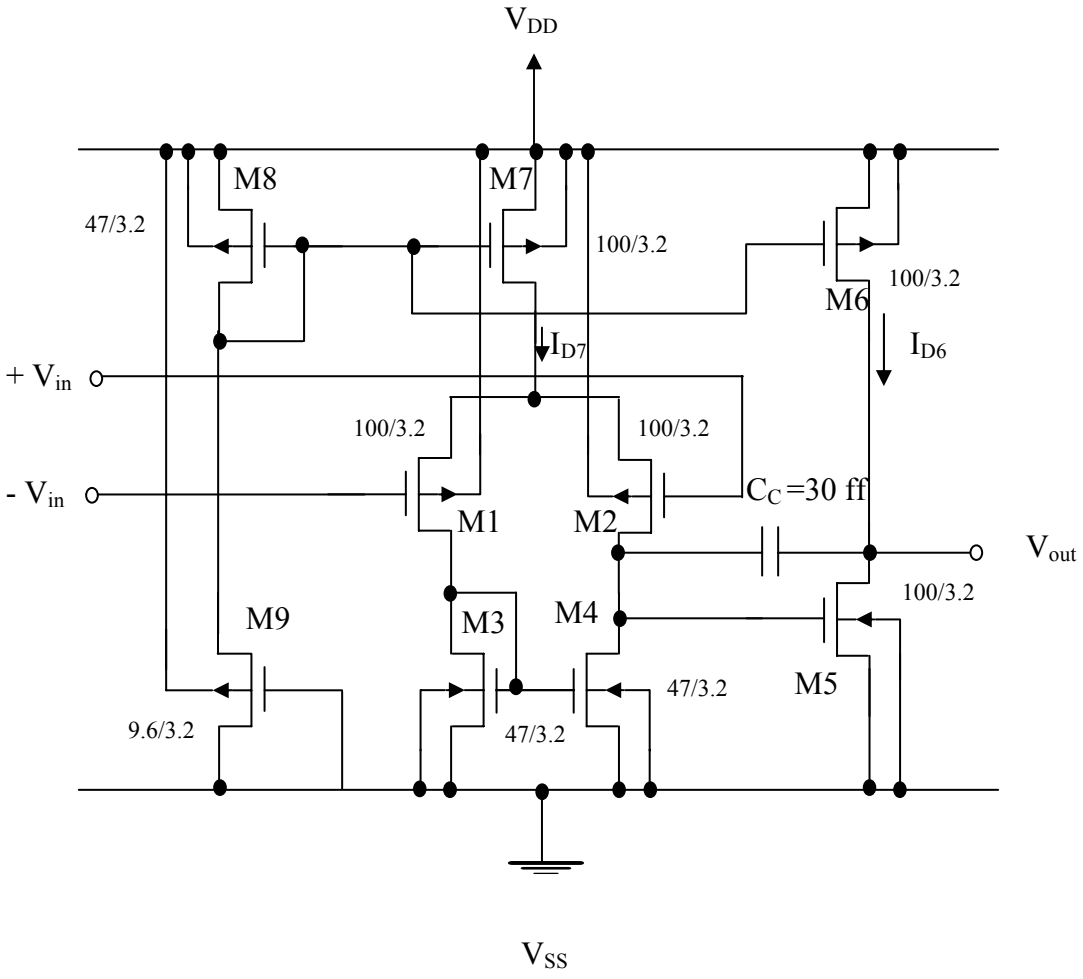



Figure C.1: CMOS operational amplifier circuit diagram.

**DESIGN:**

DC supplies were fixed first at Vdd = 3.7 V and Vss = 0 V.

The first step is to calculate the minimum value of the compensating capacitor. This is important for the stability of the operational amplifier. The compensating capacitor Cc should be greater than 0.22 × CL where CL is the load capacitance. As the output of the amplifier goes to the gate of a transistor, an approximate value of the output capacitor is taken as 100 ff. Therefore the compensating capacitor Cc > 0.22 × 100 ff. The value of the Cc is therefore taken as 30 ff.

To get a high gain with reasonable high output resistance the minimum channel length used is 3.2 μm and maximum width of the transistor used is 100 μm. Transistor M5 is critical to the frequency response and is biased at $I_{D5}$ = 100 μA and has $(W/L)_5$ = $(W/L)_{max}$ = 31.25. The input pair is biased at $-I_{D7}$ = 100 μA. To avoid input offset voltage transistors M3 and M4 are dimensioned according to

$$\frac{\left(W/L\right)_5}{2\times\left(W/L\right)_{3,4}} = \frac{-I_{D6}}{I_{D7}} = \frac{100\,\mu A}{100\,\mu A} = 1 \rightarrow \left(\frac{W}{L}\right)_{3,4} = \frac{1}{2}\left(\frac{W}{L}\right)_5 = 15.6$$

Therefore the W = 47 μm for the transistors M3, M4. In order to obtain the bias current of 50 μA, a MOS resistor is used. The open loop gain of the designed amplifier is approximately 8444.3 [32].

# APPENDIX D: EXPERIMENTAL SET UP

Basic experiments were done with discrete components to simulate the proposed IC on the breadboard. The experimental results determined useful results like the approximate power dissipation of the system and the lifetime of the batteries to power such systems. The experimental results showed that a lithium battery with an energy capacity of 1.71 kJ could power the breadboard circuit for 15 hrs and it took 4 hrs to recharge the battery. The power dissipation in this case was 10.1 mW with a 666 Ω load. The block diagram of the experimental set up is shown in figure D.1.

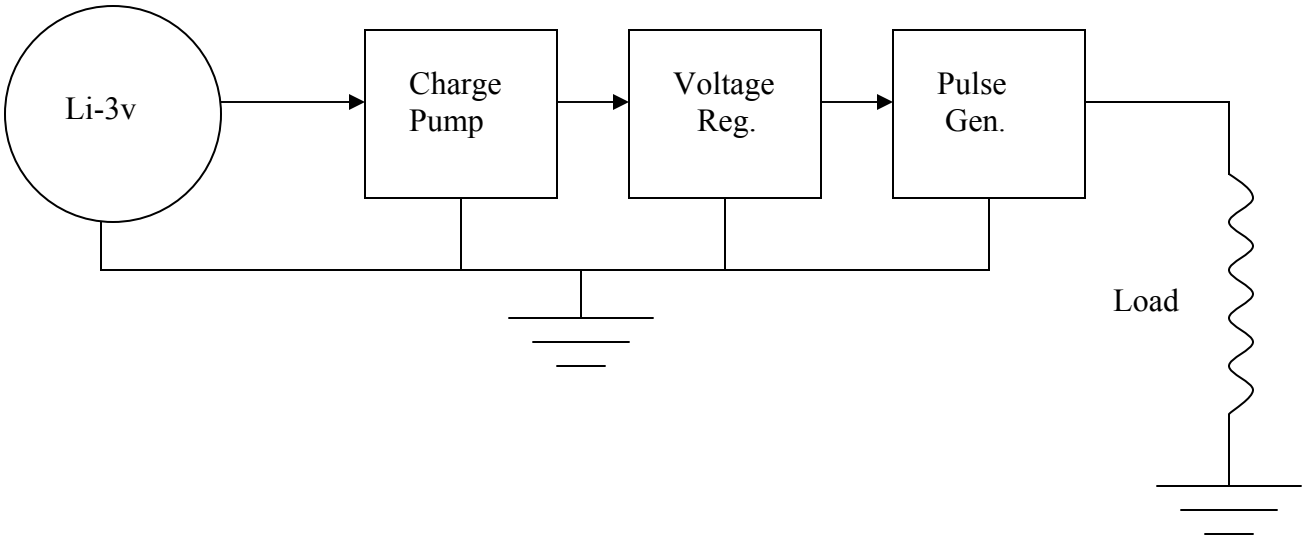



Figure D.1: Block diagram of the experimental set.

The charge pump uses four cascaded stages and boosts an input voltage of 2 V to 10 V. The voltage regulator maintains a constant output voltage of 10 V for change in the input voltage from 2 V to 3 V. The pulse generator generates 10 V pulses at a frequency of 100 Hz. The load used was a 666 Ω resistance to simulate the electrodes. The experimental results are shown in figures D.2 and D.3.

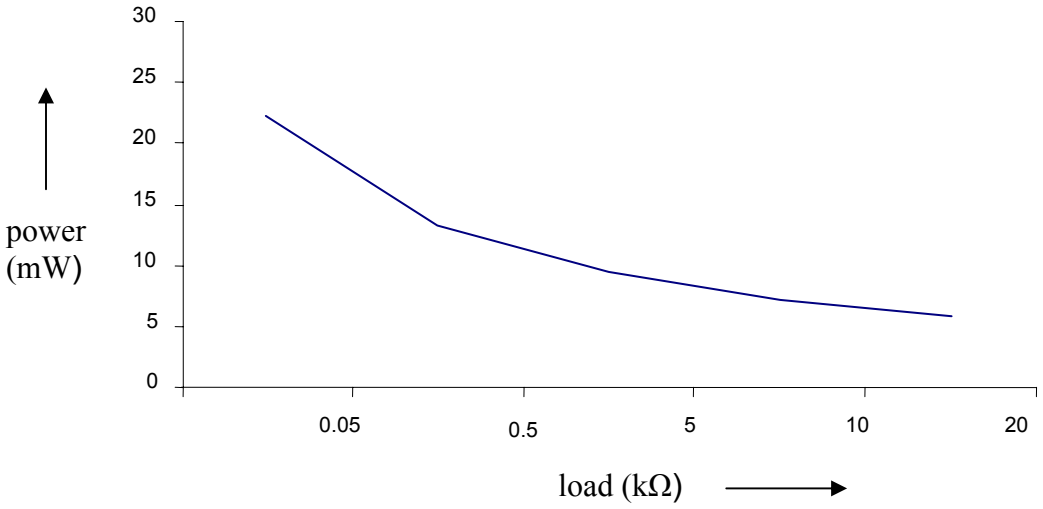



Figure D.2: Power dissipation with a 666 Ω load resistance.

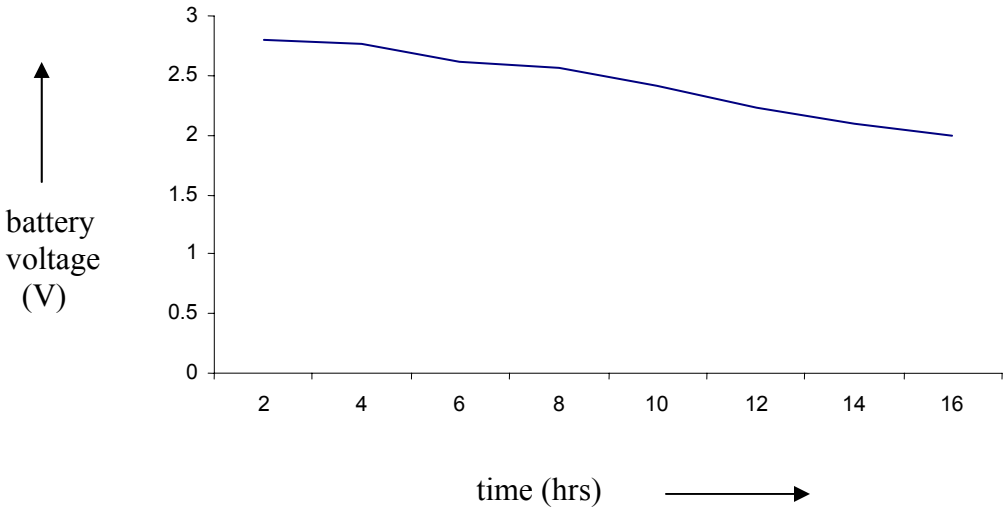



Figure D.3: Battery voltage with time for a 666 Ω load resistance.

# APPENDIX E: MOSIS MODEL PARAMETERS

**(A) Model parameters for NMOS transistor used for simulation**

.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U

+TPG=1 VTO=0.687 DELTA=0.0000E+00 LD=1.0250E-07 KP=7.5564E-05

+ UO=671.8 THETA=9.0430E-02 RSH=2.5430E+01 GAMMA=0.7822

+ NSUB=2.3320E+16 NFS=5.9080E+11 VMAX=2.0730E+05 ETA=1.1260E-01

+ KAPPA=3.1050E-01 CGDO=1.7294E-10 CGSO=1.7294E-10

+ CGBO=5.1118E-10 CJ=2.8188E-04 MJ=5.2633E-01 CJSW=1.4770E-10

+ MJSW=1.00000E-01 PB=9.9000E-01

**(B) Model parameters for PMOS transistor used for simulation**

.MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U

+TPG=-1 VTO=-0.7574 DELTA=2.9770E+00 LD=1.0540E-08 KP=2.1562E-05

+ UO=191.7 THETA=1.2020E-01 RSH=3.5220E+00 GAMMA=0.4099

+ NSUB=6.4040E+15 NFS=5.9090E+11 VMAX=1.6200E+05 ETA=1.4820E-01

+ KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11

+ CGBO=4.2580E-10 CJ=2.9596E-04 MJ=4.2988E-01 CJSW=1.8679E-10

+MJSW=1.5252E-01PB=7.3574E-01

**(C) Model parameters for NMOS transistor appropriate for the fabrication process used by the foundry**

.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.1600E-08 XJ=0.300000U

+TPG=1 VTO=0.5987117 DELTA=0.3875751 LD=1.174128E-9 KP=7.08961E-05

+ UO=623.6531569 THETA=7.30459E-02 RSH=0.1128881 GAMMA=0.707171

+ NSUB=1E+15 NFS=5.333972E+11 VMAX=2.387645E+05 ETA=1.341804E-03

+ KAPPA=5.E-01 CGDO=1.77E-10 CGSO=1.77E-10 CGBO=1E-10 CJ=2.668841E-04

+MJ=0.5 CJSW=1.503861E-10 MJSW=1.475265E-01 PB=8E-01 WD= 6.894829E-7

**(D) Model parameters for PMOS transistor appropriate for the fabrication process used by the foundry**

.MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.1600E-08 XJ=0.200000U

+TPG=-1 VTO=-0.8885277 DELTA=0.4015991E+00 LD=1E-14 KP=2.361102E-05

+ UO=100 THETA=1.301311E-01 RSH=37.9238316E+00 GAMMA=0.5055224

+ NSUB=1E+17 NFS=4.064414E+11 VMAX=3.251631E+05 ETA=1.215165E-05

+ KAPPA=140 CGDO=2.16E-10 CGSO=2.16E-10 CGBO=1E-10 CJ=2.994545E-04

+MJ=4.429209E-01 CJSW=1.49312E-10 MJSW=0.781232 PB=0.8 WD= 1E-6

# VITA

Satish Kona was born on April 17, 1980, in Visakhapatnam, India. He completed his secondary education from Alfa Junior College, Visakhapatnam, India, in May 1997. He received the degree of Bachelor of Engineering in Electrical and Electronics Engineering from Gandhi Institute of Technology and Management, Visakhapatnam, India, in May 2001. Later in August 2001, he was enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, to attend graduate school. He is presently a candidate for the degree of Master of Science in Electrical and Computer Engineering.