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Phase Noise in CMOS Phase-Locked Loop Circuits

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PHASE NOISE IN CMOS PHASE-LOCKED LOOP CIRCUITS

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ABSTRACT

Phase-locked loops (PLLs) have been widely used in mixed-signal integrated circuits. With the continuously increasing demand of market for high speed, low noise devices, PLLs are playing a more important role in communications. In this dissertation, phase noise and jitter performances are investigated in different types of PLL designs. Hot carrier and negative bias temperature instability effects are analyzed from simulations and experiments.

Phase noise of a CMOS phase-locked loop as a frequency synthesizer circuit is modeled from the superposition of noises from its building blocks: voltage-controlled oscillator, frequency divider, phase-frequency detector, loop filter and auxiliary input reference clock. A linear time invariant model with additive noise sources in frequency domain is presented to analyze the phase noise. The modeled phase noise results are compared with the corresponding experimentally measured results on phase-locked loop chips fabricated in 0.5 μm n-well CMOS process.

With the scaling of CMOS technology and the increase of electrical field, MOS transistors have become very sensitive to hot carrier effect (HCE) and negative bias temperature instability (NBTI). These two reliability issues pose challenges to designers for designing of chips in deep submicron CMOS technologies. A new strategy of switchable CMOS phase-locked loop frequency synthesizer is proposed to increase its tuning range. The switchable PLL which integrates two phase-locked loops with different tuning frequencies are designed and fabricated in 0.5 μm CMOS process to analyze the effects under HCE and NBTI.

A 3V 1.2 GHz programmable phase-locked loop frequency synthesizer is designed in 0.5 μm CMOS technology. The frequency synthesizer is implemented using LC voltage-controlled oscillator (VCO) and a low power dual-modulus prescaler. The LC

VCO working range is from 900MHz to 1.4GHz. Current mode logic (CML) is used in designing high speed D flip-flop in the dual-modulus prescaler circuits for low power consumption. The power consumption of the PLL chip is under 30mW. Fully differential LC VCO is used to provide high oscillation frequency. A new design of LC VCO using carbon nanotube (CNT) wire inductor has been proposed. The PLL design using CNT-LC VCO shows significant improvement in phase noise due to high-Q LC circuit.

CHAPTER 1

INTRODUCTION

Phase-locked loops (PLLs) have been widely used in high speed data communication systems. The design, underlying principles of operation, and applications irrespective of advances in technology are described in numerous publications and text books [1-4]. The PLL technique was first proposed as a p ractical synchronization of oscillators by Appleton [5] in 1923 and a French Scientist de Bellescise [6] in 1932. Based on the initial work, Travis [7] in 1935 addressed reasons to control the oscillation frequency of a receiver. In 1939, Rideout proposed an automatic servo system with frequency control circuits [8]. Meanwhile, the feedback control theory of the frequency synchronizing circuits was presented by Oliver [9], the analysis was achieved by Nyquist diagrams and Bode plot in control theory. Until 1970's, PLL used for frequency synthesis became available as a single chip in CMOS and other technologies advanced [10].

There are several technologies making the PLL IC chip, such as bipolar junction transistor (BJT), gallium arsenide (GaAs), bipolar CMOS (BiCMOS) and complementary metal-oxide semiconductor (CMOS) [11-15]. Now a days, the CMOS PLL circuits are widely used in digital and analog circuits in applications such as the cellular phones, microprocessors, RF front-end circuits and system-on-chip (SOC) implementations because of better performance on low power and low noise. Commercial communication systems have a rapid growth over the past decade. Most commercial communication systems operate at appropriate frequency references. A PLL frequency synthesizer, which is used to synthesize these frequency references, is able to track the phase and frequency of the system clock and to achieve a certain bandwidth with low phase noise performance. Other criteria such as the lock-in time, phase error and power consumption are also considered in a PLL design. CMOS based PLL systems are designed, analyzed

and reported in [16-23]. PLL applications as clock synthesizer in microprocessor are reported in [16-19] and PLLs in wireless transceivers are reported in [20-23].

In short channel MOS devices, the channel length is comparable with the depletion widths of the drain and source junctions. If the channel length is decreased and becomes comparable to the depletion widths, some key parameters will change. The long channel MOS transistor physics cannot be used for short channel devices [24]. Such issues include hot carrier effect (HCE) and negative bias temperature instability (NBTI). Hot carrier effect was first proposed as a reliability issue by Hu [25] and Ning *et al.* [26] in 1979. Hu [25] used the breaking bonds of SiO_2 model to physically elaborate the hot carrier effect; Ning *et al.* [26] detected the hot carrier phenomenon and analyzed hot carrier effect on a clock generator circuit under 1 μm CMOS technology. CMOS circuits' degradation by HCE was further studied and investigated by Wang [27] in 1992 and Yang [28] in 2003.

The work in this thesis is mainly focused on the studies of phase noise and jitter performances in the PLL and one of its key building blocks, the VCO. In submicron CMOS devices, the performance of integrated circuits is influenced by the hot carrier effect and negative bias temperature instability (NBTI) due to increased lateral channel electric field and results in performance degradation. Thus, jitter and phase noise may also be affected.

1.1 Phase-Locked Loop Components

The block diagram of a typical PLL is shown in Figure 1.1. There are five basic components in a PLL: phase/frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and 1/N frequency divider. The PLL operates as follows: PFD is a circuit block which detects the phase and frequency of the input

signal and compares with the phase and frequency of feedback signal and gives a switch signal to the charge pump. Charge pump is used to charge or discharge the loop filter in order to increase or decrease the control voltage which follows the PFD output. The loop filter eliminates the higher order noise and provides control voltage to VCO circuit when the switch signal is ON. VCO generates an output signal with a specific frequency related to the input signal. The divider divides the frequency of the output signal at a pre-defined fraction N and connects the feedback signal back to the PFD. The PLL is locked when the phase of input reference clock is the same as the phase of the VCO output clock. Detailed information will be provided in the following sections.

1.1.1 Phase/Frequency Detector (PFD)

Figure 1.2 shows the design of controllable D-flip-flop. The PFD built by two controllable D flip-flops and a AND gate is shown in Figure 1.3. Figure 1.4 (a) and (b) may help in better understanding the principle how PFD works (assuming divider ratio N=1 for simplicity). Figure 1.4 (a) shows the case when input reference clock has the same frequency but different phase with the VCO output clock. When the input clock rising edge is leading the VCO output clock, the UP signal will turned on and the DN signal only has positive pulses when the rising edges of input reference and VCO output clock overlap. When the input clock is lagging the VCO output clock, the DN signal will turned on and the UP signal will have low level except has positive pulses when the rising edges of VCO output and input reference clock overlap. Figure 1.4 (b) shows the case when input reference clock has different frequency but the same phase with the VCO output clock. The input reference clock is always leading the VCO output clock; therefore the DN is always low level with narrow spurs.

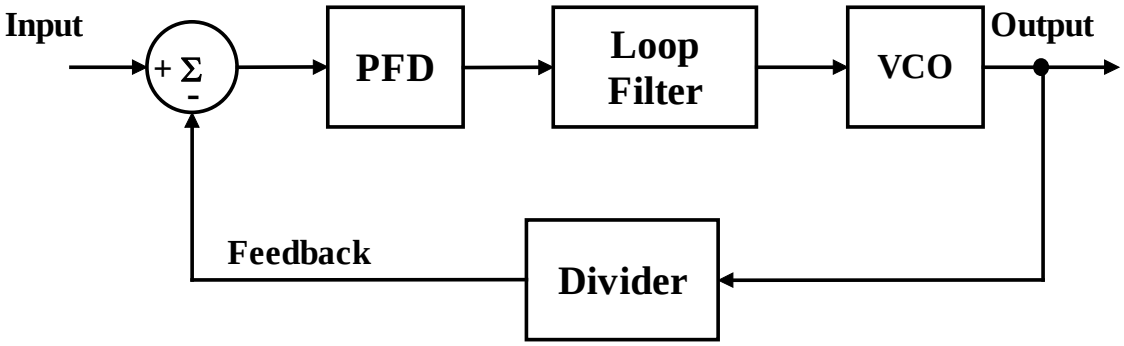


Figure 1.1: A block diagram of PLL.

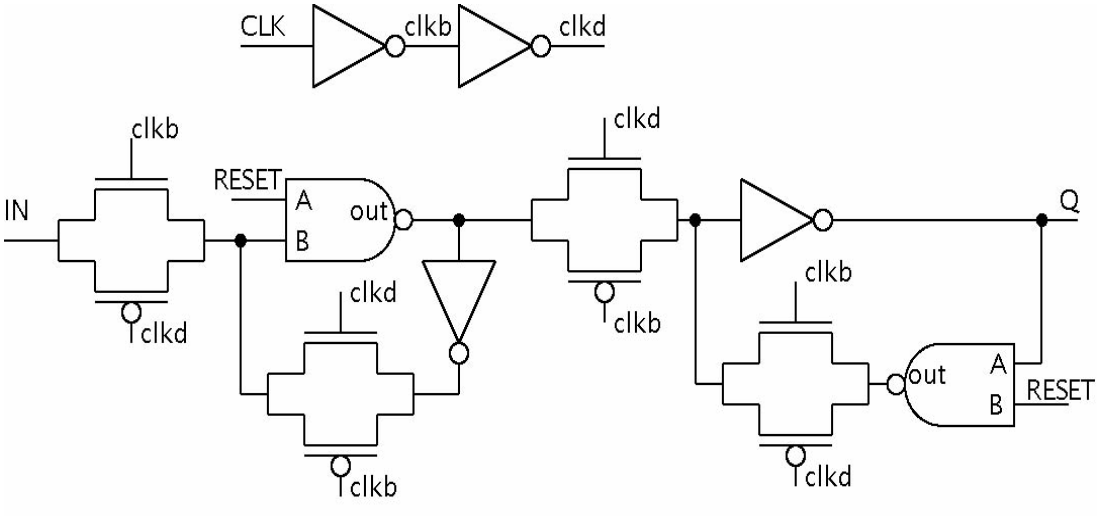


Figure 1.2: D Flip-Flop circuit diagram of a phase/frequency detector (PFD).

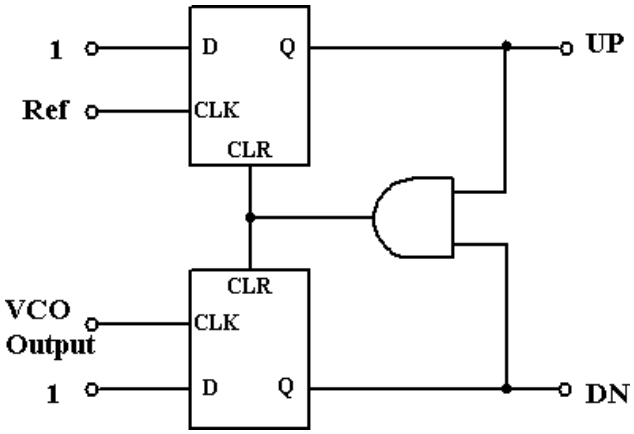
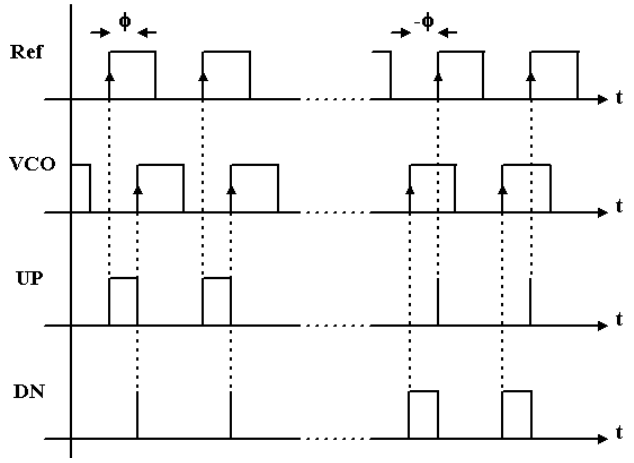
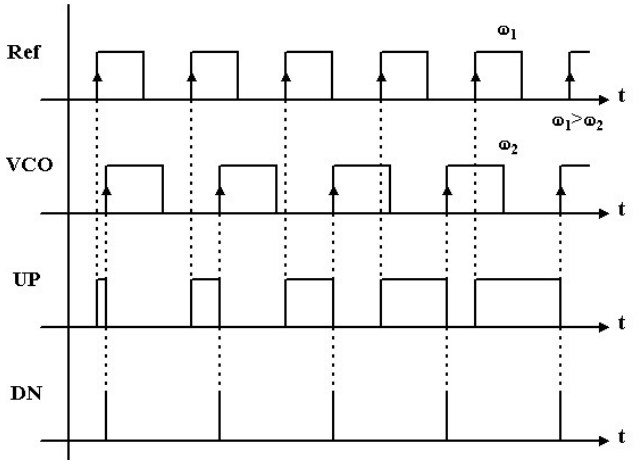


Figure 1.3: A phase/frequency detector (PFD).



(a)



(b)

Figure 1.4: PFD outputs with (a) same frequency inputs and (b) different frequency inputs.

1.1.2 Charge Pump (CP) and Loop Filter

Figure 1.5 shows the equivalent diagram of charge pump and loop filter. When PFD output UP goes high, S_1 will turn on and I_{CP} will charge the loop filter capacitor, C_1, which in turn results in an increase of the control voltage. C_2 is used to eliminate higher order noises from the PFD. The control voltage is used to adjust the VCO output frequency. On the other hand, when PFD output DN goes high, S_2 will turn on and charge pump is working in discharging mode. The current flowing into the loop filter will decrease and the control voltage will decrease too.

1.1.3 Voltage-Controlled Oscillator

The input of the VCO is usually a control voltage, V_{CTRL}, which is adjusted by the PFD and charge pump. It generates a clock signal with a certain tuning frequency. Figure 1.6 shows a diagram of single-ended current starved oscillator. M2 and M3 form an inverter, M4 and M6 are operating as a current mirror. M5 limits the current to flow into M6 and is controlled by V_{CTRL}. This VCO is achieved by charging and discharging the equivalent output capacitors of each stage in the VCO.

The single-ended VCO oscillation frequency is given by [29],

$$f = \frac{1}{\eta N(t_r + t_f)} \tag{1.1}$$

In Eq. (1), η is a constant to describe the relationship between the stage delay and the slope of the waveform. N is the number of stages in an oscillator. Rise and fall times are t_r and t_f, respectively.

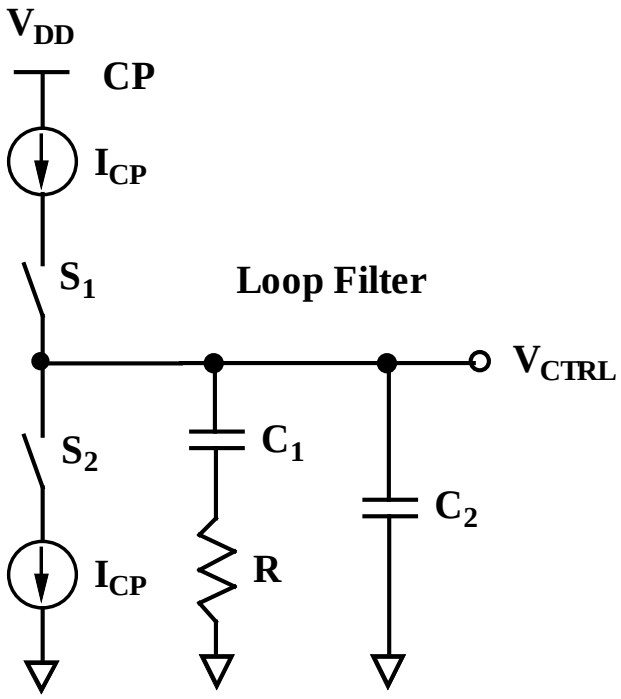


Figure 1.5: A passive loop filter following the charge pump.

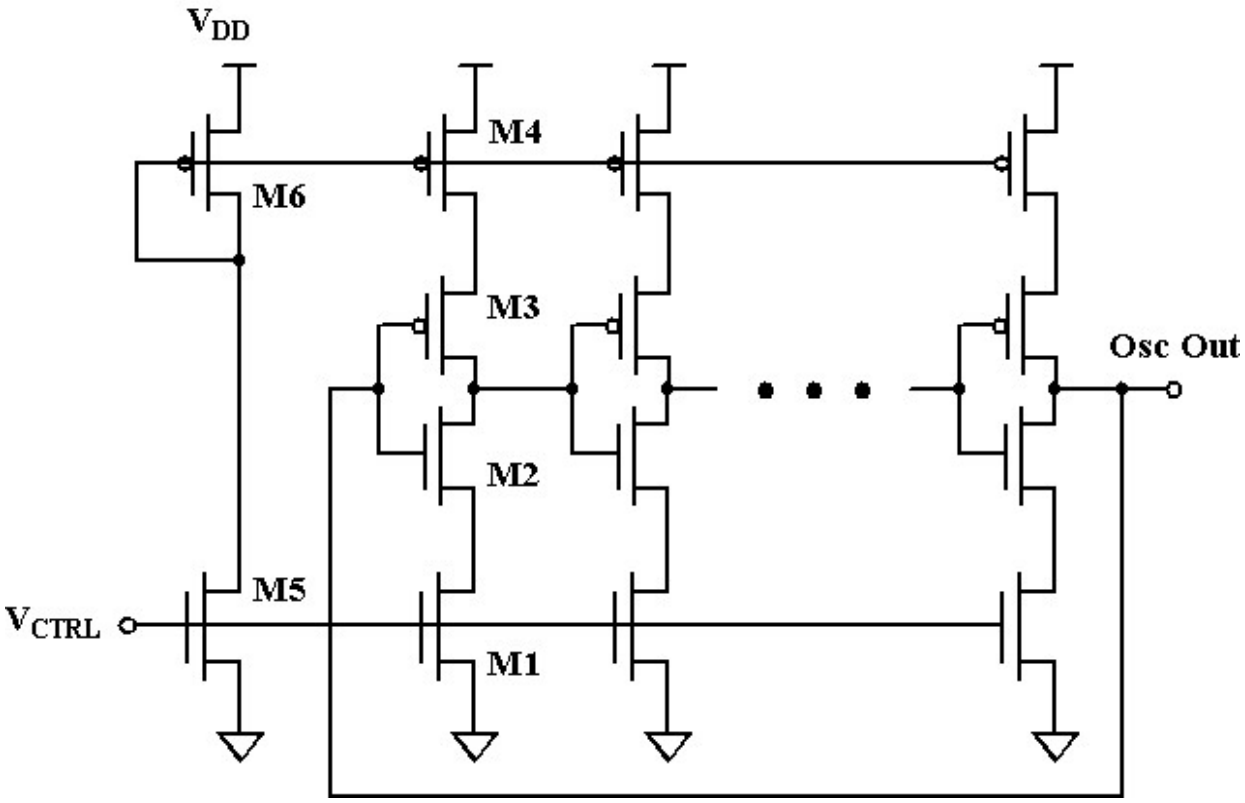


Figure 1.6: A current starved VCO circuit diagram.

Figure 1.7 shows the circuit diagram of a differential CMOS VCO. When M1 turns off and M2 turns on (*In* is logic "0" and *Inb* is logic "1"), M3 will be turned-on and M4 will be turned-off. Thus, *Outb* is "1" and *Out* is "0". Since *Outb* and *Out* are connected to *In* and *Inb* of the next stage, respectively, *In* and *Inb* will be logic "1" and "0". The oscillation frequency of differential VCO is $1/2Mt_D$, where *M* is the number of stages and t_D is the delay of the single stage.

The differential VCO oscillation frequency is given by

$$f = \frac{I_{tail}}{2\eta N q_{\max}} \tag{1.2}$$

where I_{tail} is the tail current and $q_{\max}$ is the maximum total charge stored on each node of the oscillator.

There are also other types of VCO, such as LC VCO built by using inductors and varactors and will be described in the later section.

1.2 Phase Noise and Time Jitter

1.2.1 Phase Noise

The output of a PLL is characterized by its output frequency tuning range and its frequency purity. The output of a PLL is a pure sinusoidal waveform and the power spectrum reaches a peak in the desired output frequency or called carrier frequency with no other power spectrum spread on ot her frequency. However, in reality, the output waveform deviates from the ideal position and the power spectrum reaches a peak at carrier frequency with tails on both sides which is shown in Figure 1.8. This uncertainty is characterized by phase noise in unit of *dBc/Hz*, which is measured in ratio of the phase

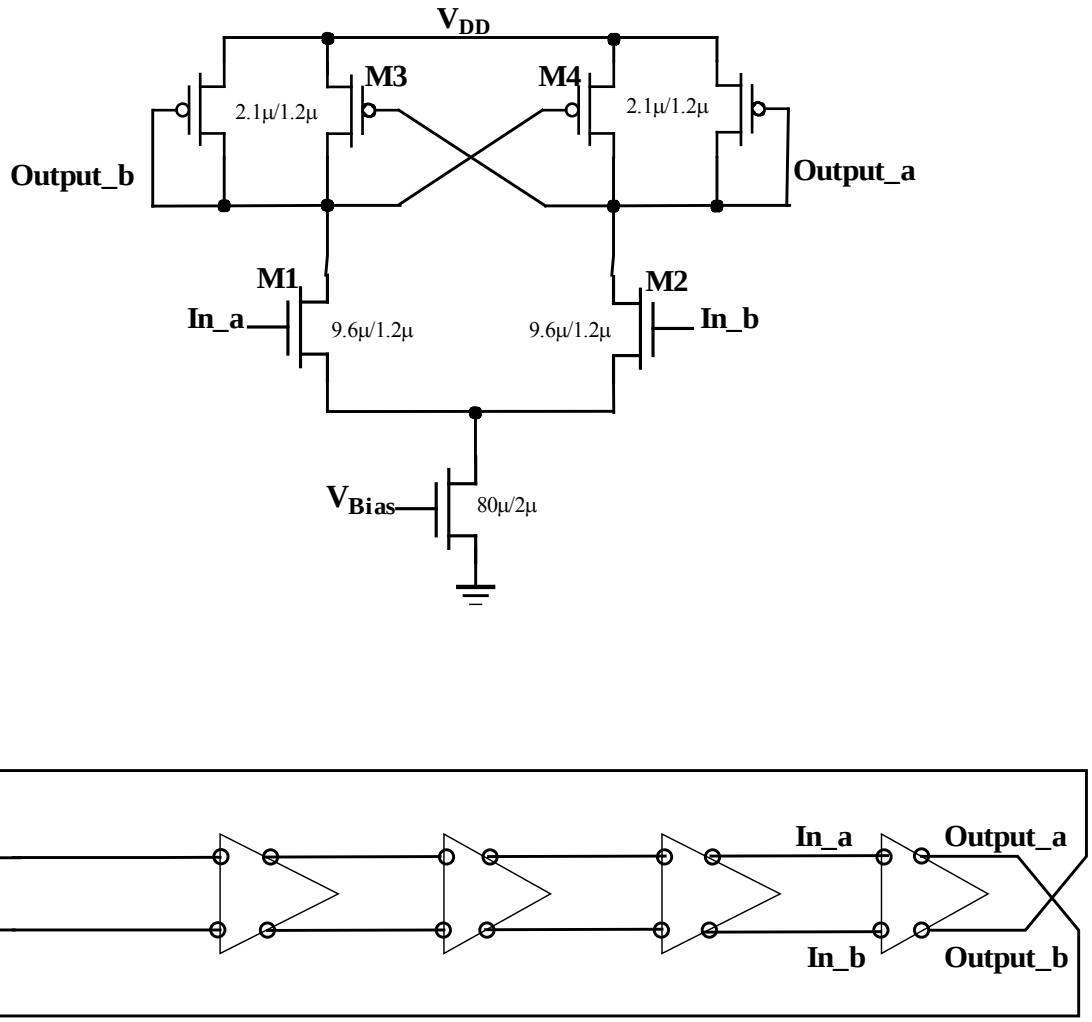


Figure 1.7: Circuit diagram of a differential ring oscillator.

noise power in 1 Hz bandwidth at a certain frequency, $f_0 + \Delta f$, offset to center frequency, f_0 .

The expression of phase noise in Figure 1.8 is shown below,

$$L_{total}\{\Delta f\} = 10\log\left[\frac{P_{noise}(f_0 + \Delta f, 1Hz)}{P_{carrier}}\right] \tag{1.3}$$

where $P_{noise}(f_0 + \Delta f, 1Hz)$ is the sideband noise power at offset frequency Δf from the carrier frequency f_0 with a measurement bandwidth of 1 Hz.

1.2.2 Time Jitter

Jitter and phase noise are different ways to express the same phenomenon [30]. Phase noise is the uncertainty of the waveform in the frequency domain and jitter is characterization in time domain of the PLL output. Jitter is the deviation of a waveform transition from its ideal position. There are mainly three types of time jitters [31]:

(1) The cycle jitter is defined as

$$\Delta T_{cn} = T_n - \overline{T} \tag{1.4}$$

where T_n is the time of the *n* th cycle of the output waveform. $\overline{T}$ is the average period.

(2) The cycle-to-cycle jitter is defined as,

$$\Delta T_{ccn} = T_{n+1} - T_n \tag{1.5}$$

(3) The accumulated jitter is defined as,

$$(4)\ \Delta T_{acc} = \sum_{n=1}^{N}(T_n - \overline{T}) \tag{1.6}$$

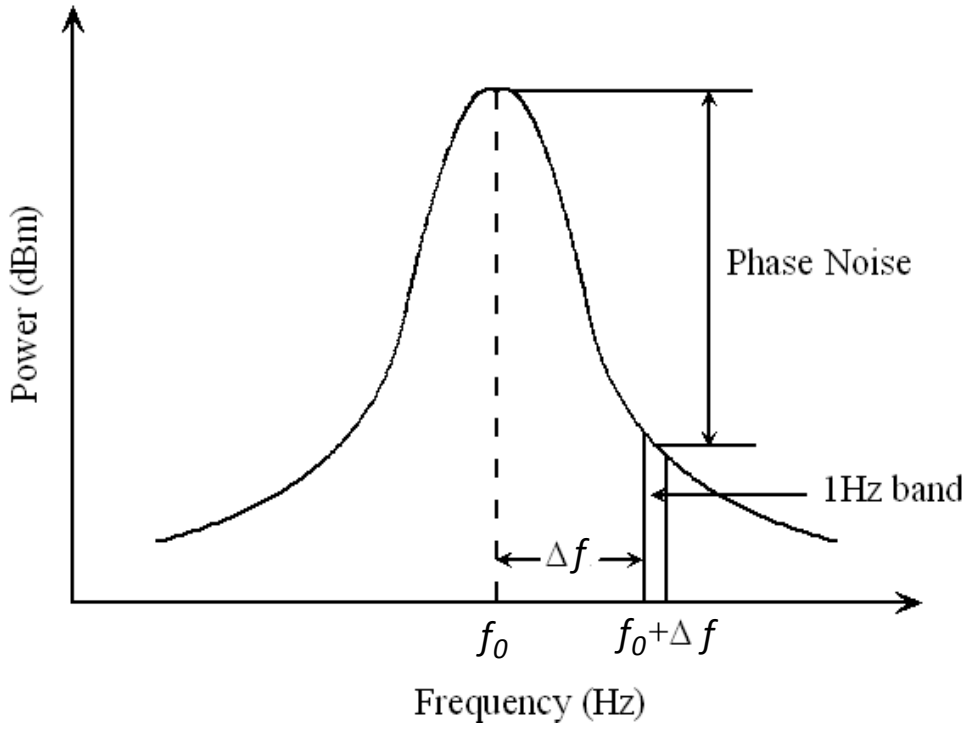


Figure.1.8: Oscillator power spectrum with phase noise at an offset frequency Δf .

where N is the N^{th} cycle of the waveform. This accumulated jitter is characterized and increased by time interval, ΔT, which is the time difference between the reference and the observed transitions during the measurement, as shown in Fig. 1.9. In jitter measurement, The RMS (root mean-squared) jitter in Eq. (1.6), which is the value of one standard deviation of the normal distribution, is more useful because this value changes not much as the number of samples increases.

1.3 Hot Carrier Effect (HCE) and Negative Bias Temperature Instability (NBTI)

1.3.1 Hot Carrier Effect (HCE)

As device size shrinks and channel electric field increases, interface and oxide traps play important roles affecting the performances of devices and thus the reliability. In CMOS circuits designed in sub-micron/deep-submicron CMOS technologies, HCE and NBTI are well known to be the critical reliability issues.

MOSFET degradation due to HCE is caused by the generation of acceptor-type interface traps. The interface traps are located in the channel and the narrow band near the drain. In an n-MOSFET, when the voltage at the drain and gate is large, electrons gain the energy over 3.7 eV [32], the interface traps are generated by breaking silicon-hydrogen bonds and electrons diffuse away from the interface. The electrons which the channel are called channel hot electrons. The electrons which diffuse from the drain are called drain avalanche hot electrons. The carrier mobility and density are reduced due to interface traps and threshold voltage increases. This mechanism is shown in Figure 1.10. Threshold voltage and electron mobility are affected by this kind of generation at the drain end of MOSFETs. The interface traps are generated by the breaking of silicon-hydrogen bonds $\equiv Si_s H$. The $\equiv Si_s H$ bond is broken by hot electrons. Interstitial

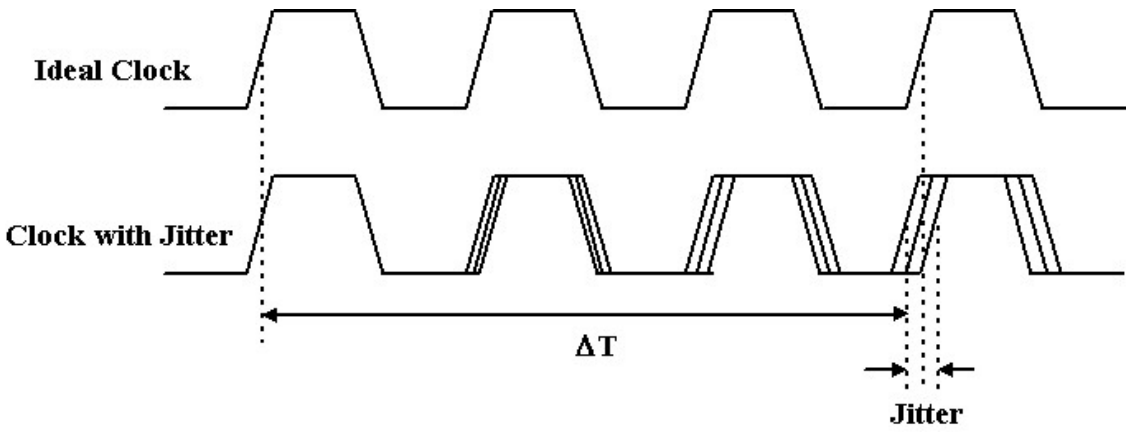


Figure 1.9: Clock jitter increases with the measurement interval, ΔT .

hydrogen atom H_i and trivalent silicon S_i^* are produced which form interface traps. Following Eq. (1.6) shows this phenomenon.

$$\equiv Si_s H \xleftrightarrow{e^-} S_i^* + H_i \tag{1.7}$$

Figure 1.11 shows the physical model for the secondary generation hot carrier injection with high electric field; the generated hot carriers can cause secondary impact ionization in the depletion region and diffuse away from channel to substrate [33].

1.3.2 Negative Bias Temperature Instability (NBTI)

NBTI degradation which occurs mainly in p-MOSFETs under the negative gate-source voltage bias, reported in 1966 by Goetzberger and Nigh [34] and results in shift in threshold voltage [35]. The NBTI effect is caused by the decrease of the MOSFET gate oxide thickness [36].

NBTI causes an increase in the threshold voltage, hole mobility, transconductance and drain current in p-MOSFETs. Among various NBTI models, The *Reaction-Diffusion* (R-D) model is the dominant one [37]. This model has two phases. In the reaction phase, NBTI is caused by the creation of SiO_2/Si interface traps and hydrogen is generated during this mechanism.

where SiH is the silicon-hydrogen bond at Si/SiO_2 interface. In Eq. (1.8), e^+ is the hole traps at the interface and Si^+ is the interface trap.

The generation of interface traps is given by [39],

$$\Delta N_{it}(t) = \frac{2k_F N_0 t}{1+\sqrt{\frac{1+4k_F N_0 k_R t^{3/2}}{0.5\sqrt{D_H}}}} \tag{1.9}$$

In the diffusion phase, the generated hydrogen diffuses into the substrate. The generation of interface traps is described as follows [38],

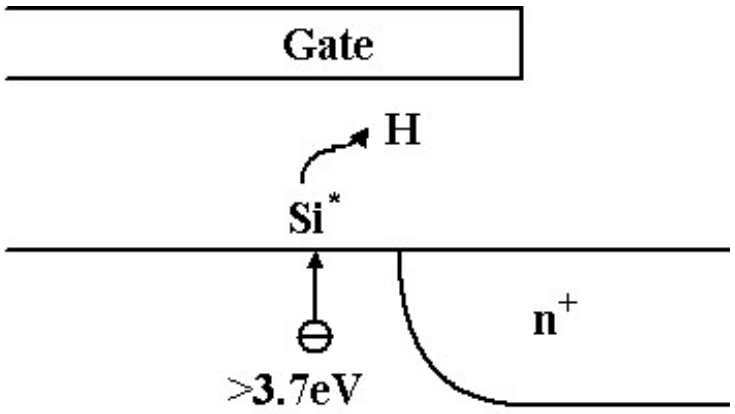


Figure 1.10: A physical model for interface-traps generation of hot carrier injection (HCI).

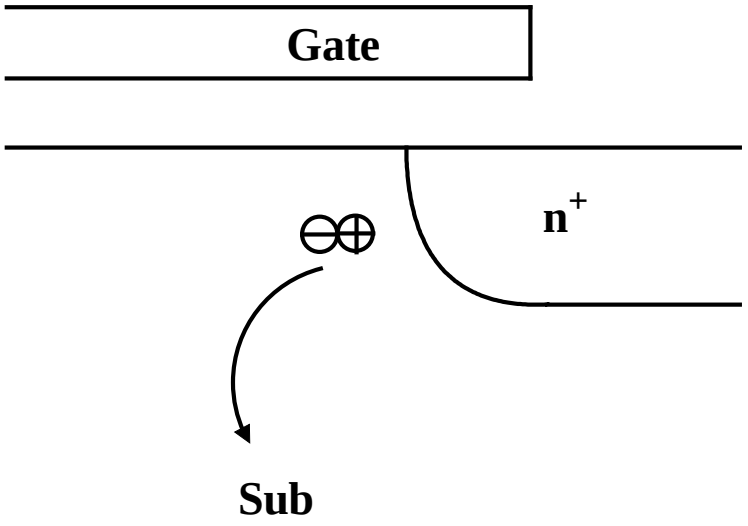


Figure 1.11: A physical model for Secondary generated hot carrier injection (HCI).

$$SiH + e^{+} \leftrightarrow Si^{+} + H \tag{1.8}$$

where k_F is the forward reaction rate, k_R is the reverse reaction rate, N_0 is the initial defect density, D_H is the hydrogen diffusion coefficient and t is the NBTI stress time. The NBTI effect is shown in Figure 1.12.

Both n- and p-MOSFETS have been extensively characterized under HCE and NBTI and their influences on analog and digital CMOS circuits have also been addressed [40-44]. However, there is no reported work on combined effects of HCE and NBTI on the performance of phase-locked loop circuits. In the present work, an attempt has been made to study combined effects of HCE and NBTI on the performance of the PLL circuits used for communication systems.

1.4 Goals and Objectives

In this research, it is proposed to study noise in CMOS phase-locked loop systems and building blocks based on MOS device physics. Earlier work done by Zhang [29] in our research group on explaining phase noise from HCE on VCO will be extended to all building blocks of PLL and include effect of NBTI. The final goal is to develop a comprehensive phase noise model of a PLL. Research of some of the studies conducted is described in following chapters.

Chapter 2 discusses the hot carrier effect on both single-ended VCO and differential VCO. Two VCO circuit designs with hot carrier injection modes are presented. Degradation models on phase noise and jitter degradation on different types of VCOs are illustrated. Both hot carrier and NBTI models of the PLL chip are presented in this chapter. Transistor level single-ended and differential ended types VCO are shown in this chapter.

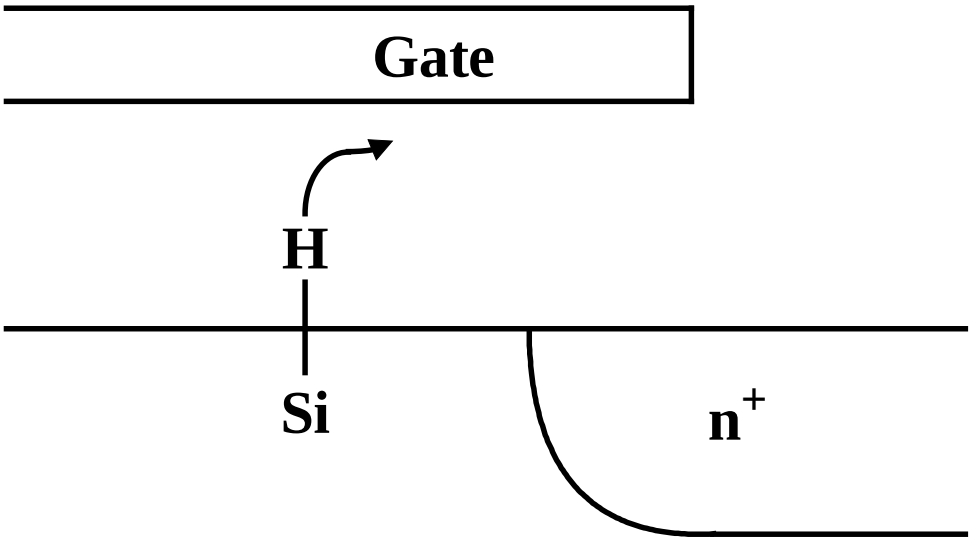


Figure 1.12: A physical model for interface-traps generation of NBTI.

Chapter 3 extends the noise studies of VCO and PLL discussed in Chapter 2. The circuit diagrams and chip layout of the PLL frequency synthesizer are given. A second-order linear time invariant model with additive noise sources in frequency domain is presented to analyze the phase noise. The modeled phase noise results are compared with the corresponding experimentally measured results on a phase-locked loop chip fabricated in 0.5 μm n-well CMOS process.

Chapter 4 discusses a new design of switchable PLL frequency synthesizer with dual phase-locked loops. The circuit design schematics and the chip layout of the switchable PLL frequency synthesizer are proposed and the phase noise and jitter measurement setups are given. Both simulation of measurement results of hot carrier and NBTI effects on tuning frequency range, phase noise and jitter have been investigated.

Chapter 5 discusses a programmable PLL frequency synthesizer. The frequency synthesizer is implemented by LC VCO and a low power dual-modulus prescaler. Current mode logic (CML) technique is used to design high speed D flip-flop in the dual-modulus prescaler circuits. A MOSFET varactor degradation model due to hot carrier effects has been used to analyze oscillation frequency and phase noise performance. NBTI effect is studied to analyze the output voltage swing and phase noise degradations of the LC VCO.

Chapter 6 presents a new type of LC VCO where a typical on-chip metallic inductor is replaced by a multi-walled carbon nanotube wire inductor. The oscillation frequency and phase noise performance of CMOS LC VCO based PLL design are studied and the performances using MWCNT based inductor and Cu inductor as a function of quality factor (Q) are compared. The MOS model parameters used in Cadence/Spectre

simulations for 0.5 μ m and 0.18 μ m n-well CMOS technologies are summarized in Appendix A. The list of papers published is presented in Appendix B.

CHAPTER 2

PHASE NOISE AND JITTER STUDY IN CMOS VOLTAGE-CONTROLLED OSCILLATOR (VCO) CONSIDERING HOT CARRIER EFFECTS*

Phase-locked loops (PLLs) have been widely used in high speed data communication systems. The design, underlying principles of operation and applications are described in numerous publications and text books [45, 46]. With the increase in operation frequency of systems, jitter or phase noise issue in PLL has become the cause of serious concern in digital communication systems. The noise sources in PLL originate mainly from its building blocks: the voltage-controlled oscillator, frequency divider, phase-frequency detector, loop filter and auxiliary input reference clock. Noise studies for each one of these building blocks have been reported in [47-49]. Hajimiri and his co-workers [47, 48] have studied phase noise and jitter in oscillator circuits. Llopis et al. [49] have studied phase noise in frequency dividers up to microwave frequency range. In another work, Hajimiri [50] presented linear time invariant (LTI) models of VCO and frequency divider building blocks of a PLL. However, noise from other parts of the PLL such as the phase detector is considered to be not a major source of noise.

The noise in PLL has also been investigated in [51-53] due to different building blocks. Kroupa [51] presented a detailed review of all the major sources of additive noises in a PLL. However, no specific technology used in design of low-noise PLL is described. Lagutere et al. [52] have used VHDL-AMS for modeling phase noise in VCO and PLL as

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* Part of the work is reported in the following publications:

1. Y. Liu and A. Srivastava, "Hot carrier effects on CMOS phase-locked loop frequency synthesizers," *Proc. International Symposium on Quality Electronic Design (ISQED)*, pp. 92-98, March. 22-24, 2010.
2. Y. Liu and A. Srivastava, "Effect of hot carrier injection and negative bias temperature instability on the performance of CMOS phase-locked loops," *Proc. 2010 ASEE-GSW Annual Conference*, Mar. 24-26, 2010.

a whole and compared modeled phase noise with the measured values. However, the modeled noise requires adjustment in parameters to fit the measured results. Mehrotra [53] has presented noise analysis based on non-linear model of a PLL with the divider ratio set as one. Furthermore, the non-linear model is compared with the measured power spectral density (PSD) of PLL from the work of Parker and Ray [54] and agrees closely to the shape rather than values. Recently, Sangha and Hoffmann [55] presented a technique using MATLAB/SIMULINK to analyze the noise behavior of a second-order PLL by injecting noises at the input reference, phase-detector and in the control filter. Their work is focused mainly at the system level and does not relate to actual CMOS circuit level implementation.

Though the phase noise in PLL has been widely studied but is still an open subject for theoretical research as mentioned by Gardener [45]. However, there is not much reported work on the experimental study of total phase noise in PLL contributing from its building blocks at the circuit level. In the present work, an attempt has been made to experimentally measure the phase noise in a second-order PLL designed and fabricated in 0.5 μm n-well CMOS and co-relate with a linear time-invariant close loop transfer function. In Section 2.1, phase noise calculations of different circuit level building blocks are presented and a superposition method is described to calculate the total PLL output phase noise. In Section 2.2, models of hot carrier effect and negative bias temperature instability for VCO are described and studied. An experimental study of phase noise is described in Section 2.3 followed by conclusions in Section 2.4. `

2.1 Phase Noise in PLL

To investigate the loop dynamics of a PLL, a block diagram is very useful, which is shown in Figure 2.1. $\Phi_{in}(s)$ and $\Phi_{out}(s)$ are the input reference phase and VCO

output phase, respectively. $\Phi_e(s)$ is the phase error between $\Phi_{in}(s)$ and $\Phi'_{out}(s)$ which is the phase of feedback signal from the divider output. A phase/frequency detector and charge pump (CP) are characterized with current gain, K_P. The gain of PFD is $K_p = I_{CP}/2\pi$ where I_{CP} is the current of the charge pump. The loop filter has a transfer function, *F(s)*.

The VCO gain and tuning voltage are defined as K_V and V_{ctrl} , respectively. The transfer function of VCO is $2\pi K_v / s$. Since frequency is the derivative of phase with respect to time, $d\Phi_{out}(t)/dt = K_V V_{ctrl}(t)$ or $\Phi_{out}(s) = V_{ctrl}(s)K_V / s$ in frequency domain.

The characteristics of a second-order PLL can be analyzed by the linear time-invariant (LTI) model. The open loop transfer function of the loop filter in Figure 1.5 is given by,

$$F(s) = \frac{(1 + RC_1 s)}{C_1 s + C_2 s + RC_2 C_1 s^2} \tag{2.1}$$

Disconnecting the loop between the VCO output and PFD, the PLL open loop transfer function is given by,

$$G(s) = I_{CP} \cdot F(s) \cdot K_v / s \tag{2.2}$$

The PLL closed loop transfer function can then be expressed as follows:

$$H(s) = \frac{G(s)}{1 + G(s)/N} \tag{2.3}$$

In Eq. (2.3), *N* is the divider ratio. There are two poles from the loop filter and one single pole from the VCO in Eq. (2.3) which characterizes the second-order PLL.

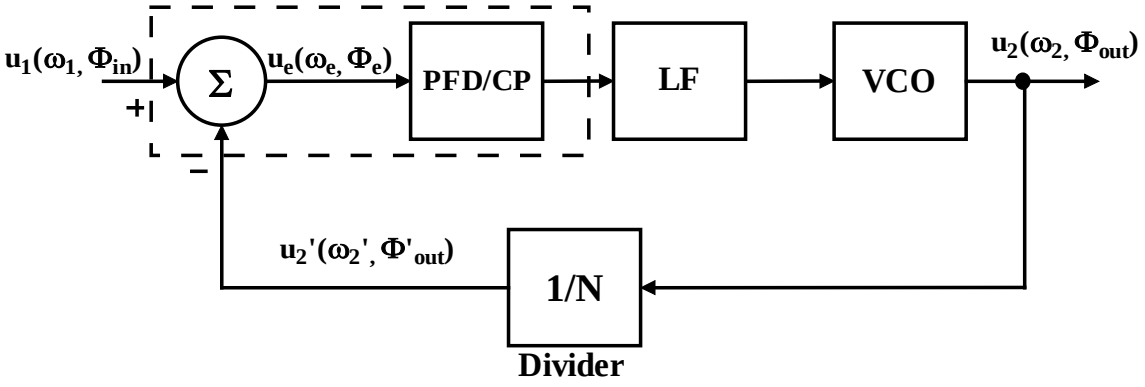

Figure 2.1: A phase domain block diagram of PLL.

Figure 2.2 shows the equivalent frequency domain model of PLL with injected noise sources. In Fig. 2.2, $n_{vco}(s)$, $n_{input}(s)$, $n_d(s)$, $n_{pfdcp}(s)$ and $n_{lf}(s)$ are the equivalent

injected noises at the output of VCO, the input, output of divider, output of PFD and output of loop filter, respectively.

2.1.1 Phase Noise Modeling of Differential VCO

Assuming a noisy VCO dominated by its white and $1/f$ noises and no other injected noises, the closed loop transfer function of the VCO phase noise can be calculated using the noise transfer function from $n_{vco}(s)$ to $\Phi_{out}(s)$, which is given by,

$$\frac{\Phi_{out}(s)}{n_{vco}(s)} = \frac{1}{1+G_{vco}(s)H_{vco}(s)} = \frac{1}{1+(2\pi K_v/s)\cdot(1/N)K_pF(s)} \tag{2.4}$$

where $G_{vco}(s)$ is the open loop transfer function from VCO noise injection, $n_{vco}(s)$ to VCO output terminal. $H_{vco}(s)$ is the feedback transfer function from PLL output to $n_{vco}(s)$. Therefore, the power spectral density of the output phase noise can be obtained as follows,

$$S_{\Phi outVCO}(\omega) = S_{\Phi inVCO}(\omega)\frac{\left|\Phi_{out}(j\omega)\right|^2}{\left|n_{vco}(j\omega)\right|^2} \tag{2.5}$$

In Eq. (2.5), ω is the offset frequency in *rad/s*. $S_{\Phi outVCO}(\omega)$ and $S_{\Phi inVCO}(\omega)$ are the power spectral density of VCO closed and open loop phase noise, respectively. $S_{\Phi inVCO}(\omega)$ and $S_{\Phi outVCO}(\omega)$ in Eq. (2.5) are expressed in rad^2/Hz. In measurements, it is expressed in *dBc/Hz*. The PSD measurement with a power meter includes a narrowband bandpass filter. The unit rad^2/Hz can be converted to a PSD unit *dBc/Hz* as follows [46],

$$S_{dB}(f) = 10\log[S_{rad}(f)] \tag{2.6}$$

In Eq. (2.6), $S_{dB}(f)$ and $S_{rad}(f)$ are the power spectral densities of phase noise at anoffset frequency, f in *dBc/Hz* and rad^2/Hz, respectively. Both $S_{dB}(f)$ and $S_{rad}(f)$

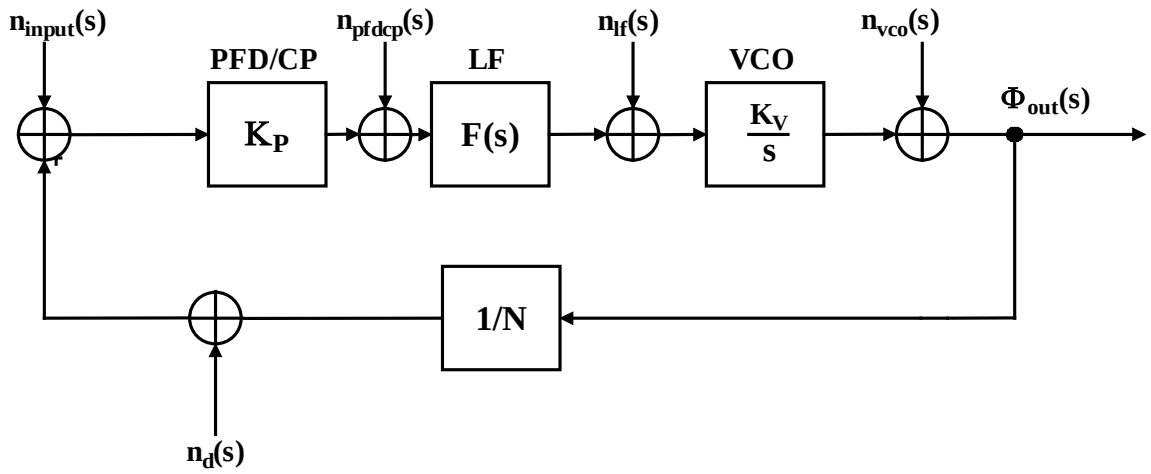

Figure 2.2: Equivalent frequency domain model of a PLL with injected noise sources.

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define the value of the noise power stored within a bandwidth of 1 *Hz* below the power of the carrier.

2.1.2 Phase Noise Modeling of Input Reference Clock

Assuming a noisy input signal, the response of the loop to the phase variations in the input can be evaluated using a similar method described in Section 2.1.1. For the PLL under consideration, the input noise transfer function is given by,

$$\frac{\Phi_{out}(s)}{n_{input}(s)} = \frac{G_{in}(s)}{1+G_{in}(s)H_{in}(s)} = \frac{(2\pi K_v / s)K_p F(s)}{1+(2\pi K_v / s)\cdot(1/N)K_p F(s)} \tag{2.7}$$

where $G_{in}(s)$ is the open loop transfer function from reference clock noise injection, $n_{input}(s)$ to PLL output terminal. In Eq. (2.7), $H_{in}(s)$ is the feedback transfer function from PLL output to $n_{input}(s)$ in Figure 2.2. The output phase noise power spectrum of input reference phase noise is given by,

$$S_{\Phi outINPUT}(\omega) = S_{\Phi inINPUT}(\omega)\frac{\left|\Phi_{out}(j\omega)\right|^2}{\left|n_{input}(j\omega)\right|^2} \tag{2.8}$$

2.1.3 Phase Noise Modeling of the Divider

The frequency divider introduces additive noise by white and $1/f$ noises. The additive noise is injected at the input of the PFD and share the same transfer function as the noise at the input terminal. Similarly, the noise transfer function for divider can be described as follows,

$$\frac{\Phi_{out}(s)}{n_d(s)} = \frac{G_d(s)}{1+G_d(s)H_d(s)} = \frac{(2\pi K_v / s)K_p F(s)}{1+(2\pi K_v / s)\cdot(1/N)K_p F(s)} \tag{2.9}$$

and

$$S_{\Phi outD}(\omega) = S_{\Phi inD}(\omega)\frac{\left|\Phi_{out}(j\omega)\right|^2}{\left|n_d(j\omega)\right|^2} \tag{2.10}$$

In Eq. (2.9), $G_d(s)$ is the open loop transfer function from divider noise injection, $n_d(s)$ to PLL output terminal and $H_d(s)$ is the feedback transfer function from PLL output to $n_d(s)$. In Eq. (2.10), $S_{\Phi inD}(\omega)$ is the open loop PSD.

2.1.4 Phase Noise Modeling of PFD/CP

Noises injected by PFD are $1/f$, substrate and supply noises. Similarly, noise model for PFD can be expressed by the following equations,

$$\frac{I_{out}(s)}{n_{pfdcp}(s)} = \frac{G_{pfdcp}(s)}{1+G_{pfdcp}(s)H_{pfdcp}(s)} = \frac{(2\pi K_v/s)\cdot F(s)}{1+(2\pi K_v/s)\cdot(1/N)K_p F(s)} \tag{2.11}$$

and

$$S_{\Phi outPFDCP}(\omega) = S_{\Phi inPFDCP}(\omega)\frac{\left|\Phi_{out}(j\omega)\right|^2}{\left|n_{pfdcp}(j\omega)\right|^2} \tag{2.12}$$

In Eq. (2.11), I_{out} is the output current of charge pump, $G_{pfdcp}(s)$ is the open loop transfer function from PFD/CP noise injection, $n_{pfdcp}(s)$ to PLL output terminal. $H_{pfdcp}(s)$ is the feedback transfer function from PLL output to $n_{pfdcp}(s)$ which is shown in Figure 2.2. In Eq. (2.12), $S_{\Phi inPFDCP}(\omega)$ is the open loop phase noise PSD.

2.1.5 Phase Noise Modeling of Loop Filter

Noise model for the loop filter can also be described by the following equations,

$$\frac{V_{out}(s)}{n_{lf}(s)} = \frac{G_{lf}(s)}{1+G_{lf}(s)H_{lf}(s)} = \frac{(2\pi K_v/s)}{1+(2\pi K_v/s)\cdot(1/N)K_p F(s)} \tag{2.13}$$

and

$$S_{\Phi outLF}(\omega) = S_{\Phi inLF}(\omega)\frac{\left|\Phi_{out}(j\omega)\right|^2}{\left|n_{lf}(j\omega)\right|^2} \tag{2.14}$$

In Eq. (2.13), $G_{lf}(s)$ is the open loop transfer function from loop filter noise injection, $n_{lf}(s)$ to PLL output terminal and $H_{lf}(s)$ is the feedback transfer function from PLL output to $n_{lf}(s)$. In Eq. (2.14), $S_{\Phi inLF}(\omega)$ is the open loop PSD of loop filter only.

In Eqs. (2.5), (2.8), (2.10), (2.12) and (2.14), the input phase noise power spectral densities are experimentally measured in *dBc/Hz* and converted in units of rad^2/Hz using Eq. (2.6). The total phase noise PSD (rad^2/Hz) of the PLL output is then obtained by summing the output phase noises (rad^2/Hz) for a noisy VCO, a noisy input reference clock, a noisy divider, a noisy PFD and a noisy loop filter. Note that the frequency divider increases the phase noise of the input by a factor of $20\log(N)$ which is to be considered. Since the input phase variations are multiplied by N at the output, the noise spectrum of the output will increase N^2 times the input. This causes $20\log(N)$ to be added into the total PLL output phase noise.

2.2 Hot Carrier Effect (HCE) and Negative Bias Temperature Instability (NBTI) Model

2.2.1 HCE and NBTI Models for Single-ended VCO

Figure 2.3 is a current starved single-ended VCO with HCE and NBTI modes. In "normal mode" the VCO is in the oscillation mode with no HCE and NBTI. In "HCE mode", VCO is under hot carrier injection and drain of n-MOSFETs (M1- M3) in the ring oscillator are stressed from $V_{HCE\ Stress}$ = 5V. In "NBTI mode", the gates of p-MOSFETs (M4- M6) are under 0V bias and the sources of p-MOSFETs (M4-M6) are under 5V bias. It is to be mentioned that the oscillator is not working when it is subjected to either HCE or NBTI modes.

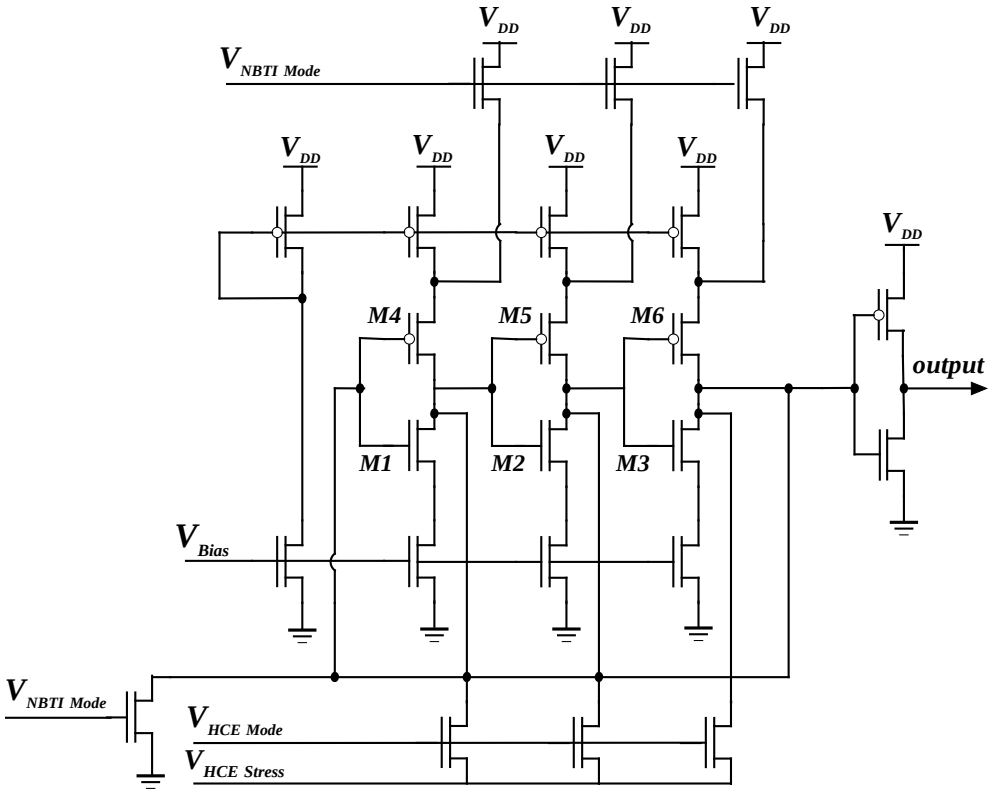

Figure 2.3: The single-ended current starved VCO with HCE and NBTI modes.

Single-ended VCO can achieve larger frequency swing, higher modulation sensitivity and is more capable for wide-band operation than the differential VCO. The gain of VCO output frequency is given by,

$$K_V = \frac{\partial f}{\partial V_{BIAS}} = \frac{\mu \cdot C_{OX}}{n} \cdot \frac{W}{L} \cdot \frac{V_{BIAS} - V_{th}}{C_L \cdot V_{DD}} \tag{2.15}$$

where C_{OX} is gate oxide capacitance per unit area, W/L is the channel width to length ratio of n-MOSFET, which decides the frequency of VCO output. V_{BIAS} is the bias voltage and V_{th} is the threshold voltage.

The single-ended VCO oscillation frequency is given by,

$$f = \frac{1}{\eta N (t_r + t_f)} \approx \frac{\mu W C_{OX} \Delta V}{8 \eta N L q_{\max}} \tag{2.16}$$

$$\Delta V = V_{DD} / 2 - V_{th} \tag{2.17}$$

In Eq. (2.16), η is a constant describing the relationship between the stage delay and the slope of the waveform which is 0.75 for 0.5 μm CMOS process. N is the number of stages in an oscillator which is 3 in this design, μ is the electron mobility, W and L are channel width and channel length of the transistor M1-M3 in Figure 2.3. The total charge in each node of the oscillator is q_{max}. Rise and fall times are t_r and t_f, respectively. The gate overdrive voltage is ΔV.

Under hot carrier injection, ΔV changes and is expressed as follows,

$$\Delta V = V_{DD} / 2 - V_{th} - \Delta V_{th} \tag{2.18}$$

where ΔV_{th} is the threshold voltage shift.

The accumulated jitter in a single-ended VCO can be modeled and calculated as follows. $\sigma_{\Delta t}$ represents the jitter and is a function of Δt, the delay between the signal input of the oscilloscope and the trigger input. $\sigma_{\Delta t}$ is given by [29],

$$\sigma_{\Delta t} = \kappa\sqrt{\Delta t} \tag{2.19}$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}}\sqrt{\frac{kT}{P}\frac{V_{DD}}{V_{char}}} \tag{2.20}$$

where κ is the jitter proportionality constant. T is the temperature. V_{char} is the characteristic voltage of the MOSFETs and is given by,

$$V_{char} = \Delta V / \gamma \tag{2.21}$$

In Eq. (2.21), γ is the noise ratio between the saturation and linear regions and numerical value for a short channel device is 4/3 [29].

VCO phase noise presents the variation of the original signal in a frequency domain. The equation below shows the phase noise performance of a CMOS single-ended VCO [29],

$$L\{\Delta f\} \approx \frac{8kTV_{DD}}{3\eta PV_{char}}\frac{f_0^{\,2}}{\Delta f^{\,2}} \tag{2.22}$$

In Eq. (2.22) Δf is the offset frequency from the carrier. P is the power dissipation and is expressed as follows,

$$P = NI_D V_{DD} \tag{2.23}$$

where I_D is the drain current in each stage.

NBTI results in the shift in threshold voltage which can be modeled by the following expression [56],

$$\Delta V_t = A\exp(\beta V_{gs} - \frac{E_a}{kT})t^n \tag{2.24}$$

where β, E_a and n are constants and described in [56].

2.2.2 HCE Models for Differential VCO

Figure 2.4 shows the circuit diagram of a differential CMOS VCO. When M1 turns off and M2 turns on (*In_a* is logic "0" and *In_b* is logic "1"), M3 will be turned-on and M4 will be turned-off. Thus, *Output_b* is "1" and *Output_a* is "0". Since *Output_b* and *Output_a* are connected to *In_a* and *In_b* of the next stage, respectively, *In_a* and *In_b* will be logic "1" and "0". The oscillation frequency of differential VCO is $1/2Mt_D$, where *M* is the number of stages and t_D is the delay of the single stage.

The differential VCO oscillation frequency is given by [57],

$$f = \frac{I_{tail}}{2\eta N q_{\max}} \tag{2.25}$$

where I_{tail} is the tail current in each stage. The expressions for κ and phase noise are as follows,

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \sqrt{N \frac{kT}{P} \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L + I_{tail}}\right)} \tag{2.26}$$

$$L\{\Delta f\} \approx \frac{8NkTV}{3\eta P} \frac{f_0^{\,2}}{\Delta f^{\,2}} \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}}\right) \tag{2.27}$$

where R_L is the effective load resistance.

The oscillation frequency and jitter/phase noise under the hot carrier injection can be modeled by varying the value of threshold voltage from equations above.

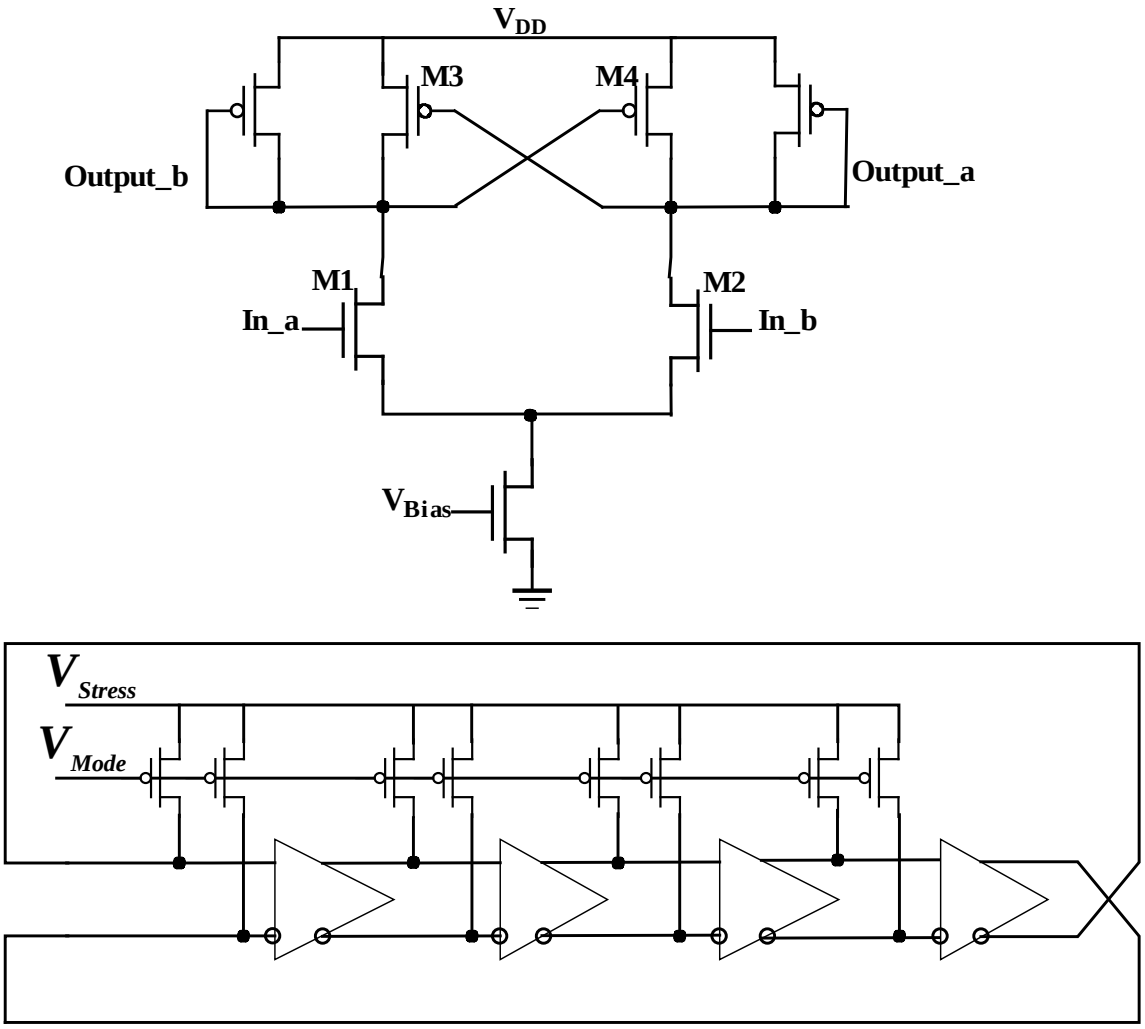

Figure 2.4: Differential VCO with hot carrier stress mode.

2.3 Experimental Study

A second-order passive loop filter is designed as shown in Figure 2.5 with PFD. The PFD is built from two controllable D flip-flops. Compared with that using logic gates, it is faster and simpler for an IC chip design.

Figure 2.6 shows the layout design of PLL circuit in 0.5 μm n-well CMOS process. PLL and its open loop building blocks are labeled in Figure 2.6. The designed loop parameters of the fabricated PLL chip are: divider ratio, $N = 8$, charge pump current, $I_{CP} = 30\mu A$, loop filter components: $R = 41.5k\Omega$, $C_1 = 43.3pF$ and $C_2 = 100\,fF$, VCO gain $K_V = 30MHz/V$. The loop bandwidth is 800 kHz. The locking range is 80 MHz-120 MHz and locking time is $1.3\mu s$. The steady-state phase error of the synchronized loop is 3 ns when the PLL is working at 80 MHz. In the layout design, the separate building blocks of PLL: PFD, loop filter, VCO and divider are included in order to experimentally measure the open loop phase noise power spectrum in *dBc/Hz*. These are exactly the same CMOS circuits integrated in the PLL and subjected to same operating conditions. For instance, the PLL input is set at 10 MHz and output signal is obtained at 80 MHz; the VCO bias voltage is set at 1.9 V by the charge pump and loop filter; the divider divides the signal from 80 MHz to 10 MHz. For open loop measurements, a 10 MHz reference clock is connected to the spectrum analyzer to measure open loop phase noise; 1.9V dc voltage is given to control the open loop VCO; a noise filtered 80 MHz input signal is given to the open loop divider. Thus, open loop phase noise can be measured on these individual PLL building blocks which make it possible to determine closed loop phase noises. Since the closed loop phase noises of individual blocks are the only noise contribution of each component to the PLL output and without noises from other components, these closed loop phase noises cannot be measured in a real chip. When a

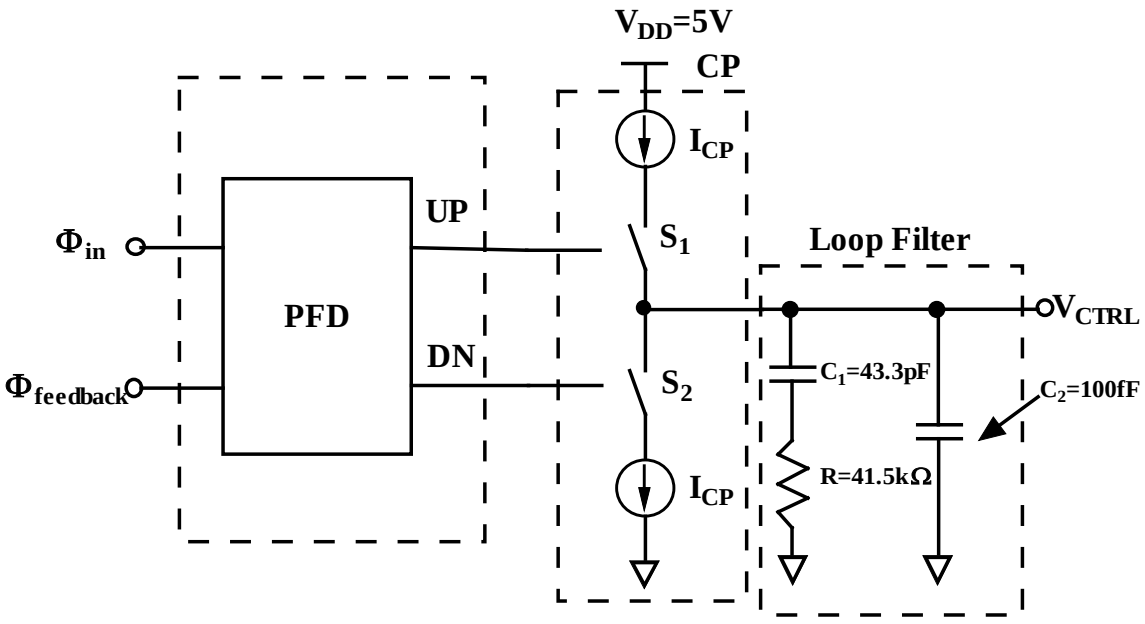

Figure 2.5: Block diagram of loop filter with PFD

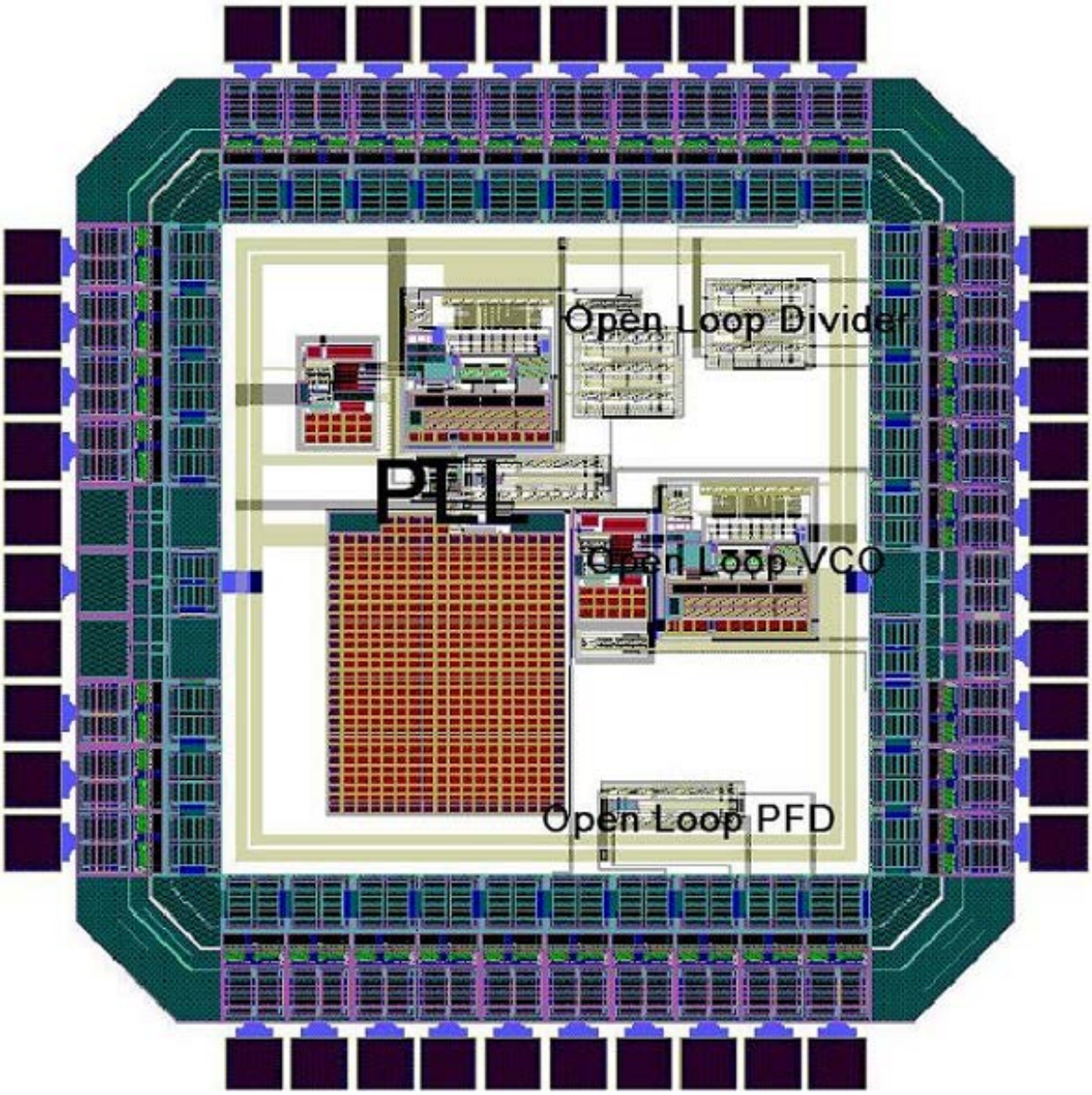

Figure 2.6: PLL chip layout.

PLL is running in a system, phase noise measurement of each building block is mixed with noises from other components which are not the exact closed loop phase noises.

2.4 Measurement Setup and Results

Figure 2.7 shows the photograph of RF test board with mounted PLL chip which is specially designed for this experiment. SMA connecting cables which provide repeatable electrical performance with low noise injection to the chip are used in this measurement. The input signal is provided by HP 8133A 3 GHz Pulse Generator and the output is connected to the 6.7 GHz Agilent ESA-E4404B Spectrum Analyzer. The chip is powered by V_{DD} = 5V and V_{SS} = 0V. The built-in phase noise module in spectrum analyzer is used for the phase noise measurement.

Figure 2.8 shows the experimentally measured voltage-frequency tuning characteristics of the VCO. The gain of the VCO is 30 MHz/*V* measured at 80 MHz. The free running frequency of the VCO is $f = f_0 + K_V V_{ctrl}$, where $f_0 = 25MHz$, V_{ctrl}=1.9V and K_V=30*MHz/V*.

Figure 2.9 shows the experimentally measured single-sideband (SSB) phase noise of the open loop VCO oscillating at 80 MHz. The open loop VCO has two pins: bias voltage and VCO output. Bias voltage pin is connected to a dc 1.9*V* and the output frequency is 80 MHz. The open loop means that only the VCO is working in this case and it is outside the PLL. The calculated closed loop VCO phase noise is obtained from Eq. (2.5) by substituting the experimentally measured open loop PSD and multiplying the square value of the transfer function calculated from Eq. (2.4).

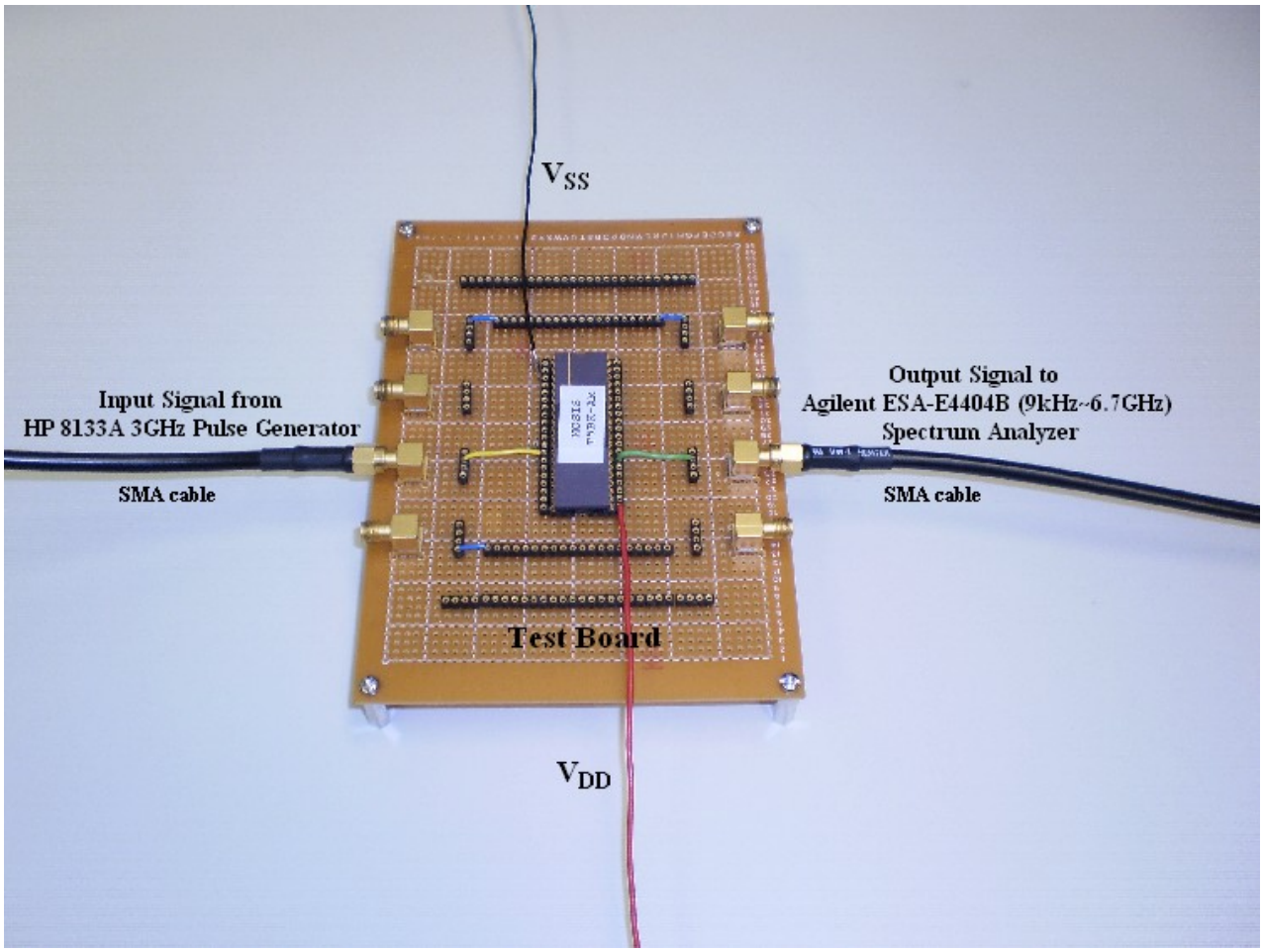

Figure 2.7: Photograph of RF test board with mounted PLL chip.

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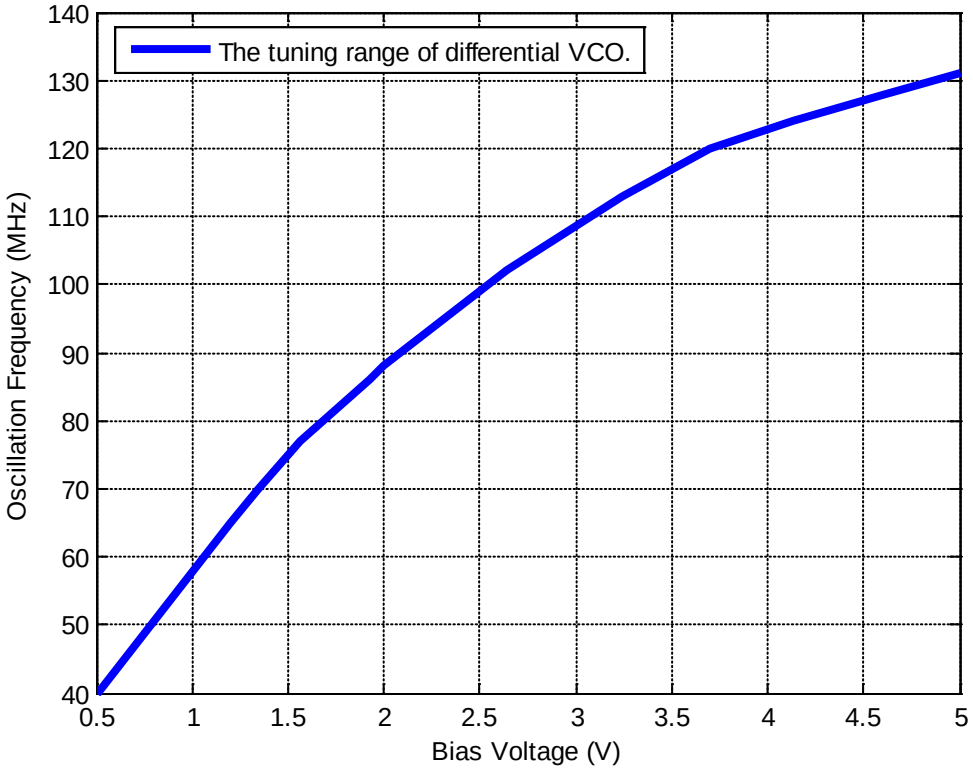

Figure 2.8: The tuning characteristics of differential VCO

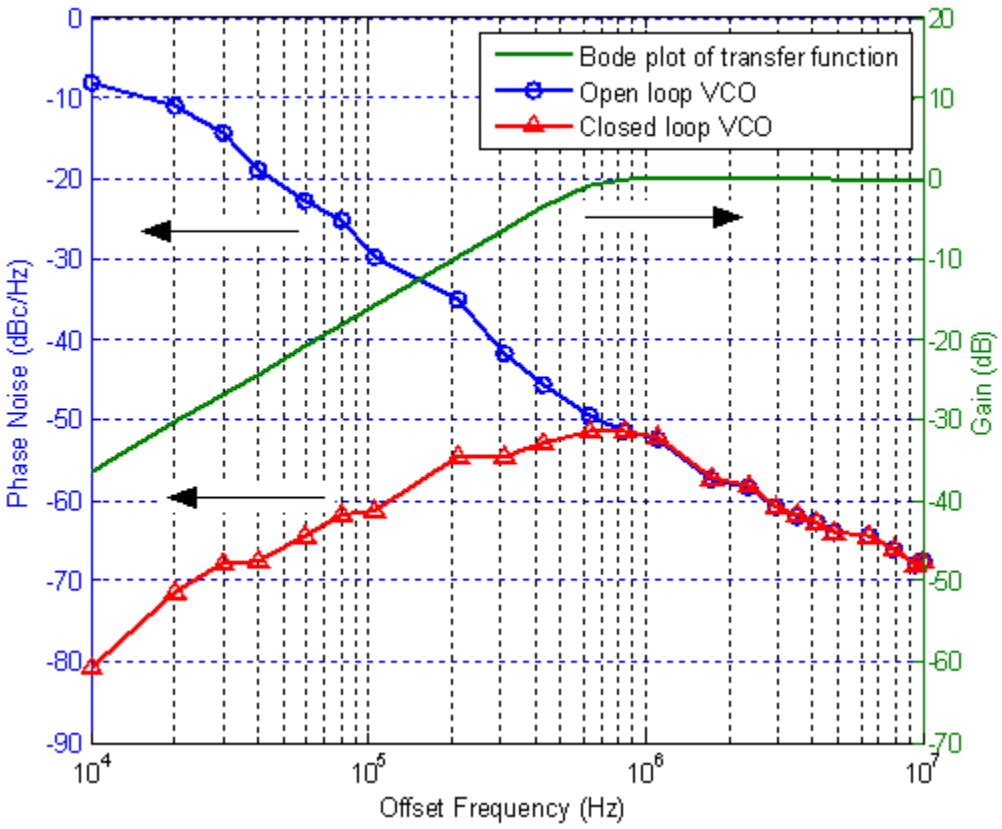

Figure 2.9: Experimental results of VCO phase noise at 80 MHz PLL output frequency.

In this paper, both the open loop and closed loop VCO phase noises are shown. It is to be noted that Hajimiri's work [50] on VCO only gives description of phase noise without any experimental support. It is very interesting to note that prediction of shape of phase noise by Hajmiri [50] agrees with our experimental findings. In Fig. 2.9, open loop phase noise of VCO is -20 dB/decade along the offset frequency, closed loop phase noise is 20 dB/decade at the lower frequency and -20 dB/decade at the higher frequency.

The Bode plot of the transfer function is 20 times the logarithm of the transfer functions of each block obtained from Eqs. (2.4), (2.7), (2.9), (2.11) and (2.13). The calculated closed loop phase noises are shown in Figs. 2.9-2.13. Phase noise power spectrum and Bode plot can be expressed in the same diagram with two Y axes to present how transfer function and open loop phase noise affect the closed loop phase noise. It should be noted that in Figs. 2.9-2.13, the Bode plots of transfer functions are expressed in Gain (dB) and the phase noise is expressed in dBc/Hz.

Figure 2.10 shows the experimentally measured SSB phase noise from the input reference clock which is generated by HP 8133A 3 GHz Pulse Generator. The experimentally measured phase noise is between -70 to -103 dBc/Hz from 10 kHz to 10 MHz offset frequency at 10 MHz center frequency. The closed loop phase noise when pulse generator is connected to the chip is obtained from Eqs. (2.7) and (2.8).

Figure 2.11 shows the experimentally measured divider open loop SSB phase noise at 80 MHz PLL output frequency. Following the method described above, the (2.10), (2.12) and (2.14). When the slope of Bode plot is negative, the closed loop phase noise will go negative more sharply than the open loop one. On the other hand, when the slope of Bode plot is positive, the closed loop phase noise will go negative less sharply than the open loop one or turns out to be flat.

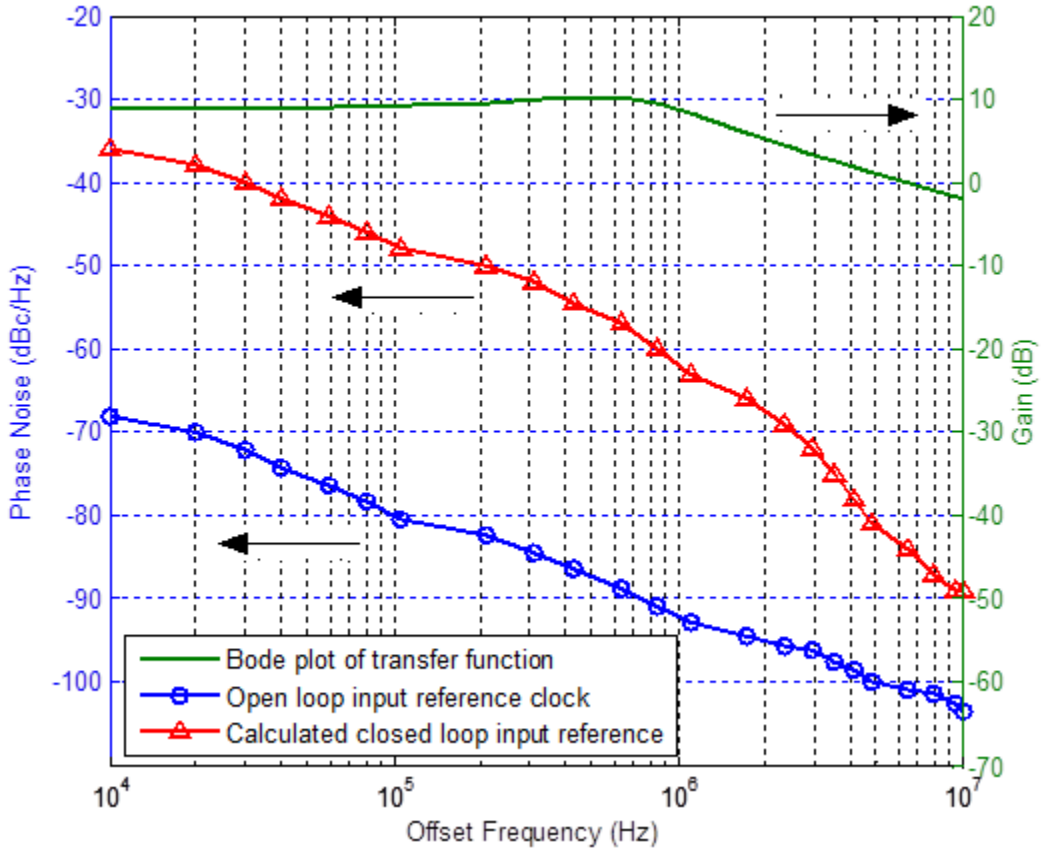

Figure 2.10: Experimental results of input reference clock phase noise at 80 MHz PLL output frequency.

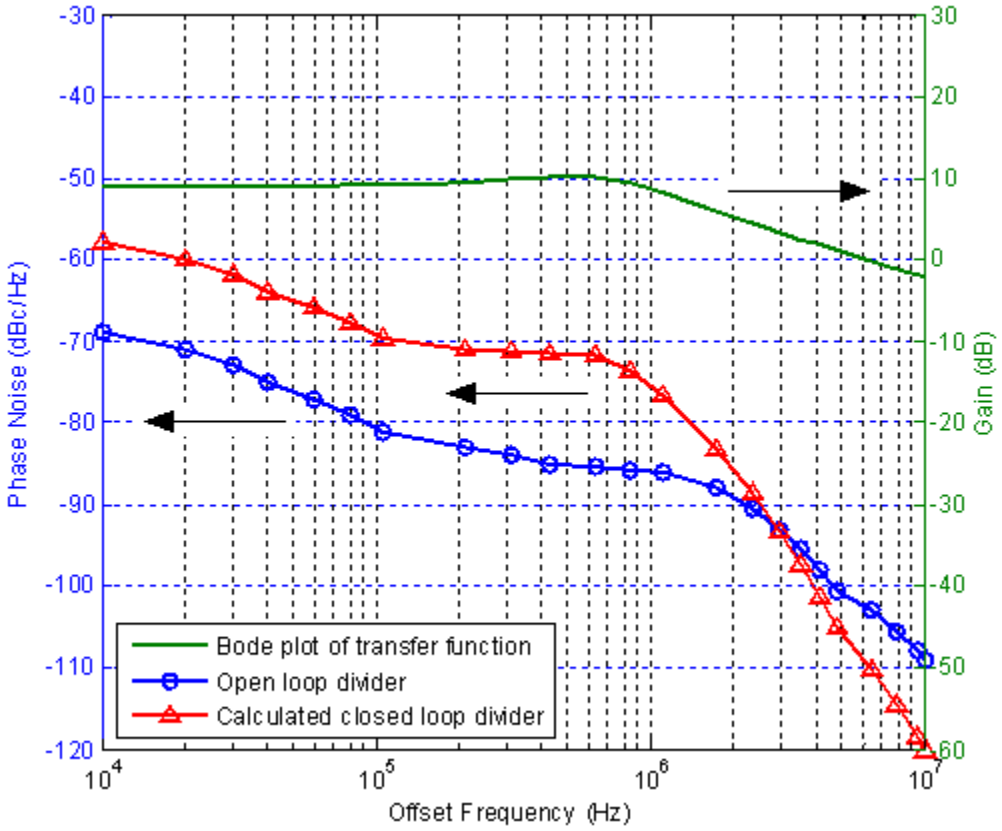

Figure 2.11: Experimental results of divider phase noise at 80 MHz PLL output frequency.

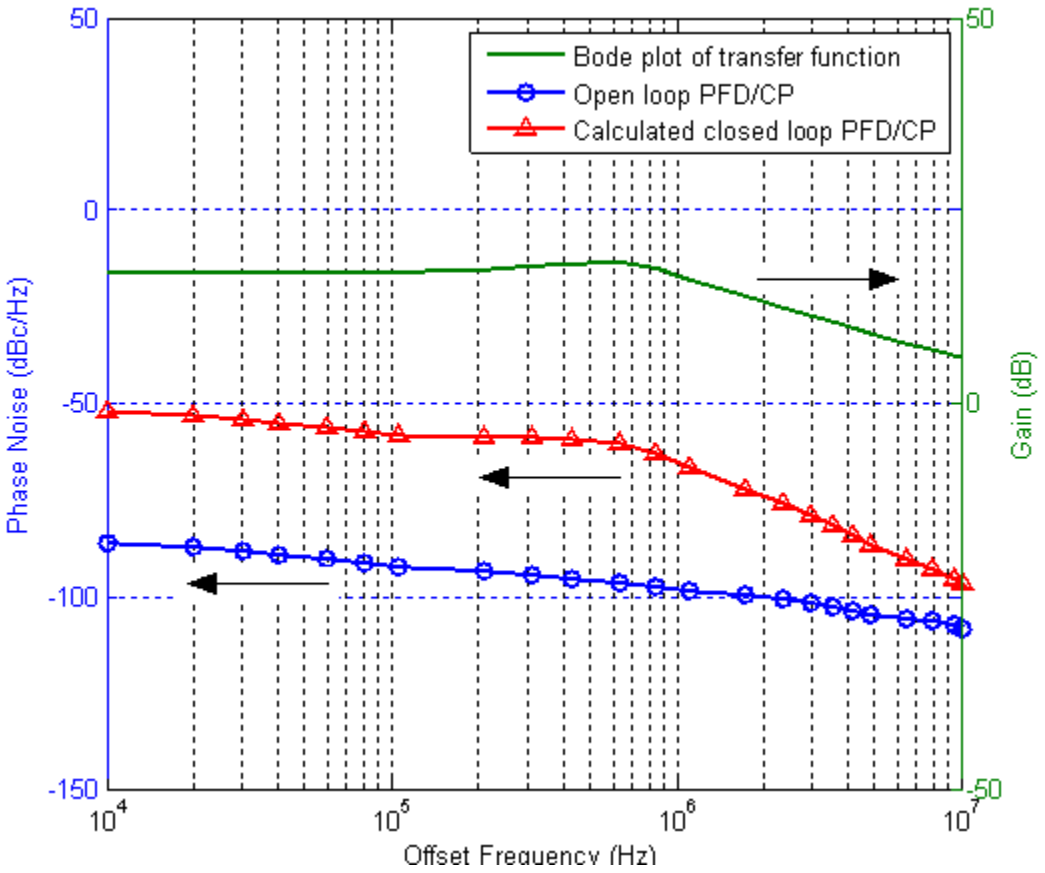

Figure 2.12: Experimental results of PFD/CP phase noise at 80 MHz PLL output frequency.

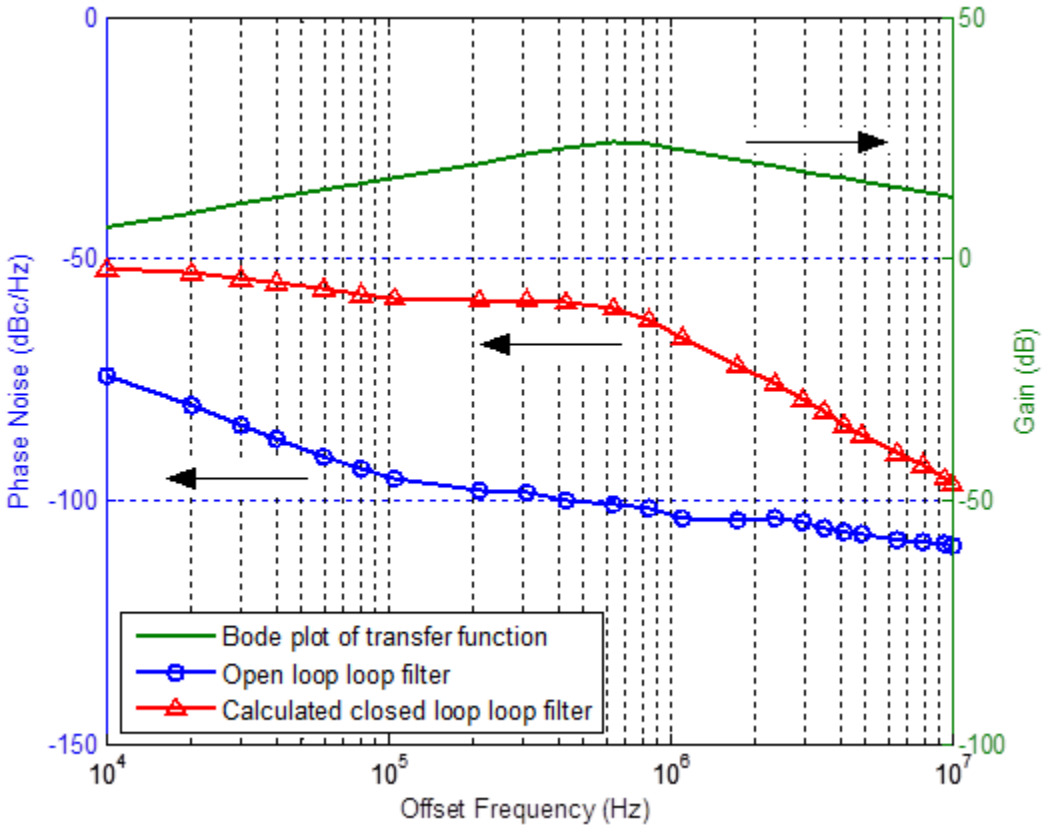

Figure 2.13: Experimental results of loop filter phase noise at 80 MHz PLL output frequency.

Figure 2.11 shows the experimentally measured divider open loop SSB phase noise at 80 MHz PLL output frequency. Following the method described above, the (2.10), (2.12) and (2.14). When the slope of Bode plot is negative, the closed loop phase noise will go negative more sharply than the open loop one. On the other hand, when the slope of Bode plot is positive, the closed loop phase noise will go negative less sharply than the open loop one or turns out to be flat.

The PLL output phase noise is obtained by the superposition of the noises spectra from VCO, input reference, divider, PFD and loop filter and are shown in Figures 2.14. The solid line shows the PLL output phase noise by summing the closed loop output phase noises from all other components: VCO, input reference clock, PFD/CP, loop filter and divider. There is a peak observed in VCO closed loop phase noise when the offset frequency is near the predicted loop bandwidth, 800 kHz. The low-pass loop filter in PLL blocks all higher order noises. Thus, the phase noise of PLL follows the closed loop VCO phase noise beyond the PLL bandwidth. At low offset frequencies, noise is dominated by the input reference clock since the loop gain tries to make the phase of VCO stable. Phase noises generated by PFD/CP, divider and loop filter dominate the mid of offset frequencies of the PLL output phase noise.

The experimental PLL output phase noise compared with the calculated one is shown in Figure 2.15. The experimentally measured phase noise of the fabricated CMOS PLL circuit follows the calculated frequency dependence phase noise behavior and is in good agreement. By comparing the experimental PLL output and calculated PLL output phase noise, 1-2 dB difference is observed which is within the experimental error of measurement.

2.5 Conclusion

In this work, a second-order order PLL circuit is designed in 0.5 μm n-well CMOS and an attempt has been made to model phase noise based on superposition of phase noises from its following circuit building blocks: t he input reference, VCO, frequency divider, PFD and the loop filter. Experimentally measured phase noise of the PLL chip follows the modeled behavior and is in good agreement. The closed loop phase noise of PLL can be obtained by the superposition method under its linear operating range.

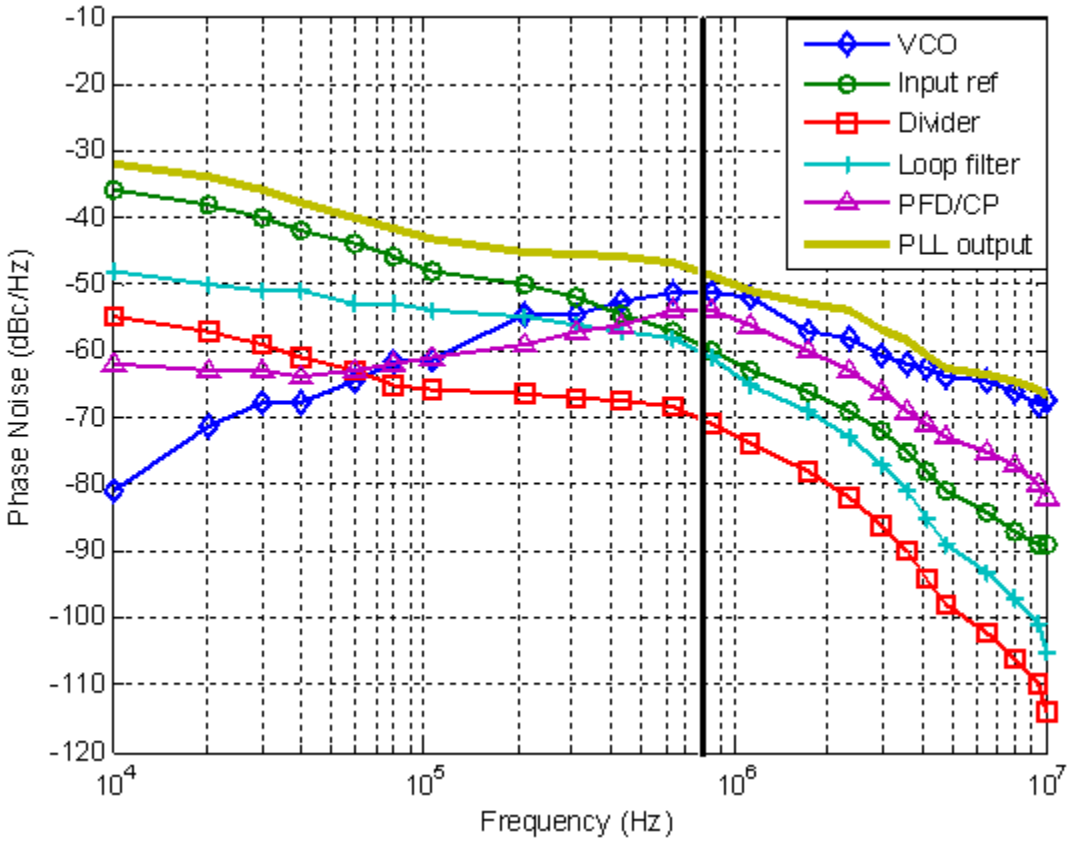

Figure 2.14: Closed-loop PLL output noise performance compared to the closed-loop noise performances of the individual components.

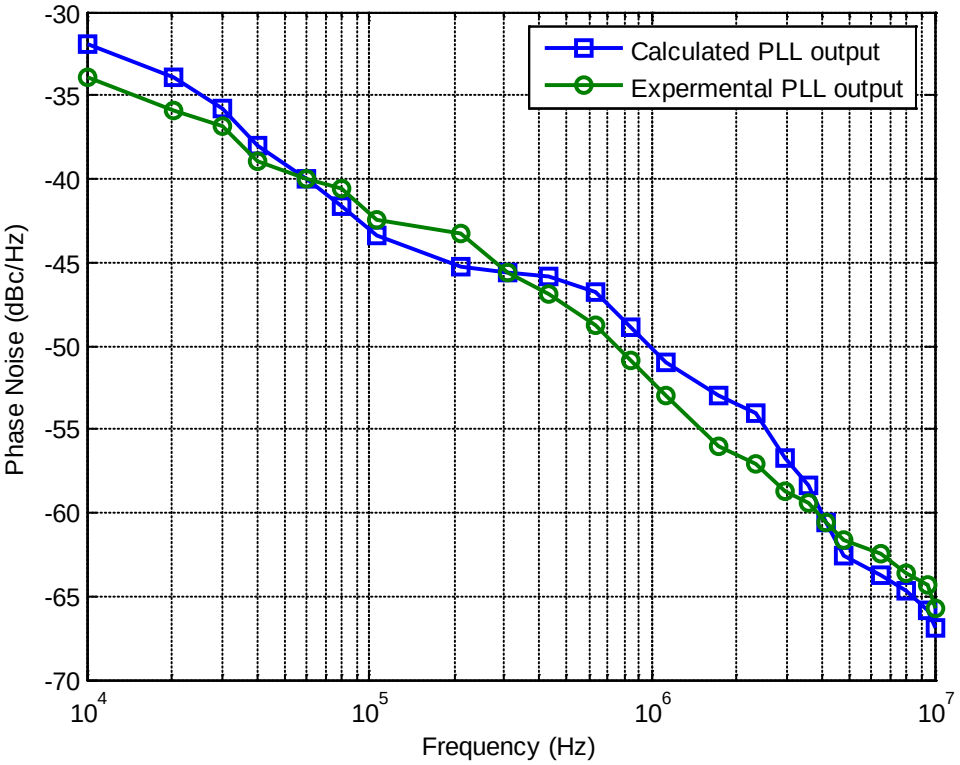

Figure 2.15: Calculated and measured PLL phase noises.

CHAPTER 3

PHASE NOISE AND JITTER STUDY IN CMOS SWITCHABLE PHASE-LOCKED LOOP CONSIDERING HOT CARRIER EFFECTS*

The phase-locked loops have been widely utilized in high speed communication systems. Low-cost frequency synthesizers with voltage-controlled oscillators (VCOs), such as the single-ended ring oscillator and differential ring oscillator, are widely used in wireless LAN. There are many concerns in these applications for the PLL design. These concerns include phase noise, jitter, power consumption, frequency tuning range, VCO tuning gain and locking/settling time etc. Tradeoffs often exist among different design goals. For example, narrow PLL bandwidth may be required to minimize the noise contribution from dividers and to suppress reference spurs [57]. However, this leads to a long locking time. Furthermore, as the operating frequency increases, power consumption also rises.

We propose a switchable PLL, which combines two relatively narrow bandwidth PLLs into a single chip and use a frequency detector to decide which PLL to choose according to the reference frequency. As a result, the switchable PLL can work over a wide tuning range and at a high frequency. It also achieves a short locking time without sacrificing the jitter and phase noise performance.

Two PLL frequency synthesizers are integrated in a single chip design, one is working in high frequency range and the other is working in low frequency range. Both

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*Part of the work is reported in the following publications:

1. Y. Liu, A. Srivastava and Y. Xu, "Switchable PLL frequency synthesizer and hot carrier effects," Journal of Circuits and Systems, Vol. 2, No. 1, pp-45-52, Jan. 2011.
2. Y. Liu, A. Srivastava and Y. Xu, "A switchable PLL frequency synthesizer and hot carrier effects," *Proc. ACM Great Lakes Symposium on VLSI*, pp. 481-486, May 10-12, 2009, Boston, USA.

PLLs include phase-frequency detector (PFD), charge pump (CP), 2nd order loop filter, current starved VCO and 1-by-8 divider. The input range is from 40 MHz to 144 MHz and output range is from 320 MHz to 1.15 GHz. The charge pump and 2nd order low pass loop filter are used to make the system stable and minimize the high frequency noise. PFD is implemented with NOR gates and D-flip flops.

In submicron CMOS devices, the performance of integrated circuits is influenced by the hot carrier effect due to increased lateral channel electric field and results in circuit degradation. Thus, jitter and phase noise may also be affected. Recently, results of hot carrier stress on CMOS VCOs, one of the modules of a PLL have been reported [58-60]. In this work, hot carrier effect has been considered and its effect on phase noise and jitter has been studied.

3.1 The Switches

As shown in Figure 3.1, the switch includes a local oscillator, frequency detector (FD) and a two input multiplexer (MUX). The same kind of VCO described above is working as local oscillator but the difference is that local VCO doesn't have stress mode and the oscillation frequency is locked at 80 MHz. The FD compares it with the input signal. When the input frequency is higher than 80 MHz, the FD output is high which means the high frequency PLL (H_PLL) output signal will go out via the MUX. On the other hand, when the input signal frequency is lower than 80 MHz, the output of the frequency detector is low and the low frequency PLL (L_PLL) output signal will go out via the MUX.

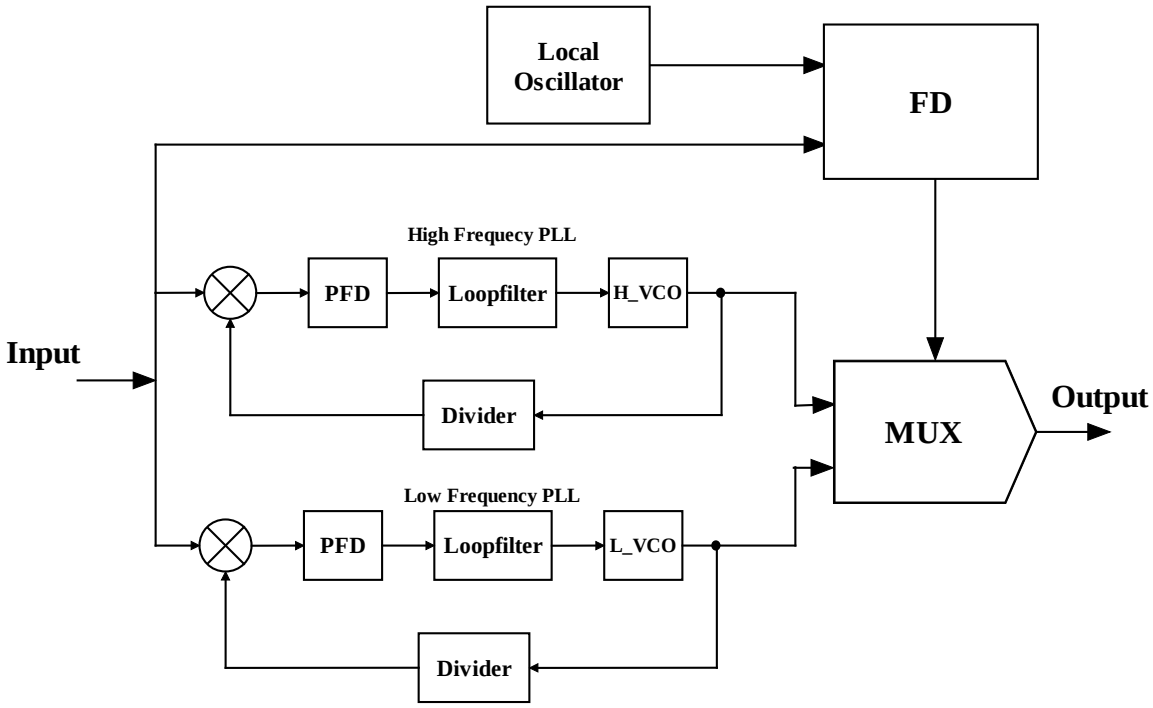


Figure 3.1: Building blocks of a switchable PLL architecture.

The FD circuit schematic is shown in Figure 3.2. The structure of the detector is same with the PFD in each PLL. The RC circuit transfers the output AC signals of PFD to relatively high and low DC voltage signals and comparator compares these two signals to give high or low voltage, which drives the MUX.

3.2 Analysis

Figure 3.3 shows the output of the switchable PLL at different frequencies where 320 MHz waveform is the low frequency PLL (L_PLL) output and 1.12 GHz waveform is the high frequency PLL (H_PLL) output.

Figure 3.4 shows the variation of PLL output frequency versus control voltage, with and without hot carrier effects. Both the oscillation frequency and frequency range of the PLLs decrease. For the worst case, the overlapping frequency range, which is 250 MHz without hot carrier effects, decreased to 200 MHz. Figure 3.5 shows the PLL tuning frequency range under NBTI stress. It appears from the comparison of figures 3.4 and 3.5 that NBTI stress follows the behavior similar to HCE on PLL tuning frequency with frequency overlap.

The function of RC in the frequency detector is to translate the PFD output pulses into DC voltages, which are shown in Figure 3.6. If the input frequency is less than the reference frequency, which is output of the local oscillator defined as 80 MHz, the output is at low level; while if the input frequency is higher than the reference frequency, the output is at high level. But if the input frequency is closer to the reference frequency, it will take more time to get the DC output. Figure 3.7 shows this phenomenon.

When the input frequency equals the reference frequency, the output will be oscillating and the stable time will be infinity as shown in Figure 3.7. To deal with this problem, the frequency overlapping range of the two PLLs is expanded.

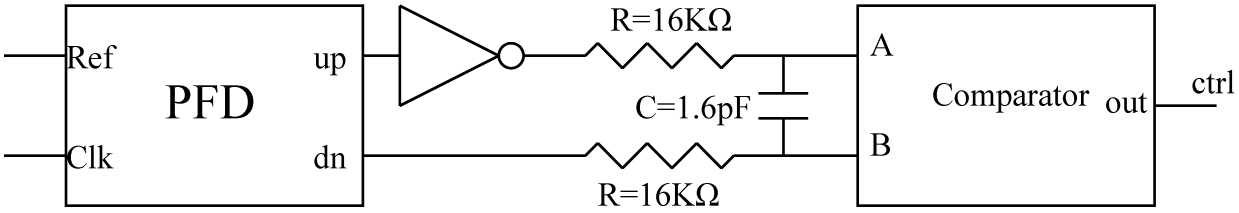


Figure 3.2: Frequency detector architecture.

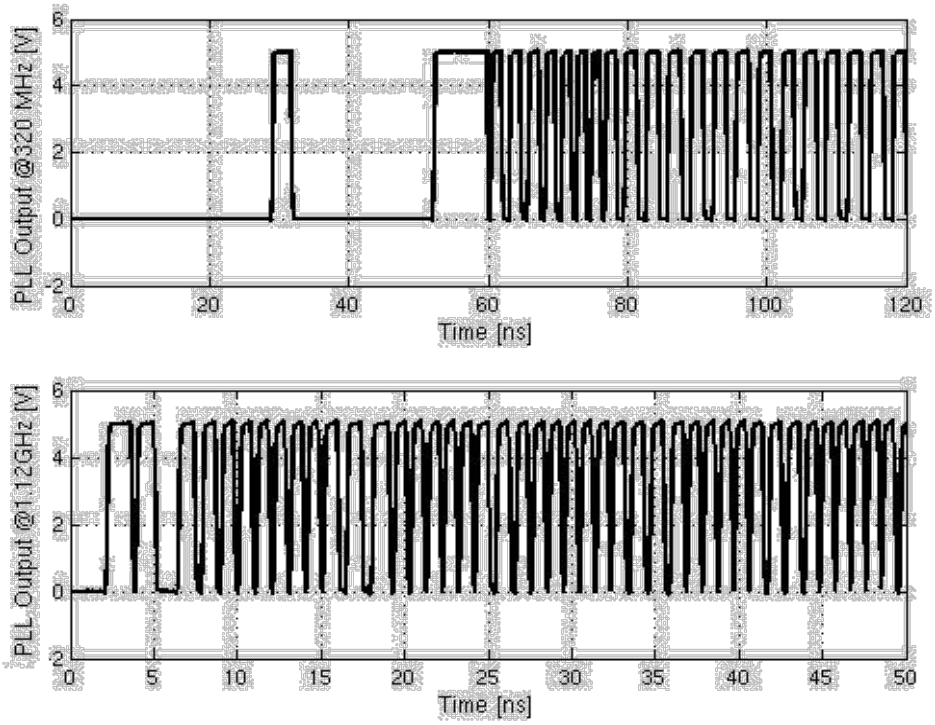


Figure 3.3: Switchable PLL outputs at different frequencies.
(L_PLL starts to oscillate after 60ns and H_PLL starts to oscillate after 5ns).

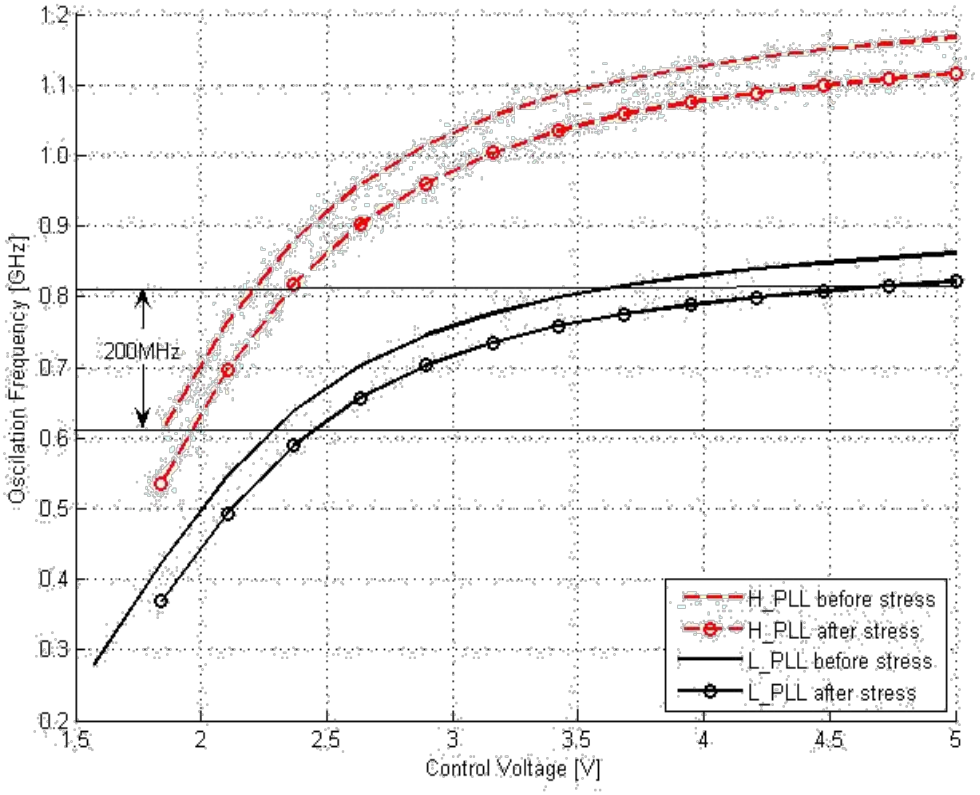


Figure 3.4: Hot carrier effects on frequency synthesizer.

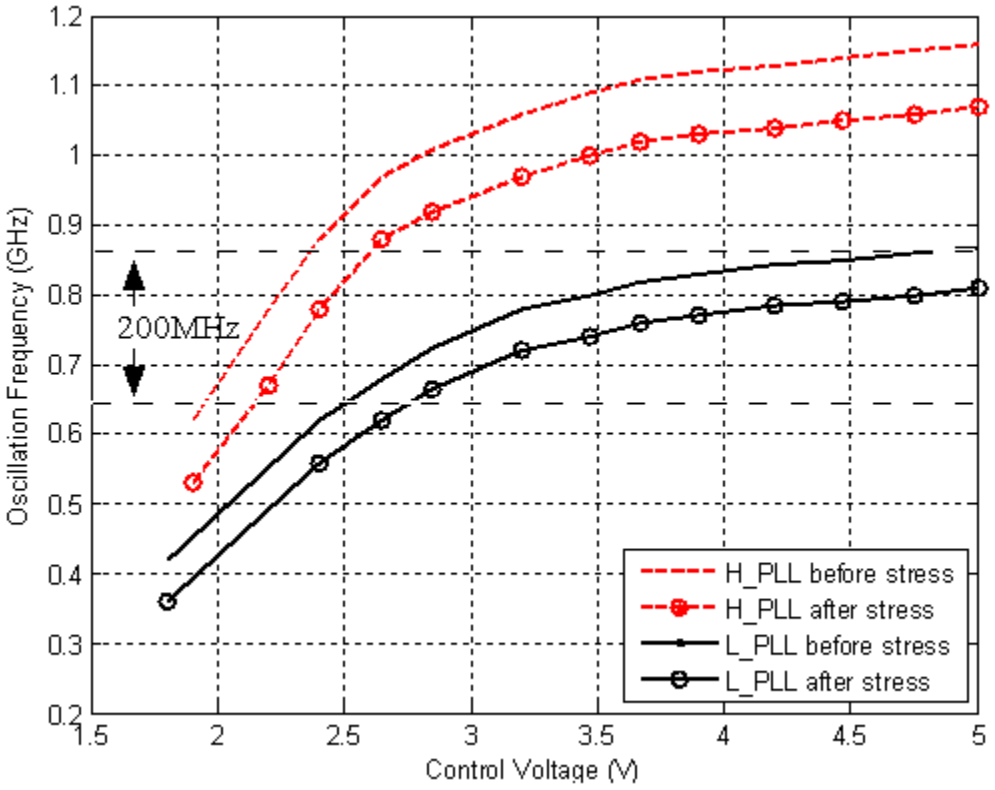


Figure 3.5: The NBTI degradation of switchable PLL tuning frequency range.

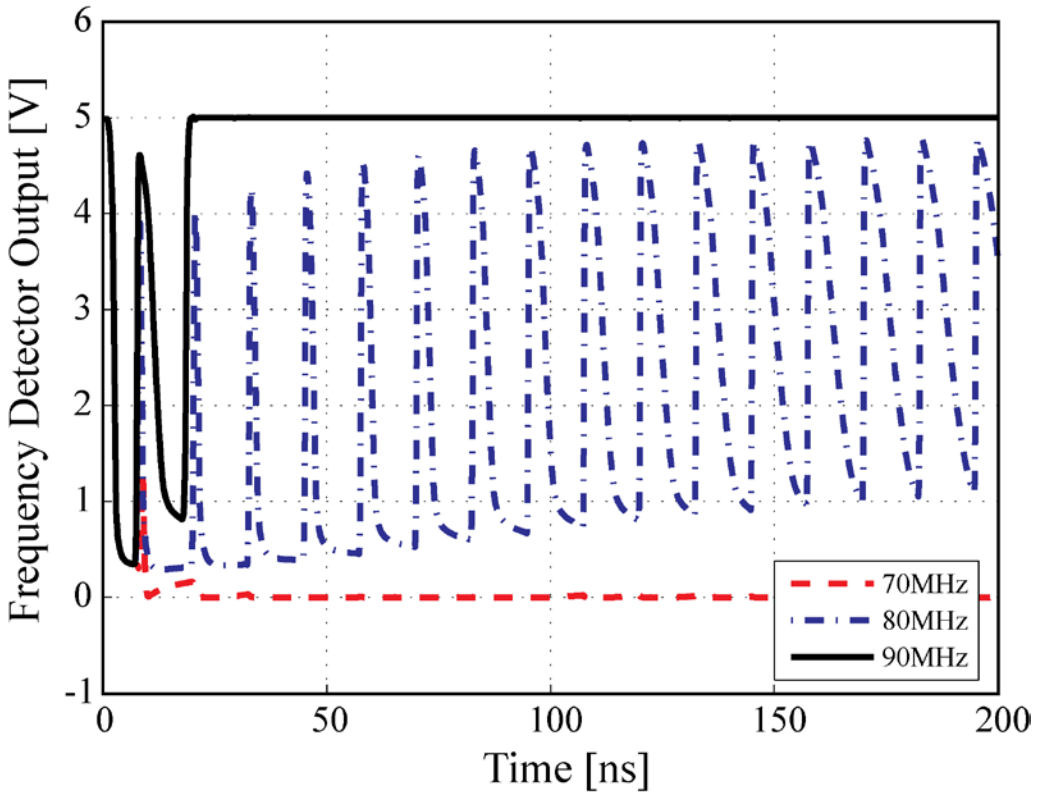


Figure 3.6: Frequency detector output.

In Figure 3.5, it can be noticed that the overlapping range is 200 MHz at least. Thus, if the input frequency is close to reference frequency (80 MHz) the control voltage of the local oscillator can be adjusted to change the reference frequency higher or lower. The large overlapping range guarantees that the difference between the input frequency and reference frequency is large enough so that the stabilizing time is smaller than 200 ns, which is the stabilizing time of the high frequency PLL. As a result, the stabilizing time of the switchable PLL is decided by the PLLs, while the operation range is much larger than that of the single PLL.

3.3 Simulation Results

Figure 3.8 shows the simulation, modeled and measured results of the oscillation frequency of open loop VCO in H_PLL before and after hot carrier stress versus different bias voltages. The simulation results are performed by Cadence/Spectre. It is shown that at a 4 V bias, the frequency is around 1150 MHz before stress and it is about 950 MHz after stress. This is the effect on VCO output frequency due to hot carrier injection in MOSFETs. Figure 3.8 includes experimental data on tuning range of VCO whose operation frequency is slightly lower than the simulation one. Phase noise and jitter measured under hot carrier stress for both VCO and PLL are reported in the following section.

Figure 3.9 shows the decrease of H_PLL VCO frequency gain at 2.5 V bias voltage versus stress time, which agrees with the Eq. (2.15). After 4 hours of hot carrier injection, the VCO gain decreases by about 33%, from 460 MHz to 310 MHz.

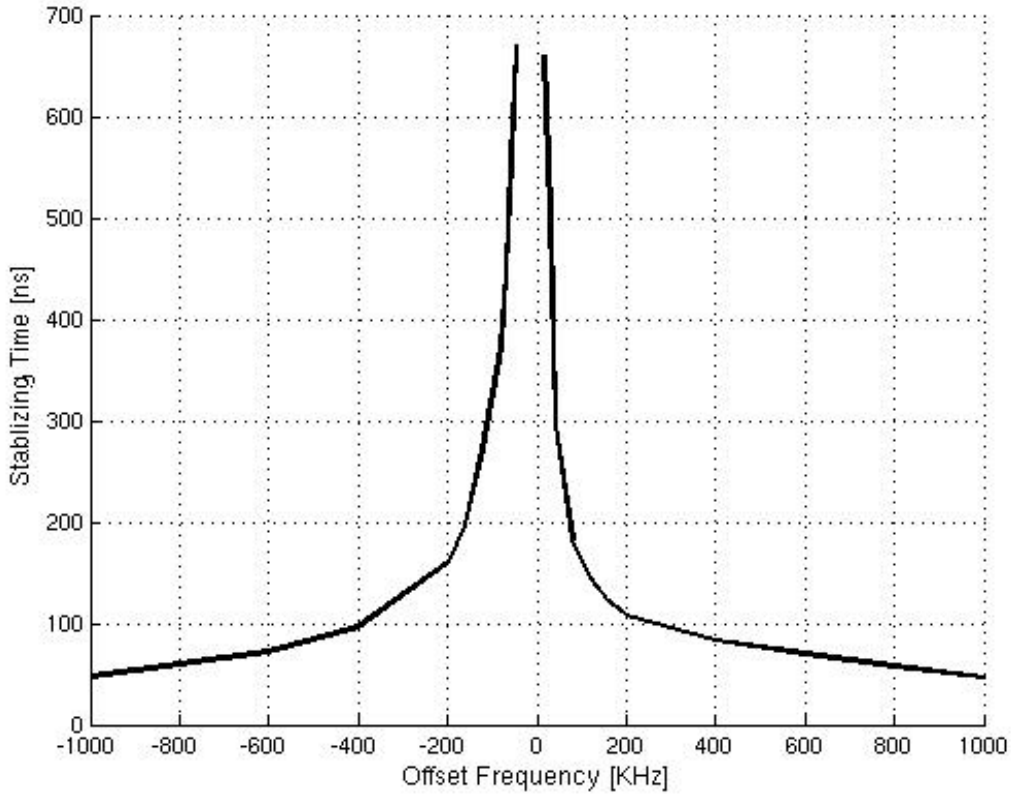


Figure 3.7: Frequency detector stabilizing time versus frequency.

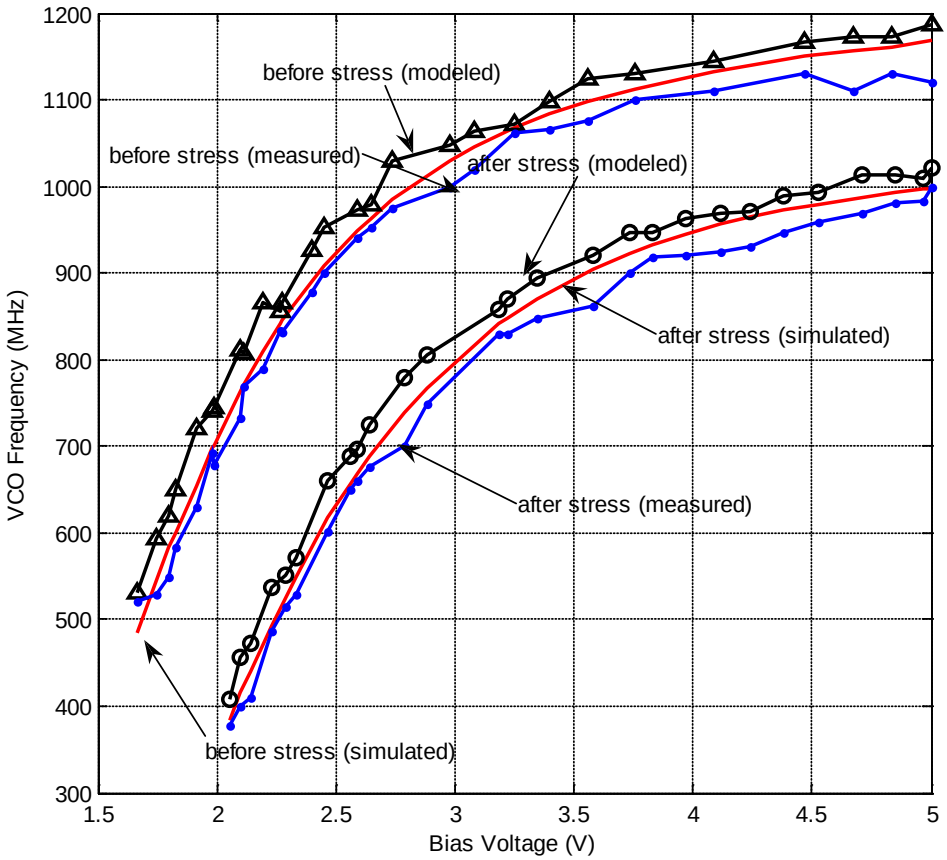


Figure 3.8: The degradation of VCO frequency due to hot carrier effects.

Figure 3.10 shows the simulation result for the variation of the jitter proportionality parameter, κ changing with the oscillation frequency before and after 4 hours of stress. κ increases by about 10%, which means the value of the jitter of the 3 stages single-ended VCO increases by about $0.2\sqrt{\Delta T}ns$ due to hot carrier effects from Eq. (2.20). ΔT is the time difference between rising edge of trigger clock and the observed clock. Thus, the jitter $\sigma_{\Delta T}$ mainly depends on κ, which varies with different tuning frequencies.

3.4 Experimental Results

Figure 3.11 shows the experimental and modeled phase noises of the open loop VCO at 1 GHz oscillation frequency before and after hot carrier stress. The experimental results which are from open loop VCO circuit on the chip are in good agreement with the modeled phase noises which are calculated from Eq. (2.22).

Figure 3.12 shows the experimental results of device degradation on RMS jitter performance under different PLL output frequencies due to hot carrier effects. A 40 ps increase is observed after 4 hours of stress.

The experimental results for PLL output frequencies with hot carrier effects are listed in Table 3.1, measured using Tektronix 11801A Digital Sampling Oscilloscope.

Figure 3.13 shows a photograph of the switchable PLL jitter performance measured by a digital sampling oscilloscope and is 59 ps . Figure 3.14 shows the experimental results of PLL output phase noise at 700 MHz carrier frequency by using Agilent ESA-E4404B Spectrum Analyzer, before and after stress. The offset frequency is from 10 kHz to 1 MHz. In Figure 3.14, the PLL phase noise before stress is -79dBc/Hz at 10 kHz offset frequency and is around -104dBc/Hz at 1 MHz offset frequency. The PLL

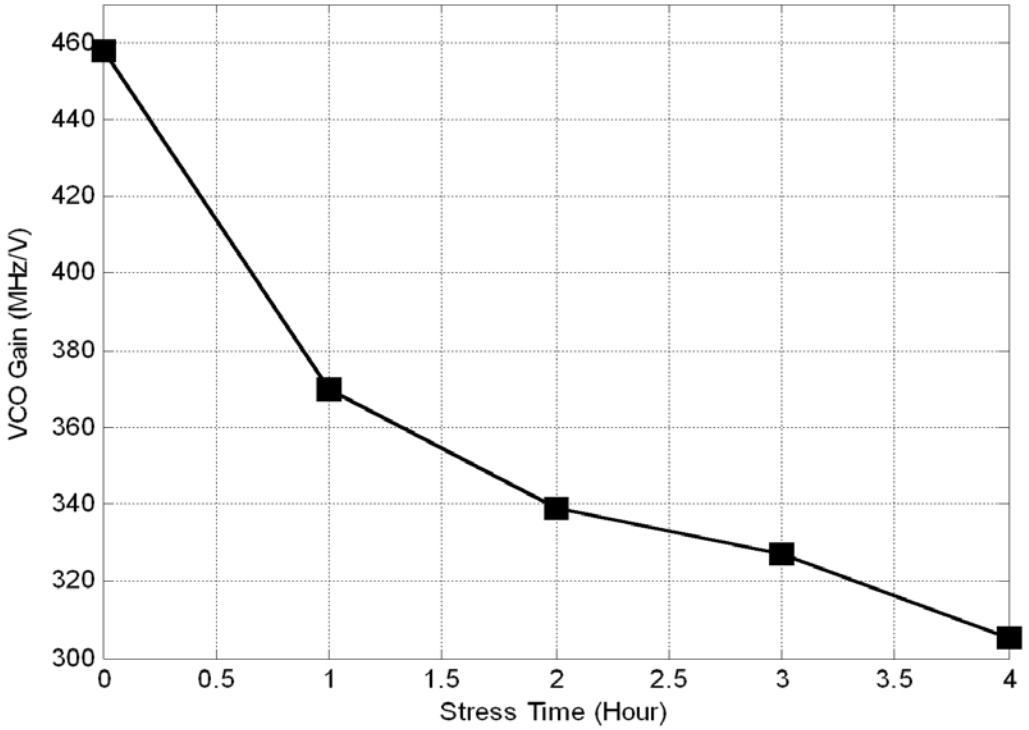


Figure 3.9: VCO gain versus stress time for H_PLL for H_PLL.
Note: Bias Voltage=2.5V.

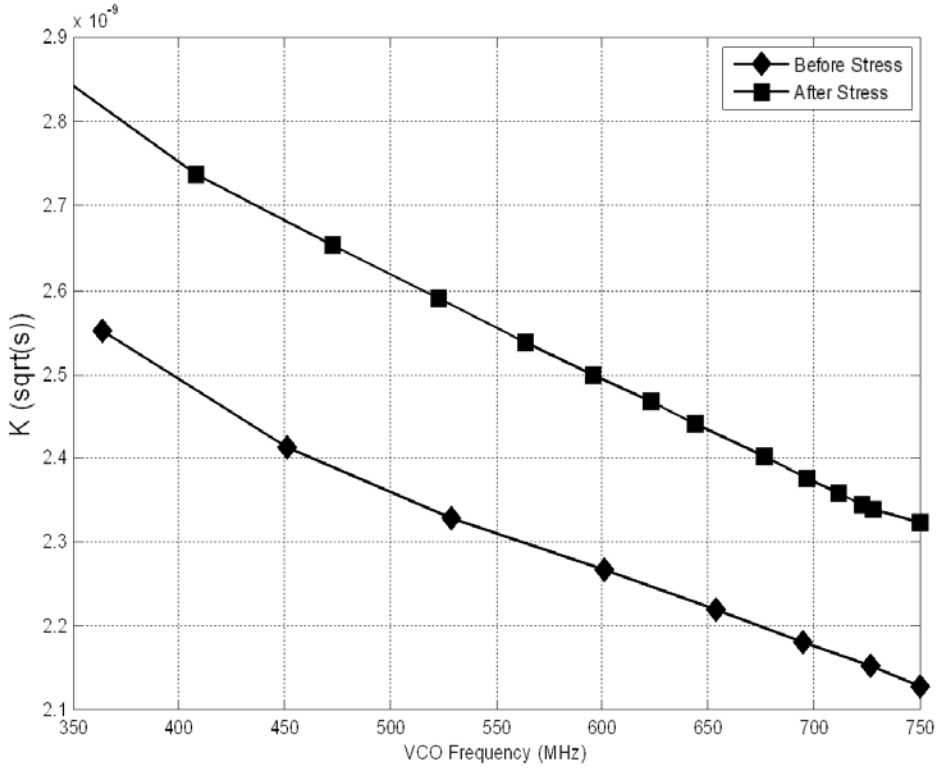


Figure 3.10: The dependence of κ and VCO frequency due to hot carrier effects.

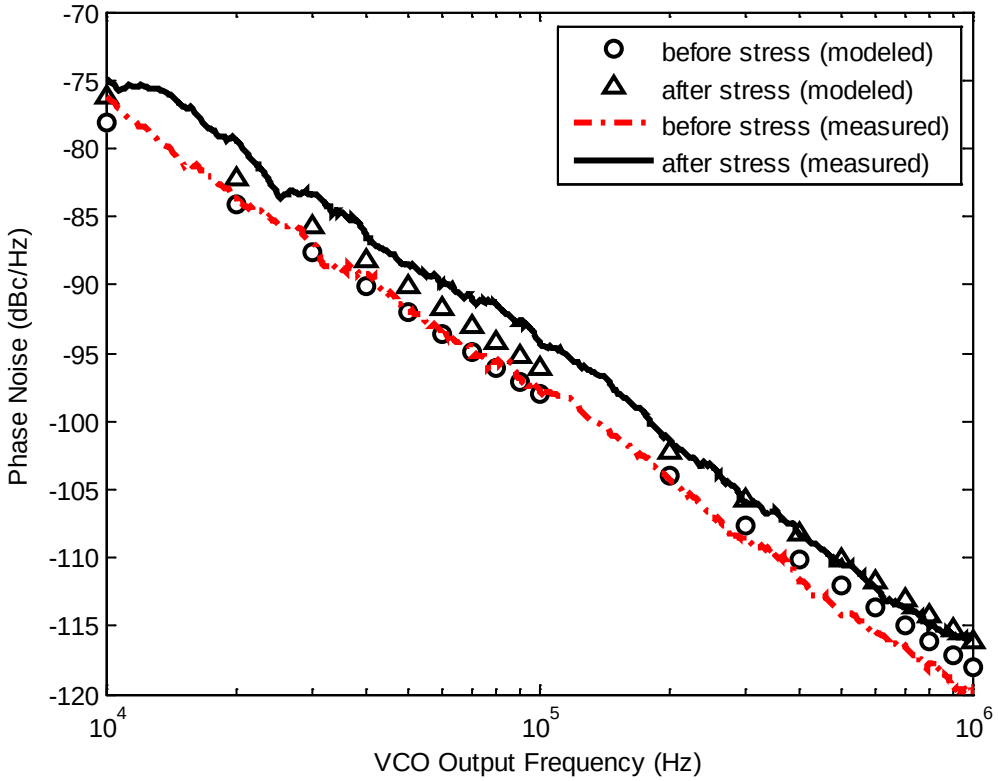


Figure 3.11: Degradation on phase noise performance under 1 GHz oscillation frequency.

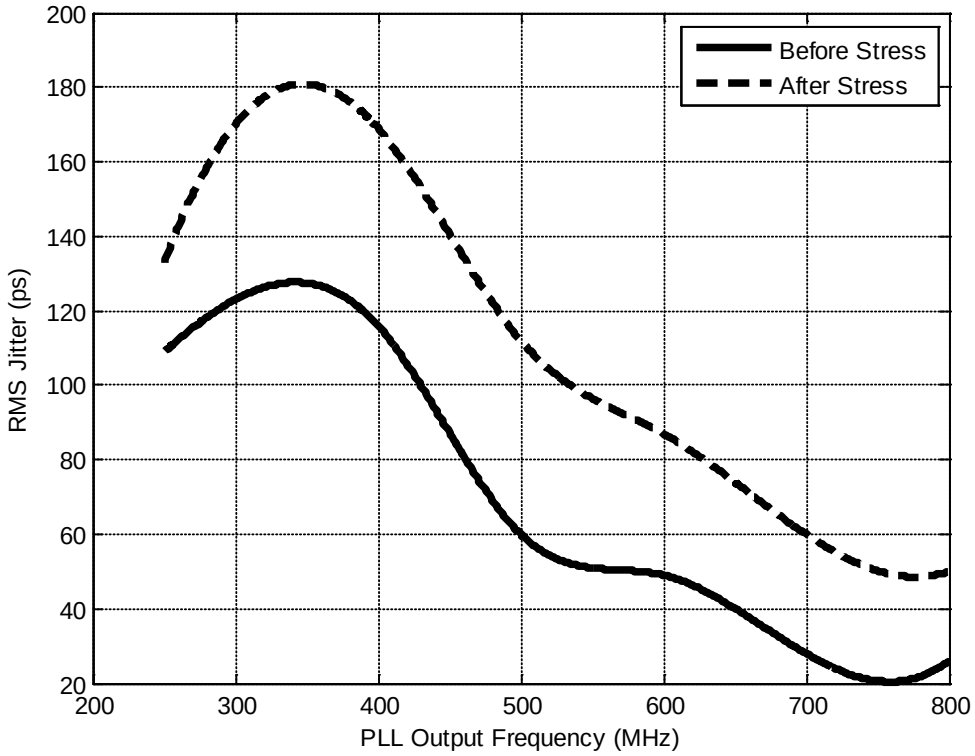


Figure 3.12: Experimental results of PLL jitter.

Table 3.1. Experimental results for different output frequencies of the PLL

Input Freq. (MHz)	**Output Freq.(MHz)**	**RMS Jitter(ps)**	**RMS Jitter (HCE) (ps)**	**Phase Noise (dBc/Hz) at 10kHz offset (w/o HCE, w/ HCE)**		**Phase Noise (dBc/Hz) at 1MHz offset (w/o HCE, w/ HCE)**	
31	250	109	132	-70	-69	-117	-116
38	300	123	168	-76	-75	-115	-111
50	400	116	166	-79	-75	-113	-109
63	500	59	113	-70	-68	-126	-124
75	600	50	87	-69	-66	-108	-104
88	700	26	60	-61	-60	-104	-103

phase noise increases by about 1-2 dB relative to carrier power per Hertz after four hours of hot carriers stress.

The switchable PLL described in the present work was fabricated in 0.5 μm n-well CMOS process. Figure 3.15 and Figure 3.16 show the *Cadence/Virtuoso* layout and the microphotograph of the fabricated switchable PLL chip, respectively.

3.5 Conclusion

A new strategy of switchable CMOS phase-locked loop frequency synthesizer is proposed, designed and fabricated in 0.5 μm n-well CMOS process. Cadence/Spectre simulation results show that the frequency range of the switchable PLL is between 320 MHz to 1.15 GHz. The experimental results show that the RMS jitter of the PLL changes from 26ps to 133ps as output frequency varies. The device degradation model designed in Chapter 2 due to hot carrier effects has been used to analyze the jitter and phase noise performance in open loop voltage-controlled oscillator (VCO).

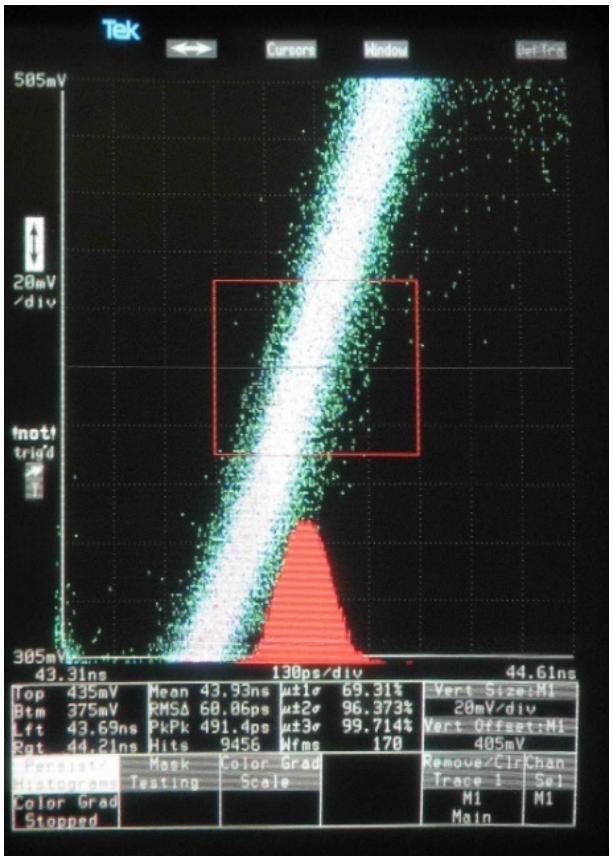


Figure 3.13: A photograph of PLL jitter.

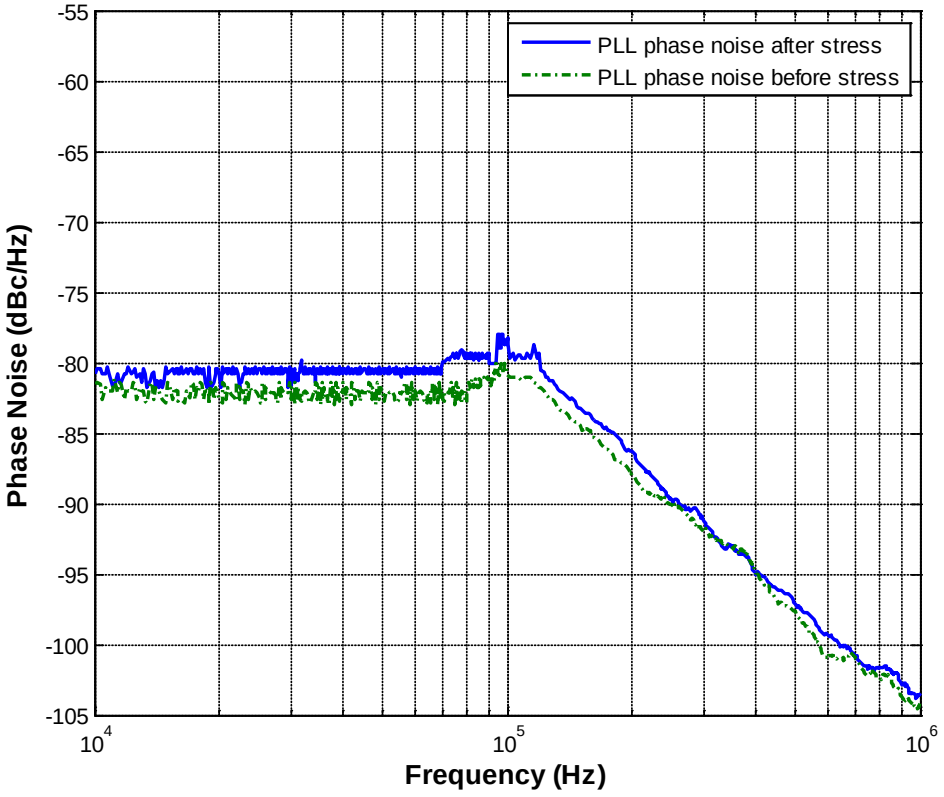


Figure 3.14: Experimental results of PLL phase noise at 700MHz carrier frequency.

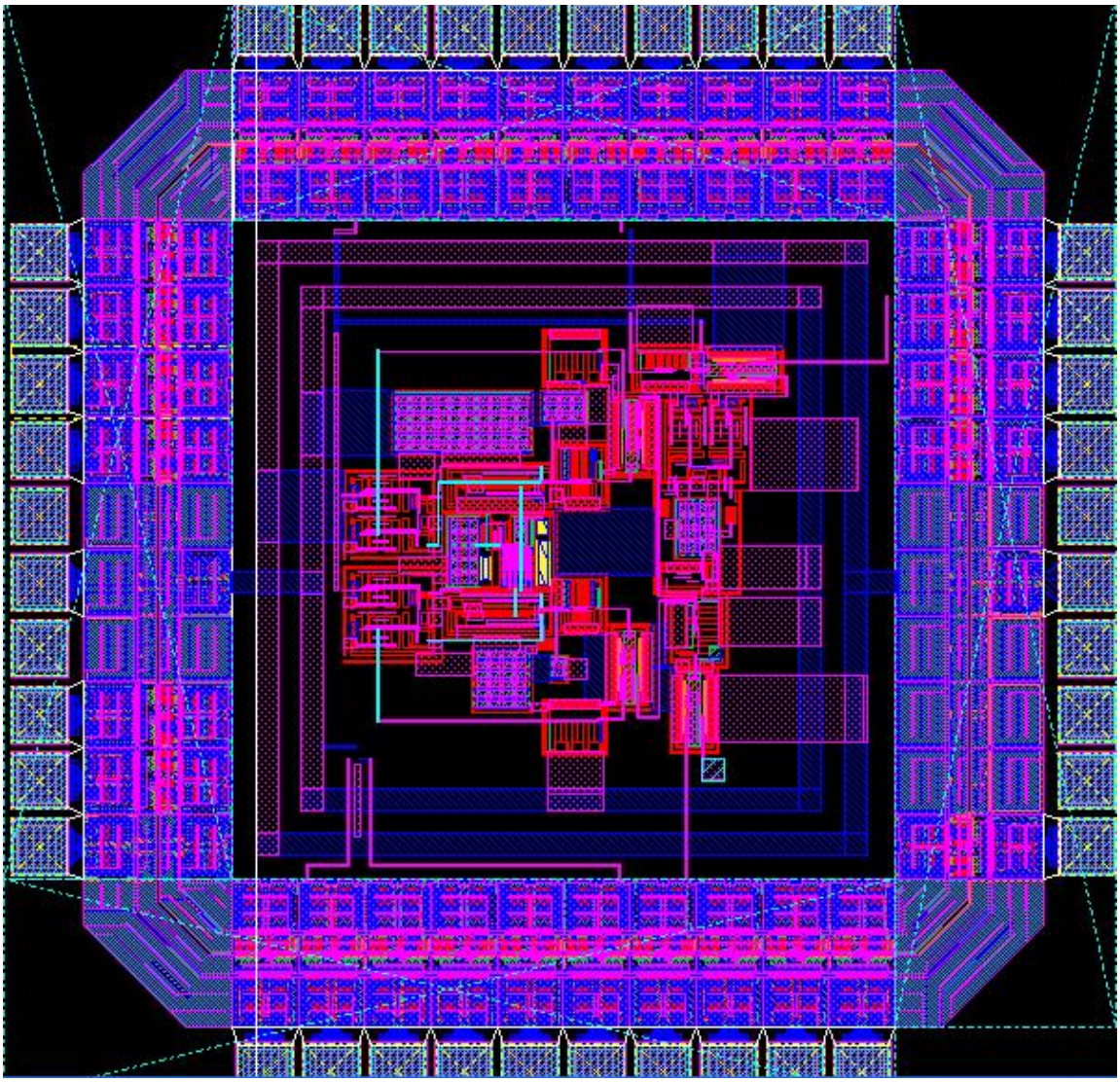


Figure 3.15: Layout of switchable PLL frequency synthesizer.

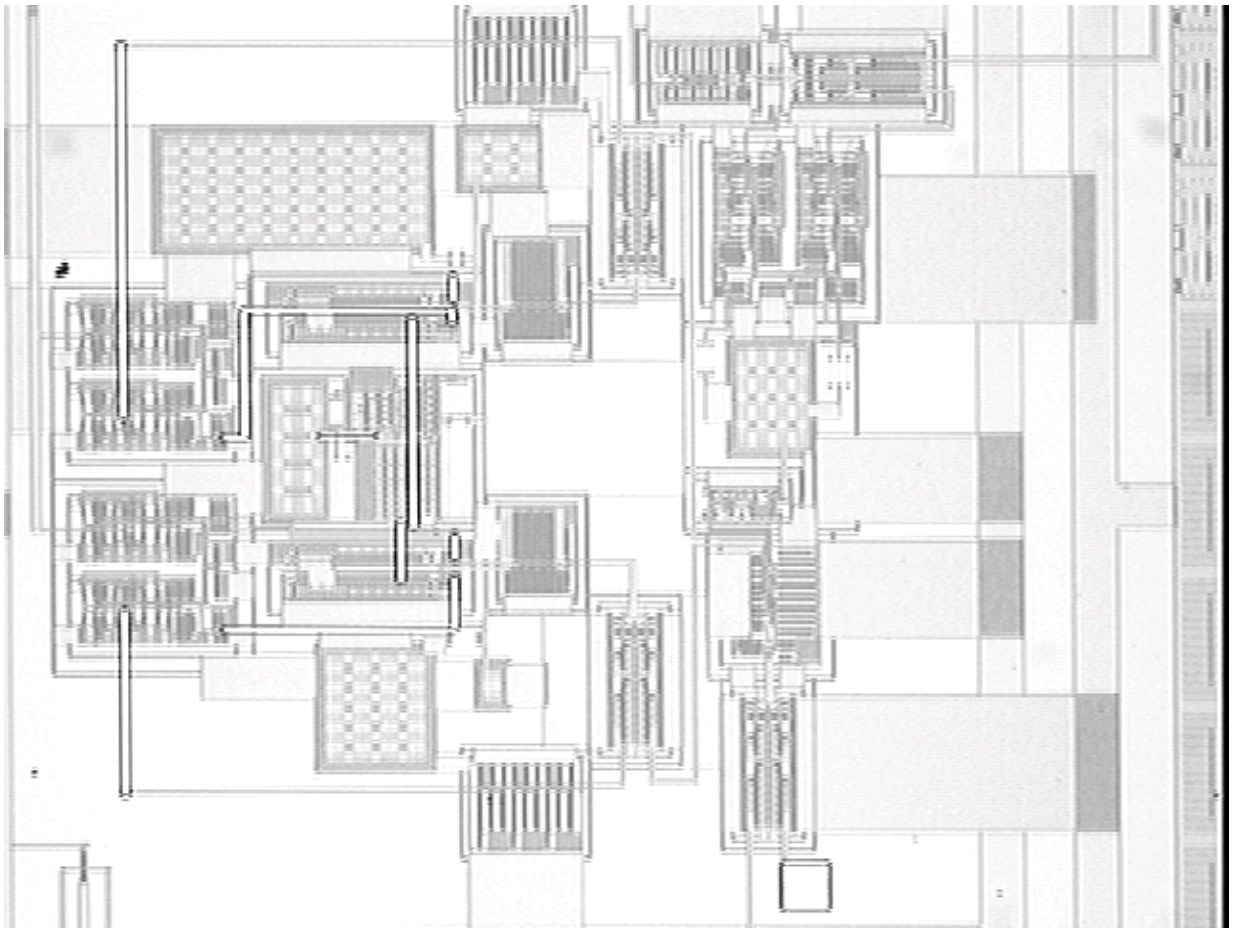


Figure 3.16: Microphotograph of fabricated switchable PLL.

CHAPTER 4

HOT CARRIER AND NEGATIVE BIAS TEMPERATURE INSTABILITY STUDIES ON LOW POWER PHASE-LOCKED LOOP WITH LC VCO AND DUAL-MODULUS PRESCALER

Phase-locked loops have been widely utilized in high speed communication systems. In wireless systems, low phase noise and precise channel spacing are in highly demand [61]. The demand for low cost and low power frequency synthesizers is also increased tremendously. Most frequency synthesizer designs use BiCMOS technology to achieve required low power consumption and high operation frequency [62, 63].

A low power and high speed PLL frequency synthesizer design is presented in 0.5 μm n-well tripple-metal double-poly CMOS technology. Voltage controlled oscillator and divider are the two essential parts in data communication systems which are responsible for large power dissipation in a PLL chip. In this work, LC VCO and dual-modulus prescaler with CML D flip-flops design styles are similar to design proposed in [64-67]. The PLL chip includes digital correction circuits, phase and frequency detector (PFD), charge pump (CP), LC VCO and prescaler blocks and is designed for a short lock-in time in 900 MHz-1.2 GHz range.

Hot carrier effects on n-MOSFETs and effects of NBTI on p-MOSFETs have been extensively characterized and their influences on analog and digital CMOS circuits have been addressed in [68,69]. There is not much reported work on the performance of LC VCOs under HC and NBTI effects for PLL circuits. In the present work, an attempt has been made to study effects of HC and NBTI on the performance of the LC VCO circuit used in the programmable PLL frequency synthesizer.

4.1 Designs of Phased-Lock Loop Circuits

Figure 4.1 shows the block diagram of a PLL consisting of PFD, CP, VCO, loop filter and dual-modulus prescaler. XO is the crystal oscillator circuit. The clock signal passes the divider-by-M circuit to generate reference clock. The divider in the feedback path is built by two counters and a dual modulus prescaler. The two counters, Main Counter and Swallow Counter, are set with B and A where A<B [70]. When the Mode Control is set to high and the prescaler is set to divide the clock signal from the VCO output by P+1, the two counters will count down until Swallow Counter reaches zero. The Mode Control signal is set to low. The prescaler divider ratio is set to P. Thus, the VCO output clock is divided by (P+1) A times and by P (B-A) times. The total factor of the divider is: N = PB+A. The VCO output frequency is: $f_{out} = Nf_{ref}$.

In the design, the main counter is an 11-bit counter and the divider ratio can reach 2047 and the Swallow Counter is a 7 -bit counter with divider ratio 127. Thus, the maximum divider ratio N = PB + A = 131135 where P=64, B=2047 and A=127 for 64/65 prescaler or N = 262143 where P=128, B=2047 and A=127 for 128/129 prescaler.

Figure 4.2 is a fully differential LC VCO and includes inductors, varactors, two cross-coupled differential pairs and p-MOSFET load resistors. The oscillation frequency range is 900 M Hz - 1.4 GHz. Figure 4.3 shows the layout of a 5nH inductor. Spiral inductor is an important component in the design of RF integrated circuits. The inductor designed in this paper is an on-chip integrated square spiral inductor as proposed in [71, 72].

Figure 4.4 is the schematic of a Dual-Modulus Prescaler made by CML D flip flop. It has three parts: Synchronous Frequency Divider-by-4/5, Asynchronous Counter and Control Logic. The prescaler divider ratio can be 64/65 or 128/129 which is switched

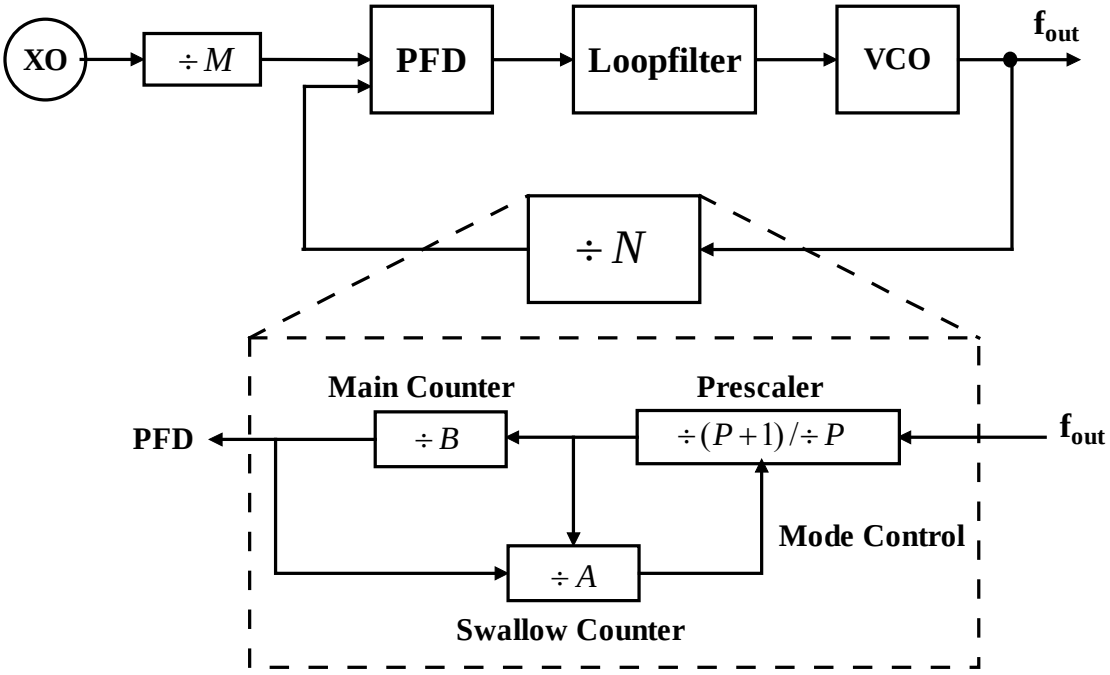


Figure 4.1: Programmable PLL building blocks.

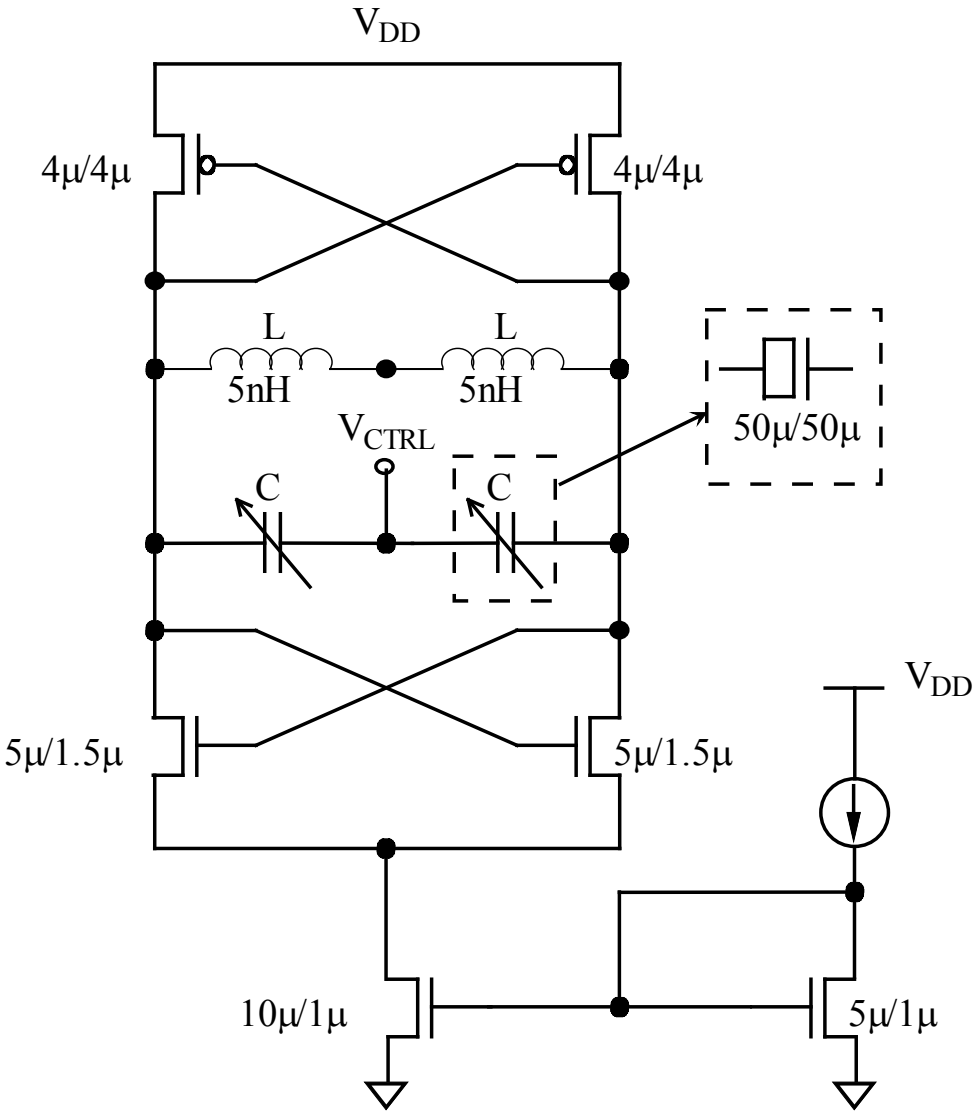


Figure 4.2: LC VCO Design.

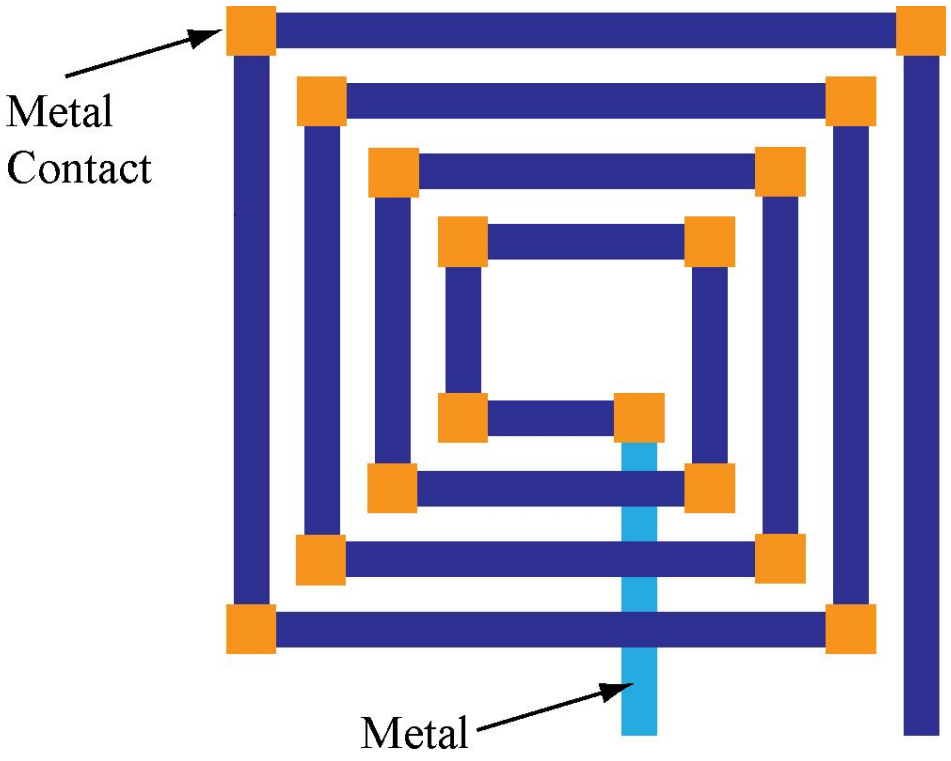


Figure 4.3: Layout of on-chip integrated square spiral inductor design.
Note: Top level metal is used in inductor design for reduced parasitics.

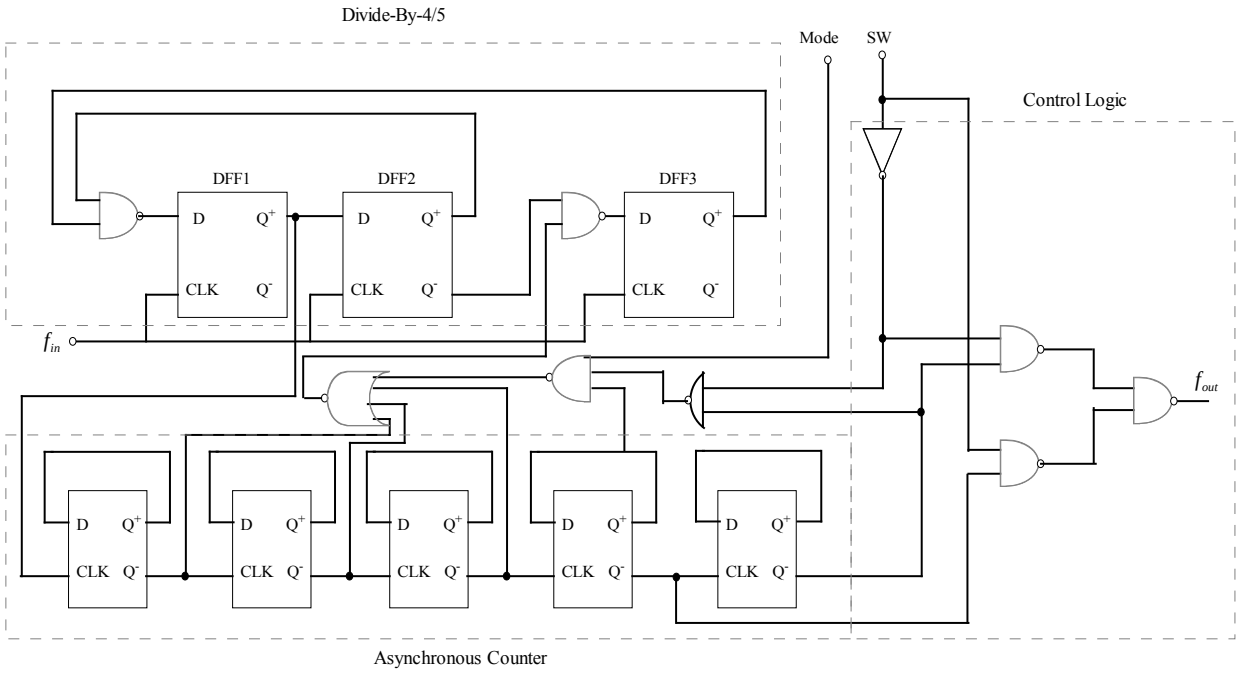


Figure 4.4: Schematic of the dual-modulus prescaler.

by the SW control signal. When MD is high, the divider ratio is 4; when MD is low, the divider ratio is 5. The SW signal controls the total divider ratio: 128/129 or 64/65 and Mode signal controls different divider ratios 128 or 129, 64 or 65.

Synchronous divider-by-4/5 is the essential part of the prescaler since it decides the highest speed which the prescaler can reach and the power consumption of the circuit. Synchronous divider-by-4/5 is built by 3 D flip-flops and 2 NAND gates as proposed in [73-76].

Figure 4.5 shows the design of the CML D flip-flop used in the divide-by-4/5 circuit. The D flip flop is modified from the CML D flip-flop latch with a resistive load [67]. The high speed switching and the low power consumption are achieved by the transistors sizes and the load resistances.

Figure 4.6 shows the 3rd order low pass loop filter schematic. The transfer function of the loop filter is given by [77],

$$Z(s) = \frac{1 + s \cdot T_2}{s \cdot C_{tot} \cdot (1 + s \cdot T_1) \cdot (1 + s \cdot T_3)} \tag{4.1}$$

The parameters in Eq. (4.1) are described as follows:

$$T_2 = R_2 \cdot C_2$$
$$C_{tot} = C_1 + C_2 + C_3$$
$$T_1 = \frac{R_2 \cdot C_2 \cdot C_1}{C_{tot}}$$
$$T_3 = R_3 \cdot C_3$$

Figure 4.7 shows the crystal oscillator circuit schematic. A crystal can be attached to OSCIN and OSCOUT terminals to generate the oscillation signal. FOSC terminal is the output signal of the crystal oscillator. The circuit is built by a resistor and an inverter connected in parallel. The signal output is FOSC.

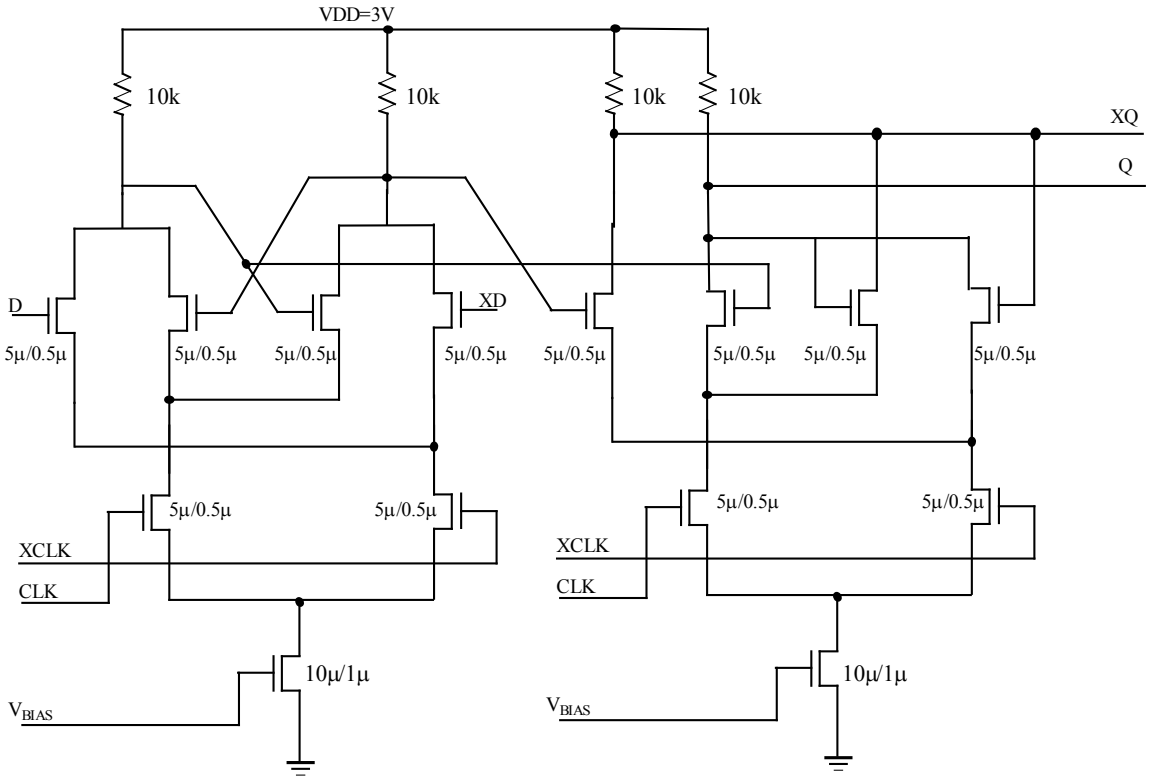


Figure 4.5: CML D flip-flop schematic. All transistors are n-MOSFETs.

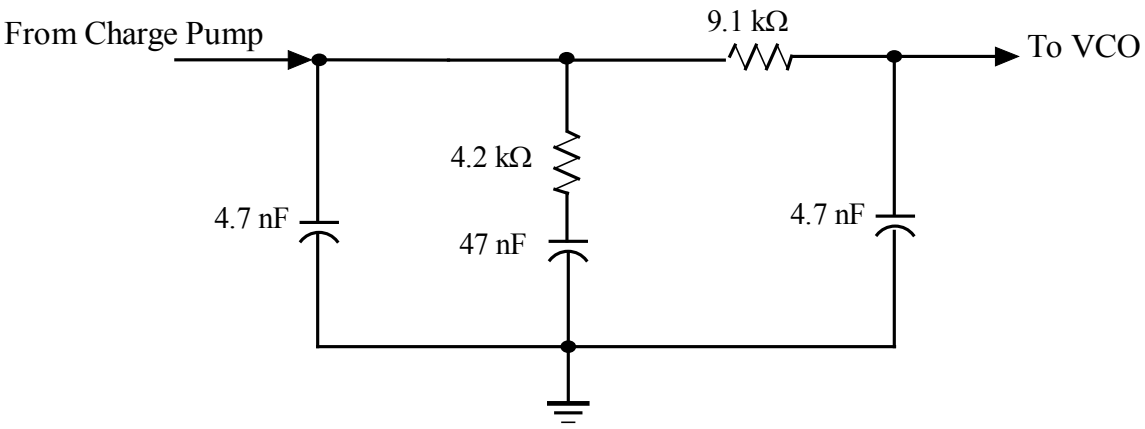


Figure 4.6: Loop filter circuit schematic.

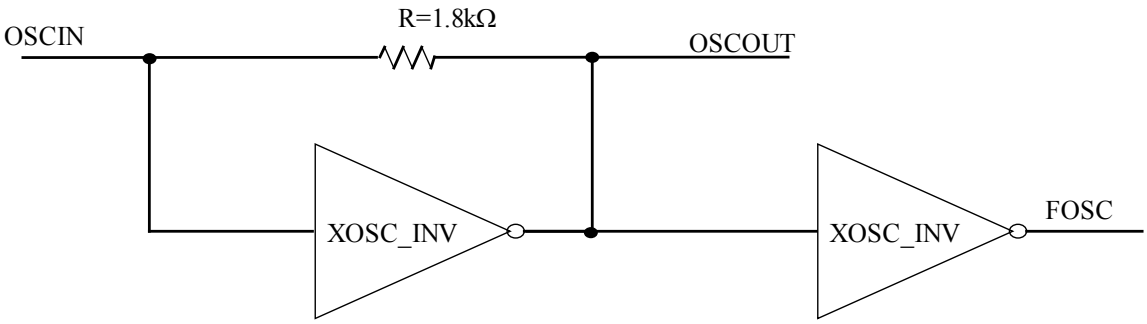


Figure 4.7: Crystal oscillator circuit.

4.2 Digital Design of Frequency Synthesizer

Programmable PLL uses shift register to control the main counter and swallow counter in precaler. All the data is read to the 19-bit Shift Register. CNT is the control bit which controls the divider to be selected. In Table 4.1 (a), when CNT is high, the clock is read for the reference divider M. The data flowing into divider M is controlled by R1-R14. SW is the divider ratio setting bit for the prescaler (64/65 or 128/129). FC is the phase control bit for the phase comparator. LDS is the LD/f_{out} signal select bit which can select the output signal. CS is the charge pump current select bit which can select 1.5 mA or 6mA. In Table 4.1 (b), when CNT is low, the clock is read for the programmable divider A and B. A1- A7 are for the 7-bit counter and A and N1- N11 are for the 11-bit counter B in divide-by-N.

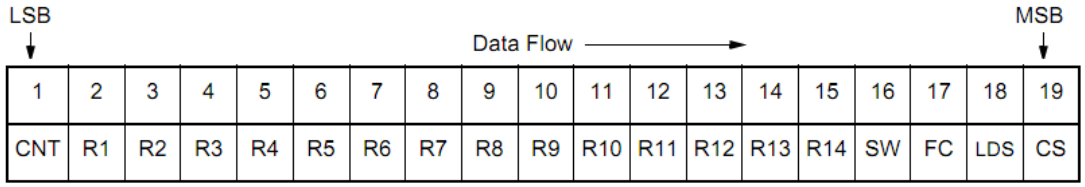
Table 4.2 (a) shows the maximum divider ratio provided by divider M. Table 4.2 (b) and (c) show the binary 11-bit programmable counter B maximum divider ratio and the binary 7-bit swallow counter A maximum divider ratio. From Figure 4.1, the total divider ratio for the prescaler divider is N = PB + A = 131135 for P = 64 and N = PB + A = 262143 for P =128.

4.3. Hot Carrier Stress and NBTI Effects on LC VCO

4.3.1 Hot Carrier Stress on Varactor and LC VCO

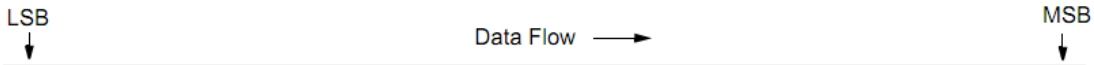
Hot carrier stress has a significant effect on CMOS devices in today's submicron technology. Hot carrier stress causes device degradation such as the increase of threshold voltage and the decrease of electron mobility [78]. An empirical model for the device degradation, which is the shift in threshold voltage, has been studied in [79]. The increase of threshold voltage is described as follows,

Table 4.1 (a). Programmable shift register with CNT high



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS	CS

Table 4.1 (b). Programmable shift register with CNT low



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

Table 4.2 (a). Binary 14-bit programmable references counter data setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 4.2 (b). Binary 11-bit programmable counter data setting

Divide ratio (N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Table 4.2 (c). Binary 7-bit swallow counter data setting

Divide ratio (A)	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

$$\Delta V_{th} = At^m \tag{4.2}$$

In Eq. (4.2), A is the degradation constant, which is strongly affected by the drain stress voltage. The parameter *m* in Eq. (4.2) which is the slope of log-log plot of V_{th} shift versus stress time, is strongly affected by the drain stress voltage.

The oscillation frequency of LC-VCO is given by,

$$f_0 = 1/2\pi\sqrt{LC}\,. \tag{4.3}$$

In Eq. (5.3), *L* is the inductor value and C is the varactor capacitance.

The varactor is an n-MOSFET device with drain and source connected as one node and the gate is the other node of the varactor. Hot carrier can be injected from the control voltage to the two varactors. The CV curve of the n-MOSFET of each varactor is shown in Figure 4.8. The CV curve of the n-MOSFET of each varactor under 4-hour hot carrier stress is also shown in Figure 4.8 for comparison. It is clearly shown that MOSFET capacitance shifts toward left by 0.4V.

The Cadence/Spectre simulations on the proposed 1.2GHz CMOS LC VCO are performed in 0.5 μm double poly triple metal CMOS technology. Figure 4.9 shows the VCO output frequency gains before and after 4-hour hot carrier stress. The frequency gain before stress is more linear than that after stress. The VCO output frequency gain increases about 100 MHz after the hot carrier stress. The frequency gain of the VCO is 100 MHz without hot carrier effect.

Figure 4.10 shows the LC VCO output phase noise with and without hot carrier stress. It is shown that the VCO phase noise increases by nearly 1 dBc/Hz between 100 Hz and 1 kHz and increases more along the offset frequency after 4 hours hot carrier stress. VCO phase noise increases close to 5 dBc/Hz at 10 kHz offset frequency.

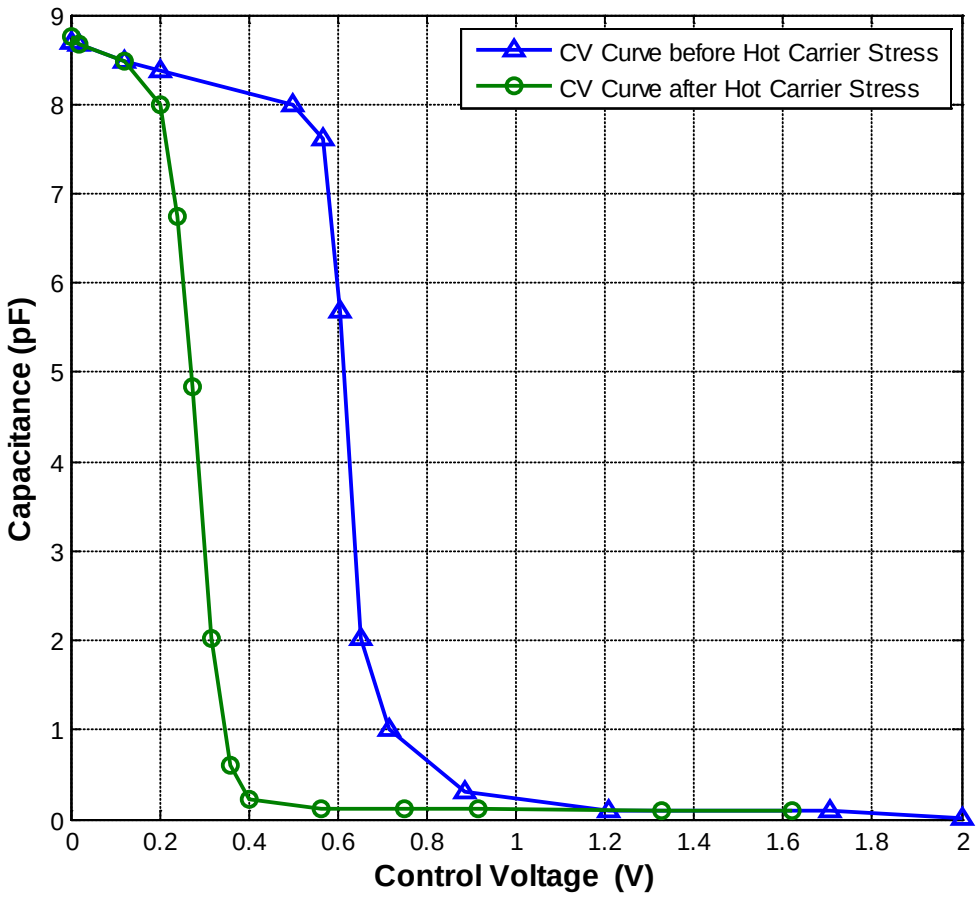


Figure 4.8: The CV curve of the n-MOSFET varactor with and without hot carrier effect.

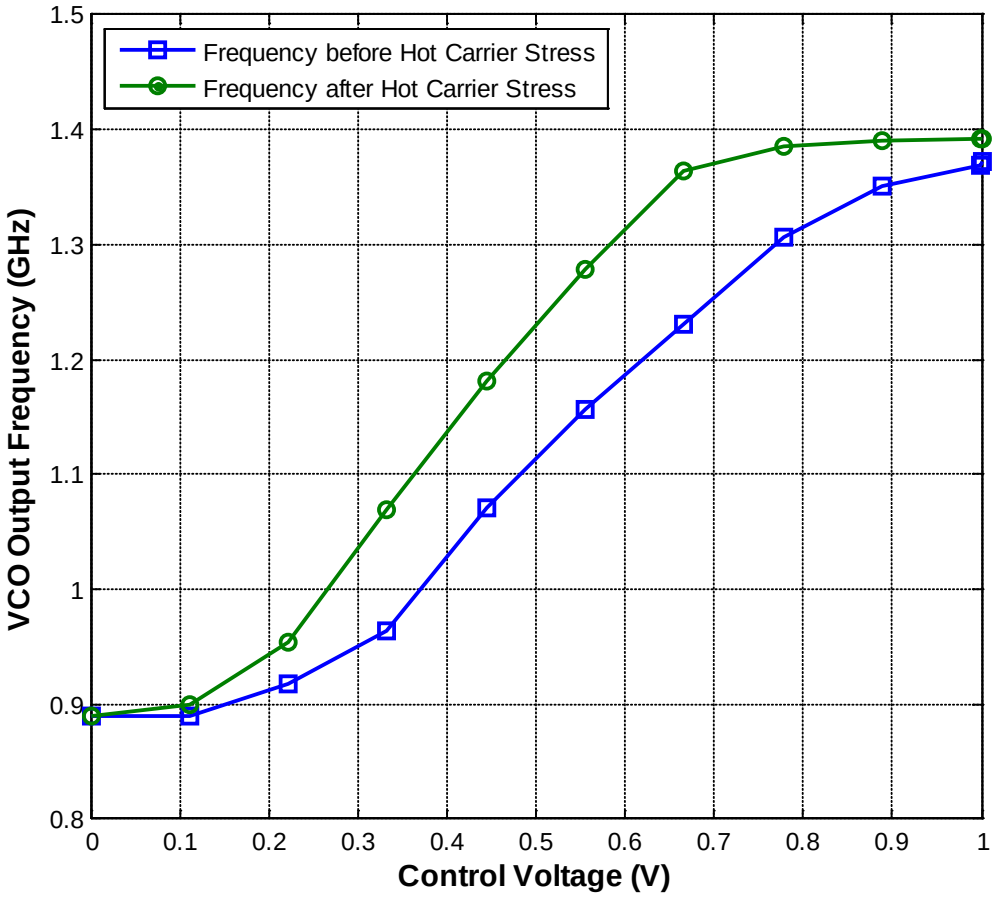


Figure 4.9: LC VCO frequency with and without hot carrier stress.

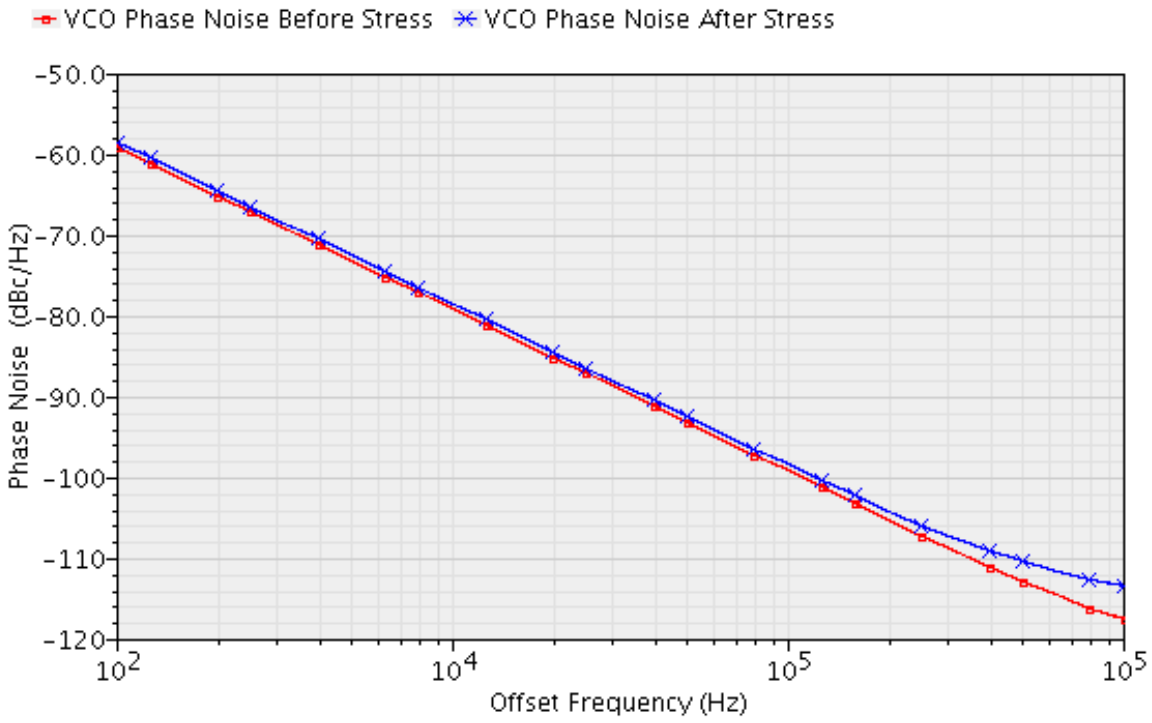


Figure 4.10: LC VCO phase noise with and without hot carrier stress.

4.3.2 NBTI Effects on LC VCO

The NBTI is another important reliability issues in CMOS technology. Like hot carrier effect in n-MOSFET devices, NBTI is more common in p-MOSFETs. The degradation of the threshold voltage model due to NBTI is shown below [56],

$$\Delta V_t = A\exp(\beta V_{GS} - \frac{E_a}{kT})t^n \tag{4.3}$$

where *A*, β and E_a are determined from fitting parameters and the values are 1, 0.75 and 0.145 eV for 0.5 μm CMOS technology. The constant n is between 0.19-0.26 for the submicron device and k is the Boltzmann constant. V_{GS} is the gate to source voltage, t is the stress time and n is the power law dependence of NBTI which is equal to 0.19.

The following equations illustrate the effect of threshold voltage shift on drain current and the phase noise [36].

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{SG} - |V_t| - \Delta V_t)^2 \tag{4.5}$$

where μ is the electron mobility, C_{OX} is gate oxide capacitance, W/L is the channel width-length ratio of n-MOSFET which decides the frequency of VCO output and V_t is the threshold voltage.

$$S_\Phi(\omega_m) = \frac{FkT(\pi\omega_o)^2}{32k_1(QR\omega_m)^2}\cdot\frac{1}{I_D^2} \tag{4.6}$$

The following equation describes phase noise $S_\Phi(\omega_m)$ of the VCO [36]. $S_\Phi(\omega_m)$ represents the phase noise of the VCO. F is the noise figure and k is the Boltzmann constanct. R is the parasitic resistor in inductor and I_D is the drain current. ω_o/Q is

bandwidth of the VCO and ω_m is the offset frequency. The phase noise increases with the decrease in I_D.

Figure 4.11 shows the drain current degradation versus the stress time across the two p-MOSFETs load in LC VCO of Figure 4.2. The drain current decreases from 8.4 μA to 4.5 μA. Figure 4.12 shows the phase noise degradation of LC VCO under 4-hour NBTI effect. The phase noise remains the same as that before 100 kHz offset frequency but it increases from that before stress when the offset frequency is larger than 100 kHz offset frequency. It shows that the phase noise is -105 dBc/Hz after NBTI stress and is -114 dBc/Hz before the stress at 1MHz.

4.4 PLL Post Layout Simulations and Results

Since crystal oscillator is a 10 MHz signal and reference input divider ratio M is set to 800, the input reference frequency is 12.5 kHz. The divide-by-N ratio is selected to be 96,000 to achieve 1.2 GHz PLL output frequency if the input reference is 12.5 kHz. The loop bandwidth is 1.15 kHz and the phase margin is 50^o. The power supply of the chip is 3V. The total power consumption is under 30 mW obtained from Cadence/Spectre simulations.

Figure 4.13 shows the chip layout of the programmable PLL frequency synthesizer. The 1.2 GHz PLL differential output is shown in Figure 4.14. The voltage swing of the PLL output is from 1.36V to 1.72V and the swing is about 0.36mV.

4.5 Experimental Results

Figure 4.15 shows the measurement setup for PLL power spectrum and phase noise. The PLL output is connected to a power splitter to fulfill the impedance match. The other ends of the power splitter are connected to the divider and the spectrum analyzer.

Figure 4.16 (a) shows the power spectrum density of the PLL output. The PLL output frequency is 1.2GHz as shown in the figure and the carrier power is -29 dBm which is 0.001 mW. Figure 4.16 (b) shows the power spectrum density of the PLL output with 4 hour hot carrier stress and it shows the carrier power of -34 dBm which is decreased by about 5 dBm.

Figure 4.17 (a) shows the phase noise measurement of the PLL output. The in-band phase noise is -66.67 dBc/Hz at 10kHz offset frequency and phase noise reaches -120dBc/Hz at 1MHz offset frequency. Figure 4.17 (b) show the phase noise after 4 hour NBTI stress and the in band phase noise increase to -65.39 dBc/Hz at 10kHz offset frequency. The difference is around 1.3 dBc/Hz before and after NBTI stress with on-chip measurement.

4.6 Conclusion

The low power design of a 3V 30mW PLL frequency synthesizer designed in 0.5 μm CMOS process is presented. The divider design is a two modulus prescaler built from CML D flip-flops. The divider has a Main Counter, a Swallow Counter and Control Logic. The on-chip inductor and n-MOSFET varactors are used in the LC VCO design. The LC VCO can work from 0.9 GHz to 1.4 GHz. The device degradation issues on both hot carrier stress and NBTI effect are studied in the LC VCO. The PLL output frequency can achieve 1.2GHz.

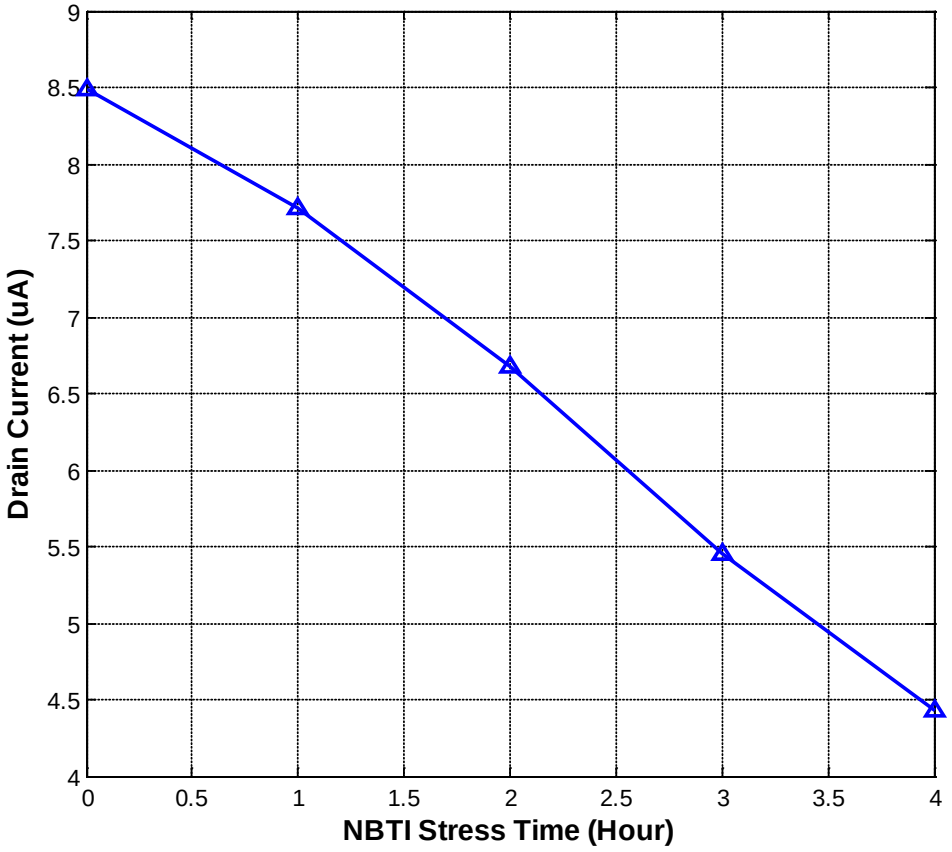


Figure 4.11: Drain current versus stress time.

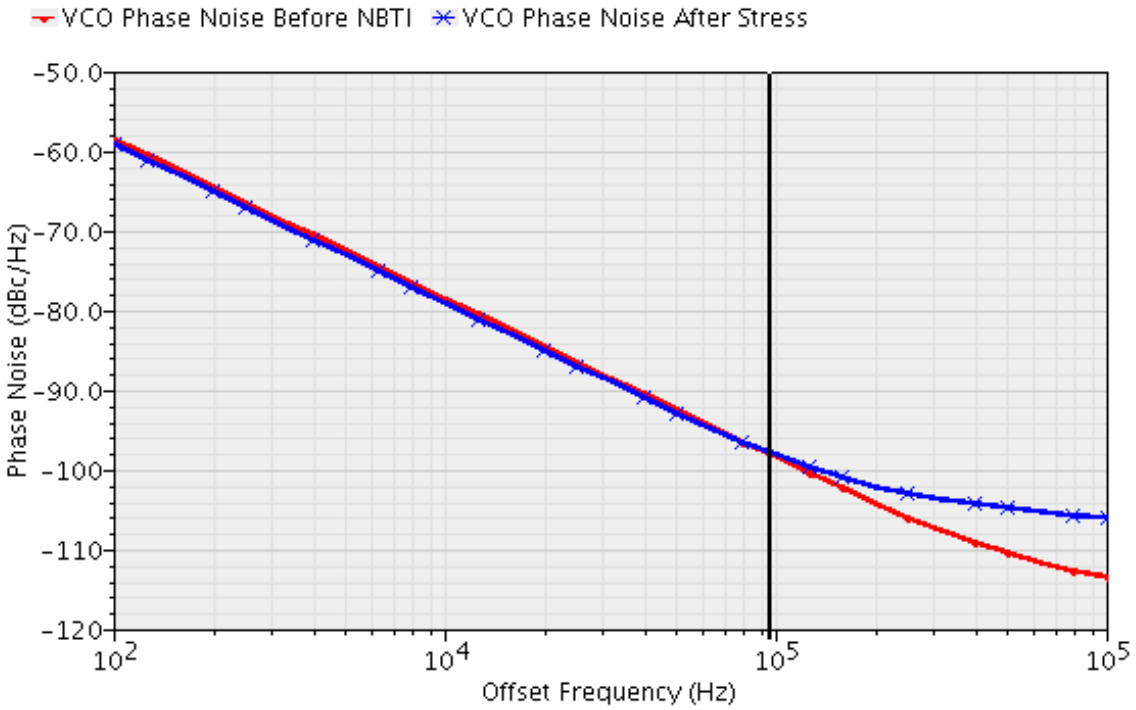


Figure 4.12: LC VCO phase noise with and without NBTI stress.

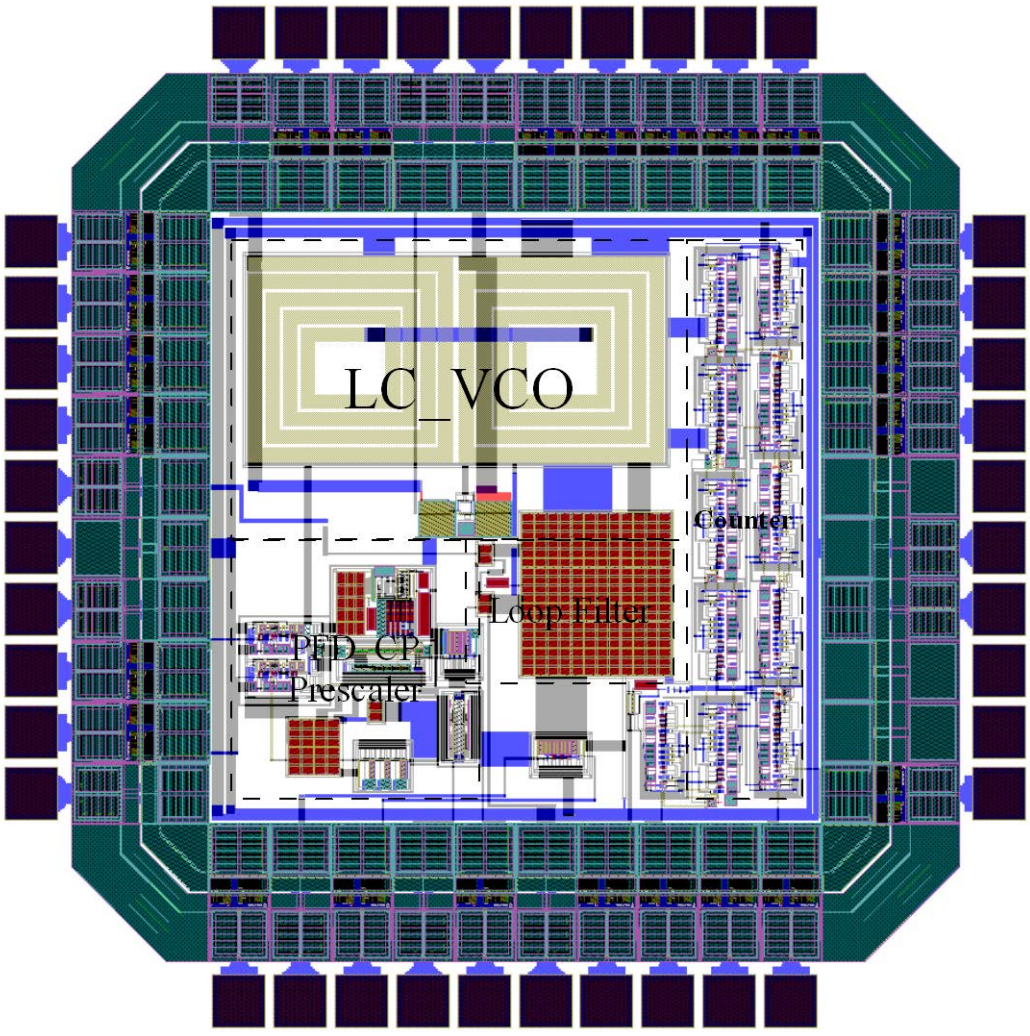


Figure 4.13: Layout of the PLL frequency synthesizer.

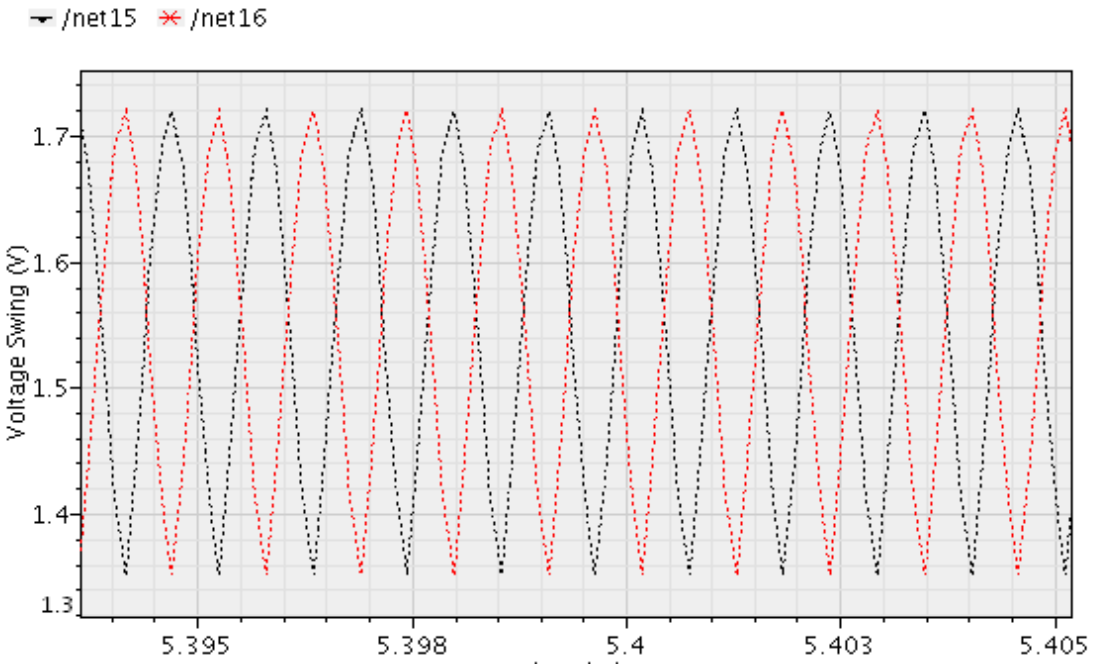


Figure 4.14: PLL frequency synthesizer differential output clocks.

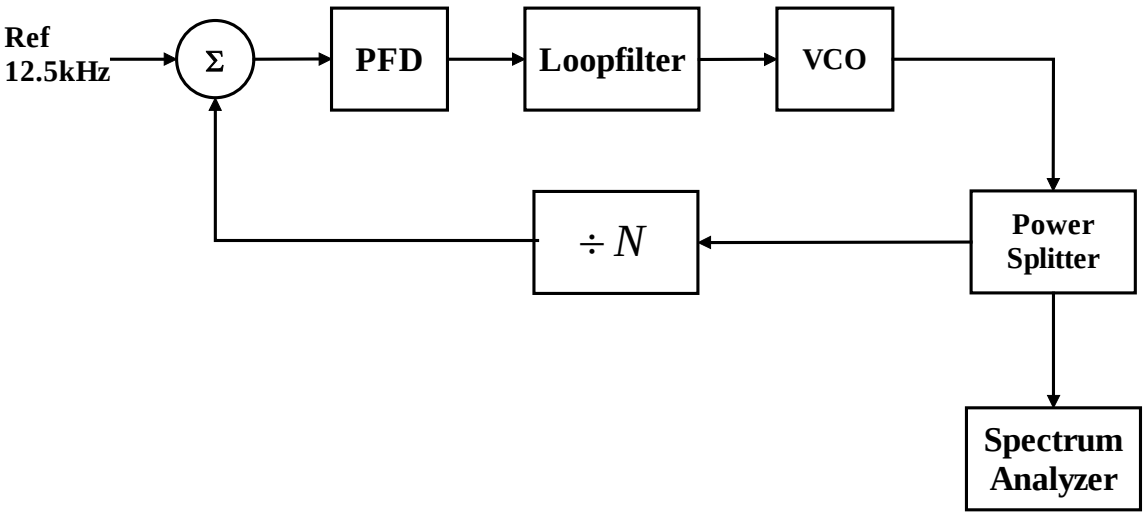


Figure 4.15: The spectrum measurement setup.

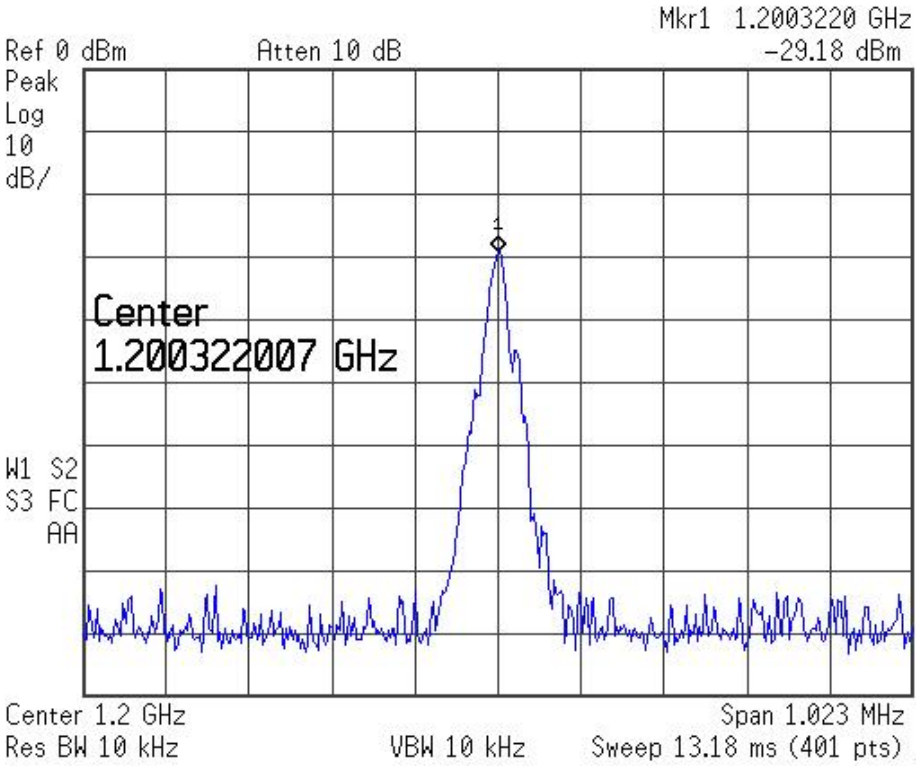


Figure 4.16 (a): Power spectrum density measurement without hot carrier effect.
Note: The Y axis scale is -10dB per grid from Ref 0 dBm.

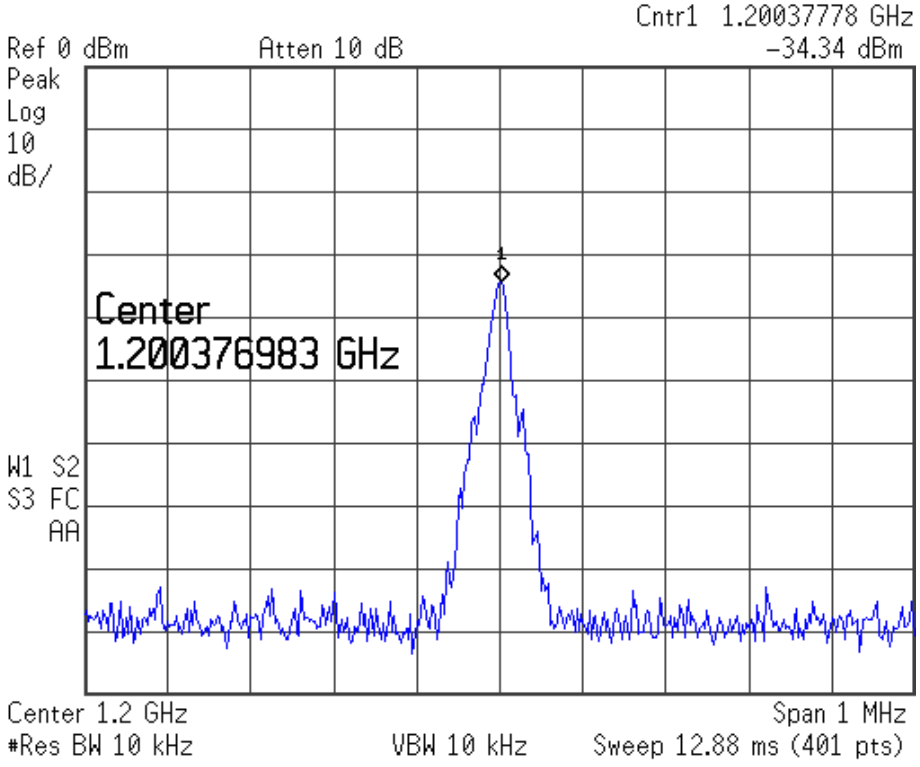


Figure 4.16 (b): Power spectrum density measurement with hot carrier effect.
Note: The y axis scale is -10dB per grid from Ref 0 dBm.

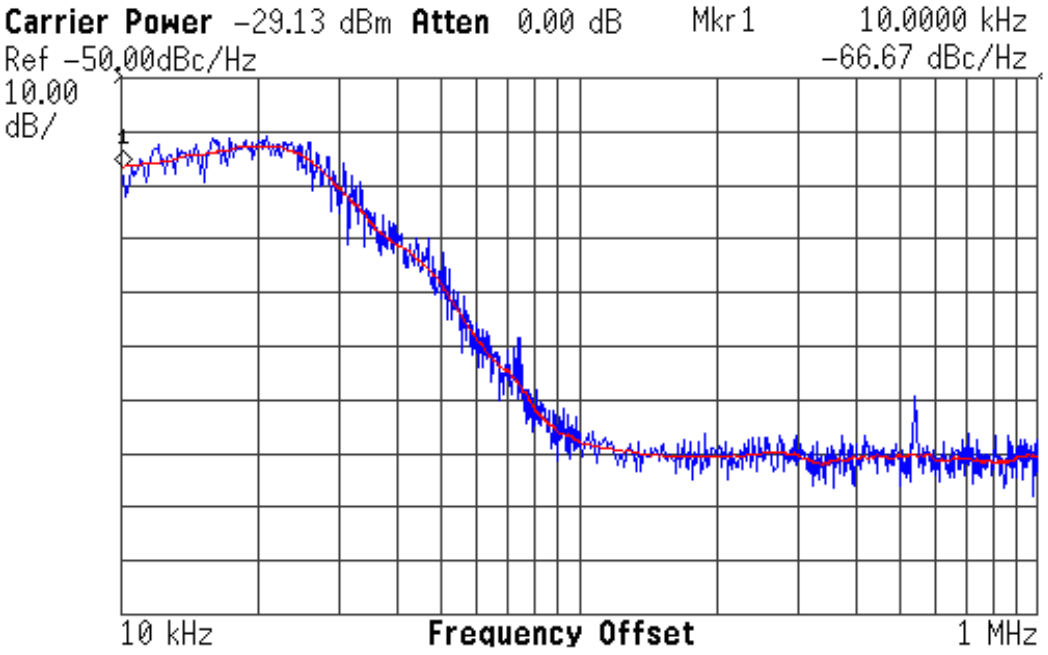


Figure 4.17 (a): PLL output phase noise without NBTI.
Note: The y axis scale is -10dB per grid from Ref -50dBc/Hz.

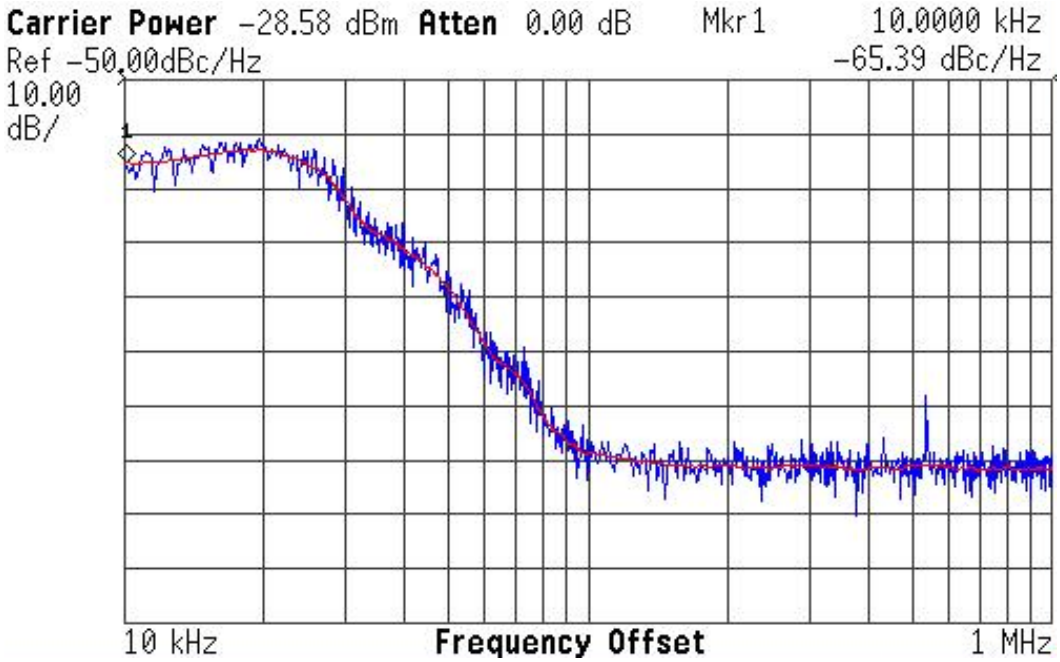


Figure 4.17 (b): PLL output phase noise with NBTI.

Note: The y axis scale is -10dB per grid from Ref -50dBc/Hz.

CHAPTER 5

CMOS LC VOLTAGE-CONTROLLED OSCILLATOR AND PLL DESIGNS USING MULTIWALLED CARBON NANOTUBE WIRE INDUCTOR*

Commonly used VCO employ LC tuned circuit where quality factor of the inductor becomes crucial to the operation of the oscillator. In the past, inductor has been realized from bonding wires to retain large quality factor [80]. With shrinking device geometries and packaging requirement on-chip inductors have been realized for radio frequency integrated circuits using Al and Cu metallization. Recently Salimath [81] has reviewed the design of several CMOS voltage controlled oscillators and presented an on-chip 1.1 to 1.8 GHz VCO implementation in CMOS for use in RF integrated circuits. However, achieving high-Q inductor is still being researched.

The one-dimensional carbon nanotubes have been extensively researched for numerous applications including in electronics since its discovery in 1991 [82]. It has been demonstrated that the carbon nanotube wire is very likely to replace the Cu interconnect in sub-nanometer CMOS technologies [83]. It has also been shown that CNT

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*Part of the work is reported in the following publications:

1. A. Srivastava, Y. Xu, Y. Liu, A. K. Sharma, and C. Mayberry, "CMOS LC voltage-controlled oscillator design using carbon nanotube wire inductor," *Proc. 5th IASTED International Symposium on Circuits and Systems*, Maui, Hawaii, USA, pp. 171-176, August 23 – 25, 2010.

2. A. Srivastava, Y. Xu, Y. Liu, A. K. Sharma, and C. Mayberry, "CMOS LC voltage-controlled oscillator design using multiwalled carbon nanotube wire inductor," *Proc. IEEE International Symposium on Electronic System Design (ISED)*, Bhubaneswar, India, December 20-22, 2010.

3. A. Srivastava, Y. Xu, Y. Liu, A.K. Sharma, and C. Mayberry, ''CMOS LC voltage controlled oscillator design using carbon nanotube wire inductors," *ACM Journal on Emerging Technologies in Computing Systems*, accepted (2011).

wire has reduced skin effect compared to metal conductors such as the Cu and has a great promise for realization of high-Q on-chip inductors for RF integrated circuits [84]. Several models of CNT based on-chip inductor have been presented in the literature [84-87].

Phase-locked loops operating in 1-2 GHz range suffer from phase noise which results in degradation in performance of RF systems. The LC VCO in PLL is the key contributor to the phase noise which uses metallic wire on-chip integrated inductor. The resistive losses lower the inductor Q-factor in such LC VCO design. Recently, Srivastava et al. [88] has proposed using CNT wire inductor for design of LC VCO circuits. We propose a new 2 GHz LC VCO design in TSMC 0.18 μm CMOS process using MWCNT wire as an inductor in LC tank circuit. We have applied our CNT interconnect model in a well-known π model [89] to study the properties of MWCNT wire on-chip inductors [88]. Q-factors are calculated for MWCNT wire inductor and Cu wire inductor for comparison. It is shown from Cadence/Spectre simulation studies that the LC VCO using MWCNT inductor wire provide significant enhancement in oscillation frequency and phase noise reduction in comparison to LC VCO using Cu wire inductor.

5.1. On-chip Inductor Modeling

Figure 5.1 shows the π-model of the on-chip inductor [89] applied to on-chip CNT wire inductor. Figure 5.2 shows the on-chip inductor layout in 0.18 μm CMOS technology. The inductor considered is a 4.5 turn planar spiral inductor which has the outermost diameter, D_{out} = 250 μm, conductor width, W = 15 μm, conductor thickness, t = 2 μm, conductor spacing, S = 1.5 μm, and oxide and substrate thicknesses of 4 nm and 300 μm, respectively. The Q factor analysis results are shown in Fig. 5.3. The maximum Q factor of MWCNT (β=1) inductor can be ~200% higher than that of the Cu inductor. This

significant enhancement in Q factor arises not only because of the lower resistance of CNTs but also because of negligible skin effect in CNT wire [90].

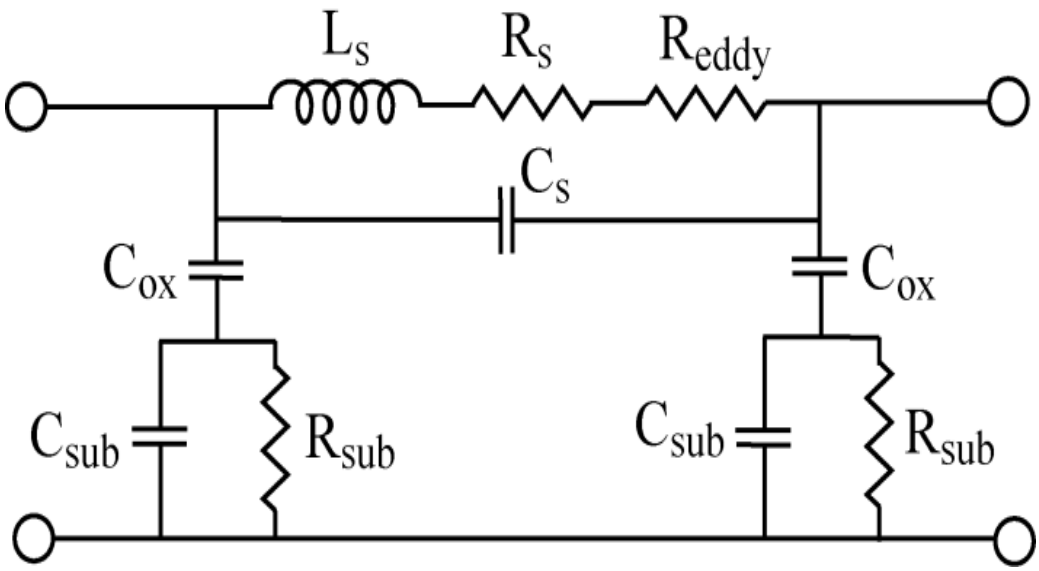

Figure 5.1: π-model of on-chip inductor.

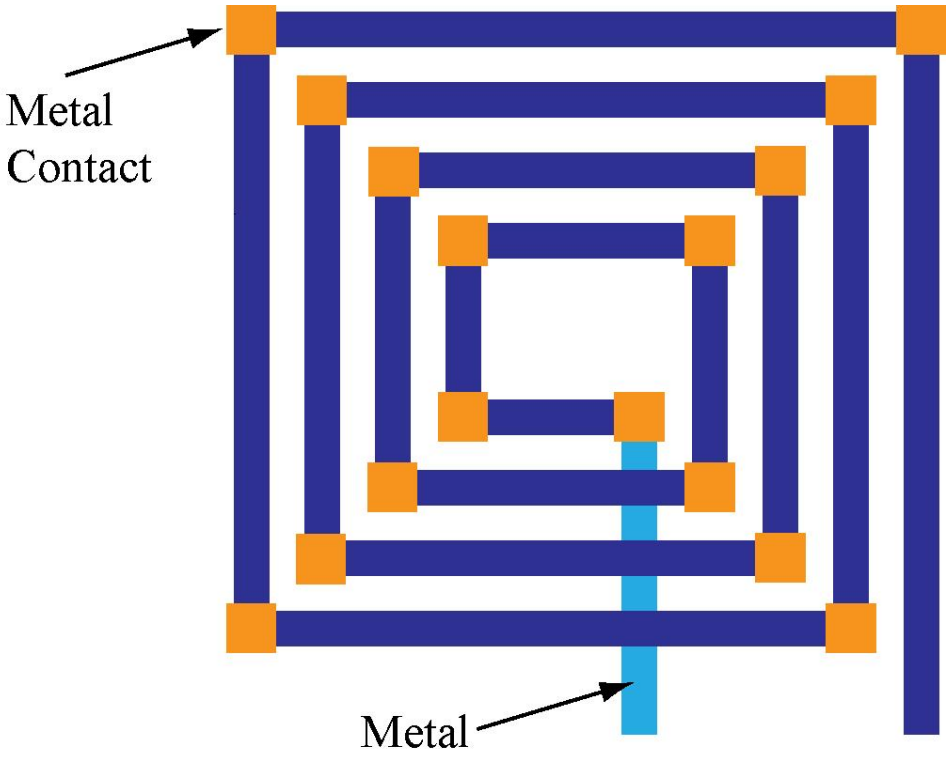

Figure 5.2: Layout of on-chip integrated square spiral inductor design.
Note: Top level metal is used in inductor design for reduced parasitics.

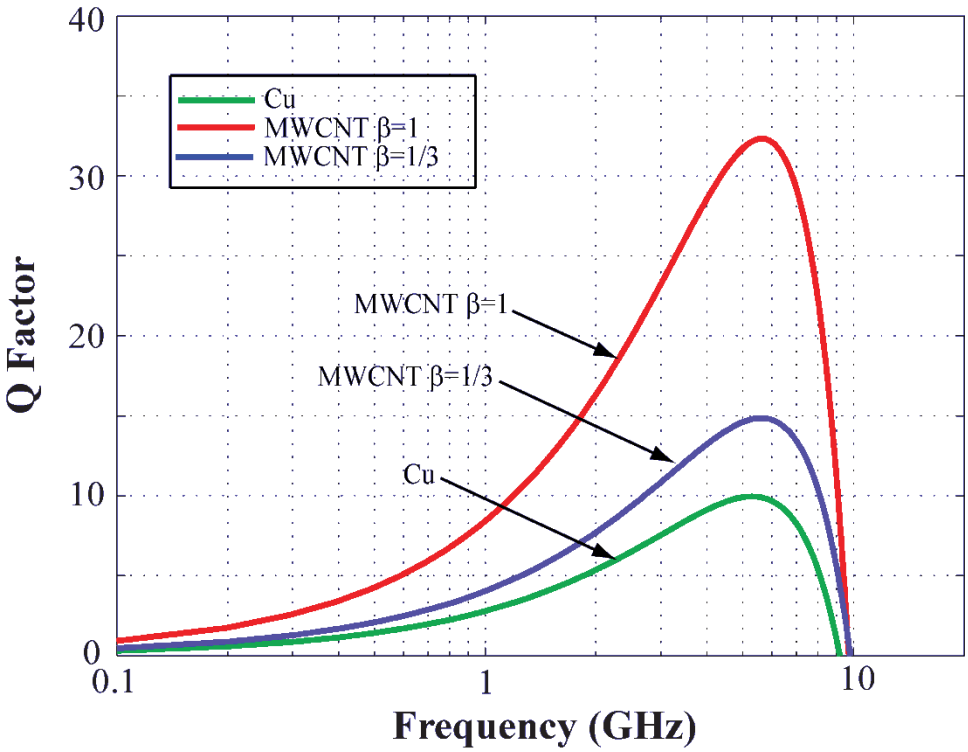

Figure 5.3. Q-factor of inductors based on MWCNT and Cu.

5.2. LC Voltage-Controlled Oscillator (LC VCO)

An LC VCO consists of three components: LC tank, tail bias transistor and cross-coupled differential pair. LC tank is made by an inductor and a capacitor connected in cascade or in parallel. The resonance frequency of LC tank circuit is given by,

$$f_0 = 1/2\pi\sqrt{LC} \ . \tag{5.1}$$

When the tank is a purely resistive, the phase of the impedance is zero. Below the resonance frequency, the LC circuit is capacitive and above the resonance frequency, it is inductive.

Figure 5.4 shows the circuit diagram of a complementary cross-coupled differential LC oscillator with tail current. The symmetrical design of the VCO gives good phase noise performance and large voltage swing. The value of the inductor is chosen to be 2.5 nH. The varactor in the circuit of Figure 5.4 is implemented from an nMOSFET with source and drain tied together. The C-V curve of the varactor is shown in Figure 5.5. The voltage-controlled capacitance range is from 200 fF to 2.2 pF which makes the LC VCO to oscillate from 1.6 GHz to 3.3 GHz.

Figure 5.6 shows the LC VCO oscillation frequency versus control voltage for inductor with no losses (ideal), MWCNT (β=1, 1/3) wire inductors and Cu wire inductor. Here, β is the probability factor characterizing shell being metallic in a MWCNT. CMOS LC VCO with MWCNT (β=1) wire inductor oscillates between 1.3 – 2.5 GHz which is higher in comparison to oscillation frequency range 1.1 – 2.4 GHz of LC VCO with Cu wire inductor. It is also shown that VCO with MWCNT wire inductor (β=1) has higher oscillating frequency than that with Cu wire inductors. For example, oscillation frequency of MWCNT (β=1) wire inductor is higher by ~ 10% at 1.2 V than that with Cu inductor.

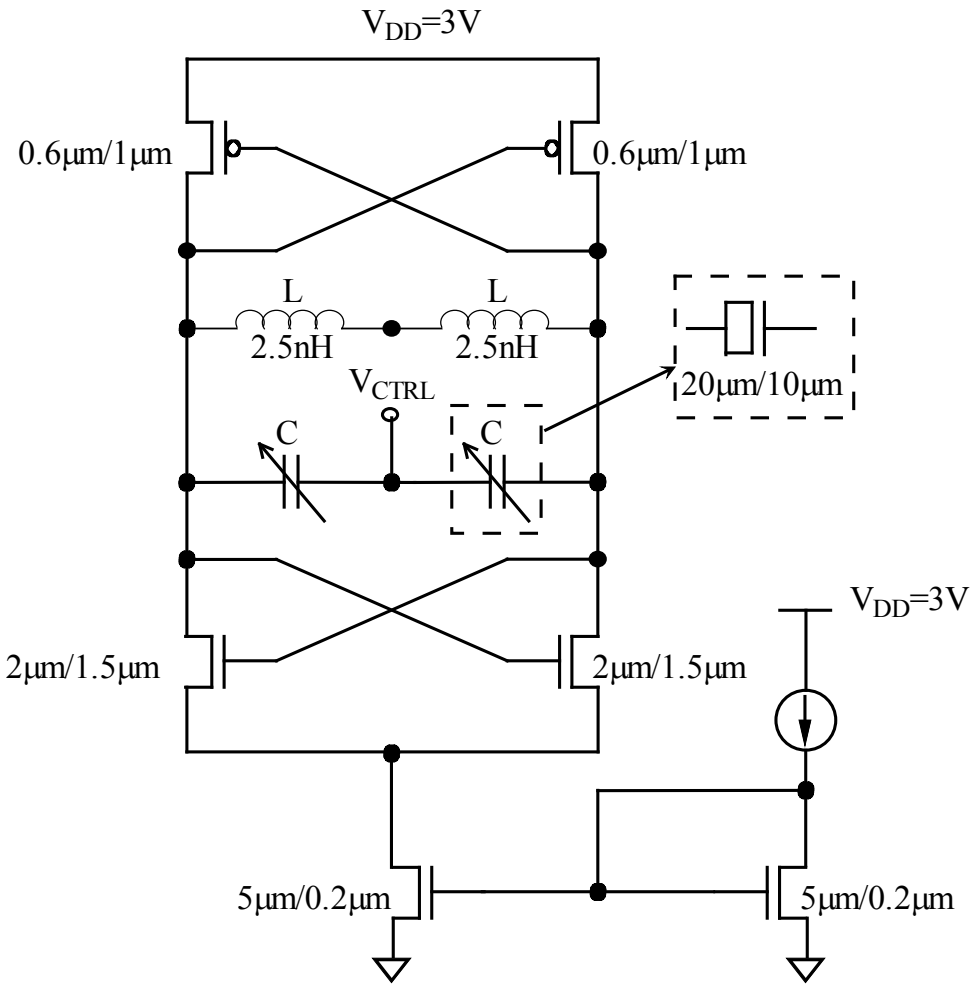

Figure 5.4. Circuit diagram of a LC VCO.

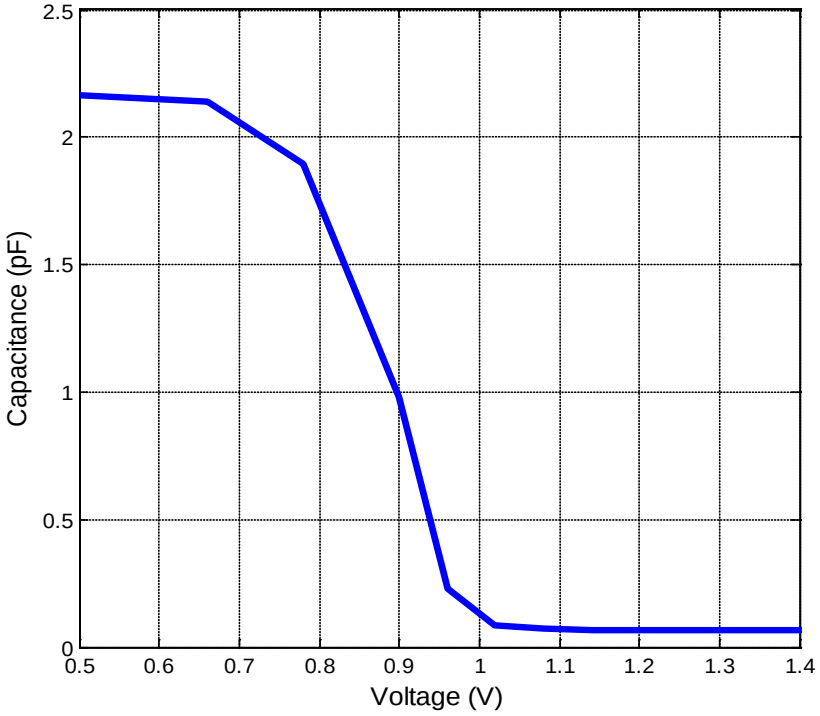

Figure 5.5. C-V curve of a varactor.

Moreover, at this 1.2 V control voltage, the Q factor of Cu inductor is 7 and Q factors of MWCNT inductors are 23 (for β=1) and 12 (for β=1/3), respectively. In addition, oscillating frequency is higher in VCO with MWCNT wire inductors for β=1 than that of β=1/3.

The noise is modeled by using the Leeson's phase noise density equation [91]:

$$L(\Delta f) = \left(\frac{1}{8Q^2}\right)\left(\frac{FkT}{P}\right)\left(\frac{f_0}{\Delta f}\right)^2 \quad (2)$$

where k is the Boltzmann's constant, T is the temperature, P is the output power, F is the noise factor, Q is the quality factor of the LC tank, f_0 is the oscillation frequency, and Δf is the offset frequency from f_0.

Figure 5.7 shows the phase noise of the LC VCO at 2 GHz tuning frequency. The VCO phase noise using inductor with no losses (ideal) is -70dBc/Hz at 10kHz offset frequency from the carrier and -123dBc/Hz at 10MHz offset frequency from the carrier. The VCO with MWCNT inductors has about 6 dBc/Hz smaller phase noise than that with Cu inductors. Moreover, at this 2 GHz tuning frequency, the Q factor of Cu inductor is 7 and Q factor of MWCNT inductors are 23 (for β=1) and 12 (for β=1/3). In addition, the phase noise is smaller in VCO with MWCNT inductors for β=1 than β=1/3.

5.3. PLL Phase Noise with MWCNT LC VCO

The working range of the MWCNT LC VCO is 1.3~2.5 GHz, The PFD, loop filter and the divider are modified. Figure 5.8 shows the block diagram of a PLL with MWCNT LC VCO. The inductor used in the design can be Cu or MWCNT wires. Figure 5.9 describes the phase noise performance of PLL with LC VCO designed using different types of inductors under 2 GHz PLL output frequency. Inductor types are with no losses (ideal), MWCNT (β=1, 1/3) wire inductors and Cu wire inductor. It is shown that the

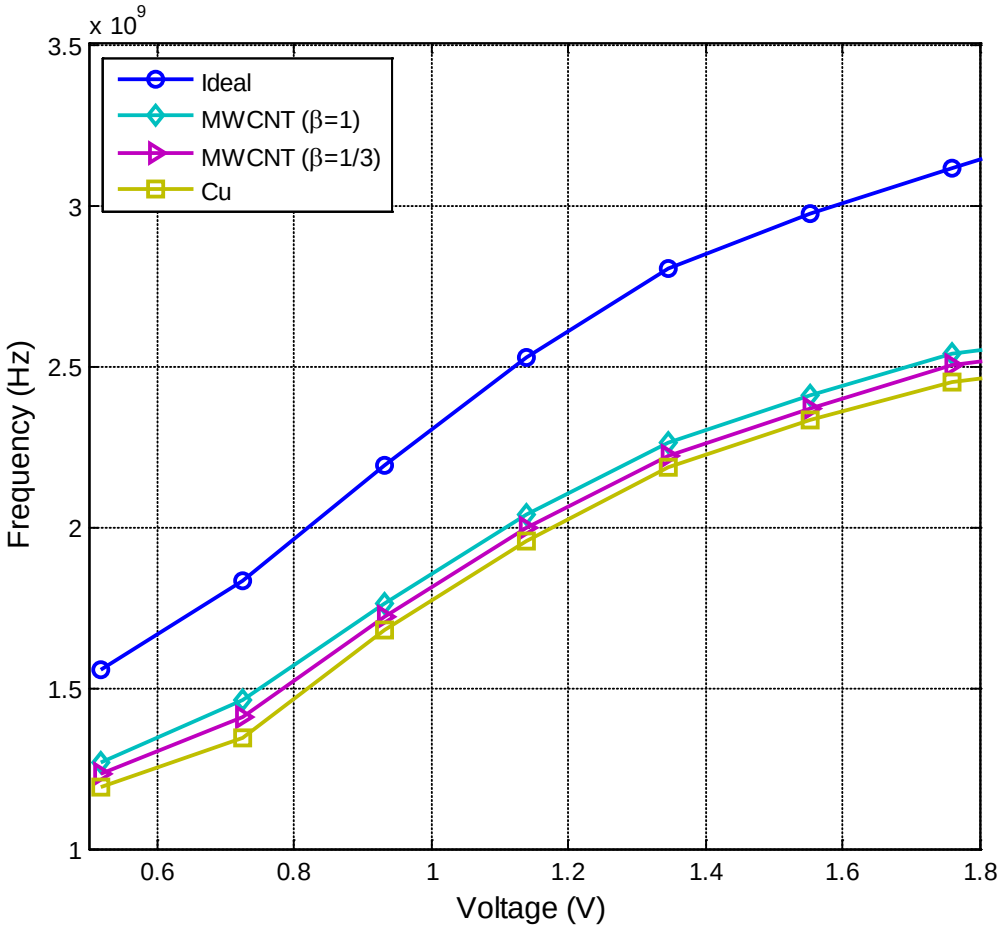

Figure 5.6. VCO oscillation frequency versus control voltage with different inductors.

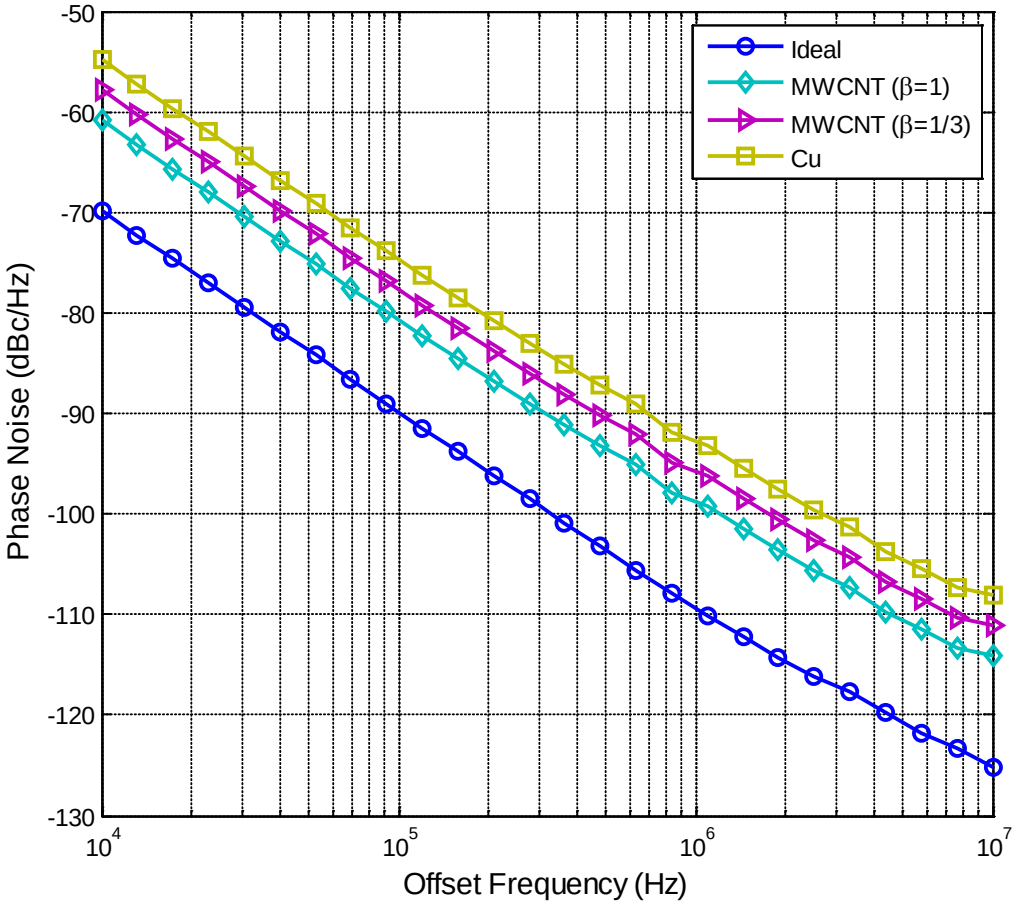

Figure 5.7. VCO phase noise versus offset frequency.

PLL output phase noise using inductor with no losses (ideal) is -79dBc/Hz at 10kHz offset frequency from the carrier and -123dBc/Hz at 10MHz offset frequency from the The PLL output phase noise using Cu wire inductor has highest phase noise performance. The PLL phase noise reaches -61 dBc/Hz at 10 kHz offset and -109 dBc/Hz at 10 MHz. Moreover, the PLL output phase noise is smaller in VCO with MWCNT inductors for $\beta=1$ than $\beta=1/3$. The phase noise decreases about 2 dBc/Hz when MWCNT $\beta=1$ is used than MWCNT $\beta=1/3$.

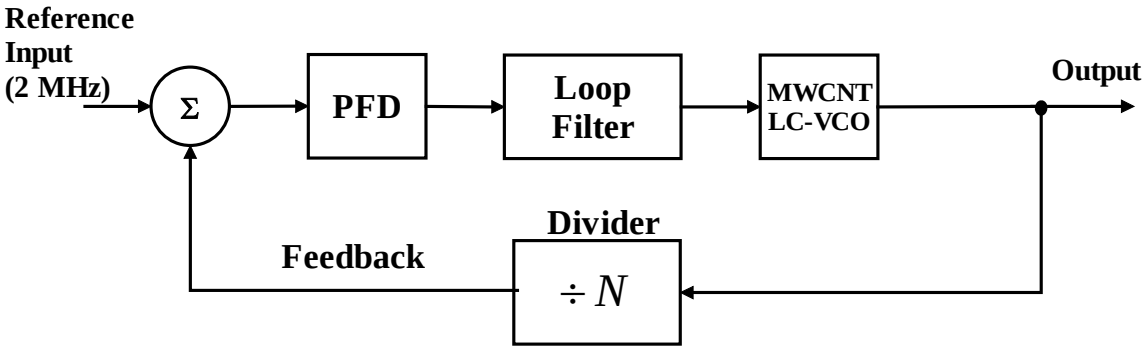

Figure 5.8: Block diagram of a PLL block diagram with MWCNT LC VCO.

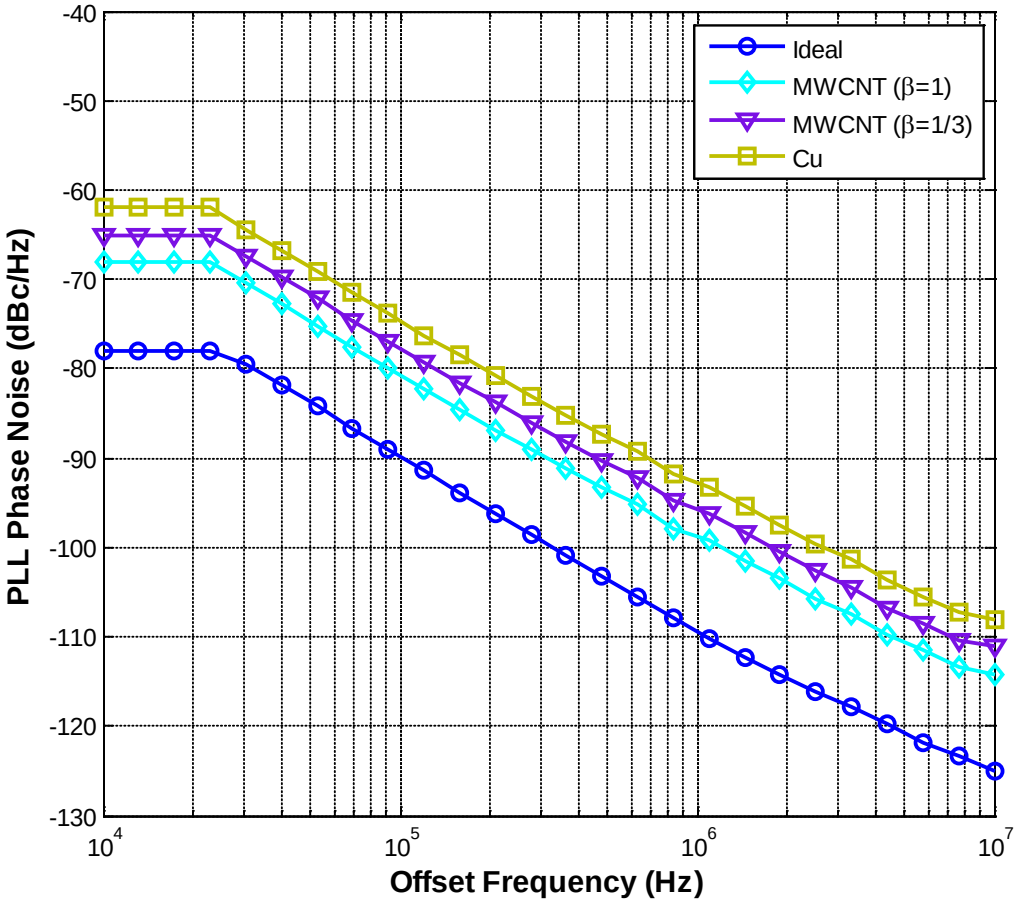

Figure 5.9. PLL output phase noise versus offset frequency.

CHAPTER 6

SUMMARY AND SCOPE FOR FUTURE WORK

In this work, different types of PLLs have been studied with phase noise and jitter issues. A summary is given as below.

6.1. Superposition Method and Experimental Study of Phase Noise in PLL

In this work, a second-order order PLL circuit is designed in 0.5 μm n-well CMOS and an attempt has been made to model phase noise based on superposition of phase noises from its following circuit building blocks: the input reference, VCO, frequency divider, PFD and the loop filter. Experimentally measured phase noise of the PLL chip follows the modeled behavior and is in good agreement. The closed loop phase noise of PLL can be obtained by the superposition method under its linear operating range. The experimental and calculated results for a second-order PLL can be extended to a higher order PLL.

6.2. Phase Noise in VCO and PLL and Hot Carrier Effects

Two fully integrated PLL frequency synthesizers are presented and the designs for phase/frequency and jitter/phase noise performances are compared. Device degradation models for the two kinds of VCOs are investigated based on hot carrier effects. The accumulated jitter can be predicted by the proportionality parameter, κ. The measured phase noise of the PLL with single-ended VCO is in the range -61 to -126 dBc/Hz under PLL oscillation frequency (200M-700MHz). The phase noise of the PLL with differential VCO is in the range -68 to -122 dBc/Hz under PLL tuning frequency (80MHz-300MHz). The measured phase noise of the PLL with single-ended VCO after HCE is in the range -60 to -124 dBc/Hz under PLL oscillation frequency (200M-700MHz). The phase noise of

the PLL with differential VCO after HCE is in the range -66 to -120 dBc/Hz under PLL tuning frequency (80MHz-300MHz). Hot carrier studies are limited to PLL implemented in 0.5 μm CMOS.

6.3. Switchable PLL and Hot Carrier Effects

A new design is proposed to expand PLL tuning range without sacrificing its speed and jitter and phase noise performances. The two CMOS PLLs are integrated on a single chip. Cadence/Spectre has been used for post-layout simulations for jitter, phase noise and switchable frequency range. The chip is experimentally tested for jitter, phase noise and switchable frequency range with and without hot carrier effects. A model is presented to address the hot carrier effects on the VCO jitter and phase noise performance. The modeled results are in good agreement with both the simulation and experimental results. The measured jitter and phase noise ranges of the PLL are around 26 to 123 ps and around −61 to −126 dBc/Hz under the entire PLL tuning frequency, 200 MHz – 700 MHz.

6.4. Low Power Phase-Locked Loop with LC VCO and Dual-modulus Prescaler Designs, Hot Carrier and NBTI Effects

The low power design of a 3V 30mW PLL frequency synthesizer designed in 0.5 μm CMOS process is presented. The divider design is a two modulus prescaler built from CML D flip-flops. The divider has a Main Counter, a Swallow Counter and Control Logic. The on-chip inductor and n-MOSFET varactors are used in the LC VCO design. The LC VCO can work from 0.9 GHz to 1.4 GHz. The device degradation issues on both hot carrier stress and NBTI effect are studied in the LC VCO. The HCE is applicable to n-MOSFETs whereas NBTI affects p-MOSFETs.

The PLL output frequency is 1.2GHz and the carrier power is -29 dBm. The in-band phase noise is -66.67 dBc/Hz at 10kHz offset frequency and reaches -120dBc/Hz at 1MHz offset frequency without HCE and NBTI stress. The PLL output carrier power is -34 dBm and phase noise is -64.68 dBc/Hz at 10 kHz offset frequency after HCE stress; phase noise is -65.39 dBc/Hz at 10kHz offset frequency after NBTI effect.

6.5. Scope for the Future Work

The noise superposition analysis can be extended to PLL circuits using LC VCO. Linear time model is used to develop the noise analysis in this work. If nonlinear model is applied, the noise model could be more accurate. Hot carrier and NBTI effects are not the only reliability issues on sub-micron CMOS devices. Other effects may also affect the short channel devices, such as soft-breakdown (SBD) and electro-static discharge stress (ESD).

In this work, only simulation results of multiwalled carbon nanotube inductor are presented. LC VCO structure with multiwalled and bundles of sigle-walled CNT wire can be designed for integration in PLL chip to increase the Q factor of the LC VCO and decrease the phase noise of the PLL chip.

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APPENDIX A

MOSIS MOS MODEL PARAMETERS FOR STANDARD N-WELL CMOS TECHNOLOGY

The following MOS Model parameters used in simulation have been obtained from the website: www.mosis.org. Both 0.5 μm and 0.18 μm N-well CMOS process parameters are used in Cadence/Spectre simulations.

RUN: T66H VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns

```
.MODEL CMOSN NMOS (                                LEVEL   = 8
+VERSION = 3.1          TNOM = 27                  TOX = 1.42E-8
+XJ = 1.5E-7            NCH = 1.7E17               VTH0 = 0.6560917
+K1 = 0.8738536         K2 = -0.0897544            K3 = 21.9401867
+K3B = -8.2202383       W0 = 1.07093E-8            NLX = 1E-9
+DVT0W = 0              DVT1W = 0                  DVT2W = 0
+DVT0 = 2.7227001       DVT1 = 0.4670998           DVT2 = -0.1723153
+U0 = 461.6553119       UA = 1E-13                 UB = 1.885415E-18
+UC = 6.856484E-12      VSAT = 1.754942E5          A0 = 0.6562813
+AGS = 0.1342215        B0 = 2.432492E-6           B1 = 5E-6
+KETA = -4.895559E-3    A1 = 1.408389E-6           A2 = 0.3288324
+RDSW = 1.416242E3      PRWG = 0.0258829           PRWB = 9.26143E-3
+WR = 1                 WINT = 2.303158E-7         LINT = 7.539811E-8
+XL = 1E-7              XW = 0                     DWG = -9.083581E-9
+DWB = 2.445322E-8      VOFF = -0.0249483          NFACTOR = 0.8038617
+CIT = 0                CDSC = 2.4E-4              CDSCD = 0
+CDSCB = 0              ETA0 = 1.964245E-3         ETAB = -2.023215E-4
+DSUB = 0.0658933       PCLM = 2.6210459           PDIBLC1 = 0.7368181
+PDIBLC2 = 2.645412E-3  PDIBLCB = -1.346078E-4     DROUT = 0.9458376
+PSCBE1 = 6.61584E8     PSCBE2 = 2.949145E-4       PVAG = 0
+DELTA = 0.01           RSH = 81.5                 MOBMOD = 1
+PRT = 0                UTE = -1.5                 KT1 = -0.11
+KT1L = 0               KT2 = 0.022                UA1 = 4.31E-9
+UB1 = -7.61E-18        UC1 = -5.6E-11             AT = 3.3E4
+WL = 0                 WLN = 1                    WW = 0
+WWN = 1                WWL = 0                    LL = 0
+LLN = 1                LW = 0                     LWN = 1
+LWL = 0                CAPMOD = 2                 XPART = 0.5
+CGDO = 2.09E-10        CGSO = 2.09E-10            CGBO = 1E-9
+CJ = 4.284376E-4       PB = 0.9184348             MJ = 0.4389925
+CJSW = 3.091424E-10    PBSW = 0.8                 MJSW = 0.2075303
+CJSWG = 1.64E-10       PBSWG = 0.8                MJSWG = 0.2075303
```

```
+CF = 0                  PVTH0 = 0.0584953       PRDSW = 105.8848326
+PK2 = -0.0258839        WKETA = -0.0190782      LKETA = 3.015064E-3     )

.MODEL CMOSP PMOS (                              LEVEL   = 8
+VERSION = 3.1           TNOM    = 27            TOX     = 1.42E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = -0.9528605
+K1      = 0.5317022     K2      = 0.0124917     K3      = 6.3482082
+K3B     = -0.6416794    W0      = 1.284945E-8   NLX     = 2.886738E-8
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.9392328     DVT1    = 0.4759313     DVT2    = -0.1149682
+U0      = 228.5251718   UA      = 3.371715E-9   UB      = 1.163631E-21
+UC      = -5.4908E-11   VSAT    = 1.511601E5    A0      = 0.885904
+AGS     = 0.1525682     B0      = 1.020429E-6   B1      = 5E-6
+KETA    = -1.92493E-3   A1      = 3.694952E-4   A2      = 0.3198543
+RDSW    = 3E3           PRWG    = -0.0411377    PRWB    = -0.02081
+WR      = 1             WINT    = 2.951834E-7   LINT    = 1.038473E-7
+XL      = 1E-7          XW      = 0             DWG     = -2.531739E-8
+DWB     = 1.921818E-8   VOFF    = -0.0776546    NFACTOR = 0.8439721
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.5617555     ETAB    = -0.0589814
+DSUB    = 1             PCLM    = 2.0722197     PDIBLC1 = 0.0237211
+PDIBLC2 = 3.093135E-3   PDIBLCB = -0.0547993    DROUT   = 0.1579219
+PSCBE1  = 5.292003E9    PSCBE2  = 5E-10         PVAG    = 8.717958E-3
+DELTA   = 0.01          RSH     = 110.7         MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.74E-10      CGSO    = 2.74E-10      CGBO    = 1E-9
+CJ      = 7.259994E-4   PB      = 0.9644989     MJ      = 0.4989143
+CJSW    = 2.585738E-10  PBSW    = 0.99          MJSW    = 0.3873857
+CJSWG   = 6.4E-11       PBSWG   = 0.99          MJSWG   = 0.3873857
+CF      = 0             PVTH0   = 5.98016E-3    PRDSW   = 14.8598424
+PK2     = 3.73981E-3    WKETA   = 5.433522E-3   LKETA   = -2.371979E-3  )
```

RUN: T92Y VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 018 microns

```
.MODEL CMOSN NMOS (                                 LEVEL   = 8
+VERSION = 3.1          TNOM    = 27                TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 2.3549E17         VTH0    = 0.3790539
+K1      = 0.4678673    K2      = 2.094882E-3       K3      = 1E-3
+K3B     = 2.8635543    W0      = 1E-7              NLX     = 1.952698E-7
+DVT0W   = 0            DVT1W   = 0                 DVT2W   = 0
+DVT0    = 0.4891847    DVT1    = 0.5915719         DVT2    = -0.5
+U0      = 305.4959128  UA      = -1.245181E-9      UB      = 2.524523E-18
+UC      = 4.296097E-11 VSAT    = 1.326081E5        A0      = 1.6595933
+AGS     = 0.3280687    B0      = -1.620759E-8      B1      = -1E-7
+KETA    = -1.129018E-3 A1      = 1.358712E-4       A2      = 0.5058927
+RDSW    = 200          PRWG    = 0.3631279         PRWB    = -0.0636973
+WR      = 1            WINT    = 0                 LINT    = 0
+XL      = 0            XW      = -4E-8             DWG     = -2.075568E-8
+DWB     = 2.088413E-9  VOFF    = -0.0992525        NFACTOR = 1.3986948
+CIT     = 0            CDSC    = 2.4E-4            CDSCD   = 0
+CDSCB   = 0            ETA0    = 6.307375E-3       ETAB    = 2.812558E-4
+DSUB    = 0.0453069    PCLM    = 1.585851          PDIBLC1 = 0.9927926
+PDIBLC2 = 2.413581E-3  PDIBLCB = -0.0251233        DROUT   = 0.9993683
+PSCBE1  = 8E10         PSCBE2  = 5.882417E-10      PVAG    = 1.009375E-7
+DELTA   = 0.01         RSH     = 3.9               MOBMOD  = 1
+PRT     = 0            UTE     = -1.5              KT1     = -0.11
+KT1L    = 0            KT2     = 0.022             UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11          AT      = 3.3E4
+WL      = 0            WLN     = 1                 WW      = 0
+WWN     = 1            WWL     = 0                 LL      = 0
+LLN     = 1            LW      = 0                 LWN     = 1
+LWL     = 0            CAPMOD  = 2                 XPART   = 0.5
+CGDO    = 4.16E-10     CGSO    = 4.16E-10          CGBO    = 7E-10
+CJ      = 1.740557E-3  PB      = 0.99              MJ      = 0.4621235
+CJSW    = 4.180326E-10 PBSW    = 0.8994981         MJSW    = 0.2677227
+CJSWG   = 3.29E-10     PBSWG   = 0.8994981         MJSWG   = 0.2677227
+CF      = 0            PVTH0   = -8.458495E-3      PRDSW   = -10
+PK2     = 4.057598E-3  WKETA   = 5.254243E-5       LKETA   = -8.084685E-3  )

.MODEL CMOSP PMOS (                                 LEVEL   = 8
+VERSION = 3.1          TNOM    = 27                TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 4.1589E17         VTH0    = -0.5224091
+K1      = 0.615586     K2      = 1.740055E-3       K3      = 0
+K3B     = 10.126439    W0      = 1E-6              NLX     = 7.427938E-9
+DVT0W   = 0            DVT1W   = 0                 DVT2W   = 0
+DVT0    = 2.6099192    DVT1    = 0.7749922         DVT2    = -0.1505238
+U0      = 100          UA      = 9.628749E-10      UB      = 1E-21
```

```
+UC      = -1E-10          VSAT    = 1.832587E5      A0      = 1.0636713
+AGS     = 0.1473504       B0      = 4.332305E-7     B1      = 2.456784E-6
+KETA    = 8.213399E-3     A1      = 0.0251405       A2      = 0.3
+RDSW    = 1.048851E3      PRWG    = 0.206411        PRWB    = -0.1916693
+WR      = 1               WINT    = 0               LINT    = 2.731764E-8
+XL      = 0               XW      = -4E-8           DWG     = -4.035405E-8
+DWB     = 6.772034E-11    VOFF    = -0.118657       NFACTOR = 1.0750885
+CIT     = 0               CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0               ETA0    = 0.2473215       ETAB    = -0.0574668
+DSUB    = 1.0277572       PCLM    = 1.2659136       PDIBLC1 = 7.65712E-3
+PDIBLC2 = -1E-5           PDIBLCB = -1E-3           DROUT   = 0.1043079
+PSCBE1  = 6.942941E10     PSCBE2  = 5E-10           PVAG    = 2.330338E-3
+DELTA   = 0.01            RSH     = 3               MOBMOD  = 1
+PRT     = 0               UTE     = -1.5            KT1     = -0.11
+KT1L    = 0               KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18       UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0               WLN     = 1               WW      = 0
+WWN     = 1               WWL     = 0               LL      = 0
+LLN     = 1               LW      = 0               LWN     = 1
+LWL     = 0               CAPMOD  = 2               XPART   = 0.5
+CGDO    = 4.99E-10        CGSO    = 4.99E-10        CGBO    = 7E-10
+CJ      = 1.840957E-3     PB      = 0.9809513       MJ      = 0.4692719
+CJSW    = 3.603168E-10    PBSW    = 0.99            MJSW    = 0.3266334
+CJSWG   = 2.5E-10         PBSWG   = 0.99            MJSWG   = 0.3266334
+CF      = 0               PVTH0   = 5.46428E-3      PRDSW   = 1.8819543
+PK2     = 3.138577E-3     WKETA   = 0.0321052       LKETA   = -6.626532E-3    )
```

APPENDIX B

LIST OF AUTHOR'S PUBLICATIONS

[1] Y. Liu, A. Srivastava and Y. Xu, "Switchable PLL frequency synthesizer and hot carrier effects," Journal of Circuits and Systems, Vol. 2, No. 1, pp .45-52, Jan. 2011.

[2] Y. Liu, A. Srivastava and Y. Xu, "A switchable PLL frequency synthesizer and hot carrier effects," *Proc. ACM Great Lakes Symposium on VLSI*, pp. 481-486, May 10-12, 2009, (Boston, MA).

[3] Y. Liu and A. Srivastava, "Reliability considerations in switchable PLL frequency synthesizers for wireless sensor networks," *Proc. SPIE Nano-, Bio-, Info-Tech Sensors and Systems*, vol. 7646, pp. 7646-28, March 7-9, 2010, (San Diego, CA).

[4] Y. Liu and A. Srivastava, "Hot carrier effects on CMOS phase-locked loop frequency synthesizers," *Proc. International Symposium on Quality Electronic Design (ISQED)*, pp. 92-98, March 22-24, 2010, (San Jose, CA).

[5] Y. Liu and A. Srivastava, "Effect of hot carrier injection and negative bias temperature instability on the performance of CMOS phase-locked loops," *Proc. 2010 ASEE-GSW Annual conference*, Mar. 24-26, 2010, (Lake Charles, LA).

[6] A. Srivastava, Y. Xu, Y. Liu, A. K. Sharma, and C. Mayberry, "CMOS LC voltage-controlled oscillator design using carbon nanotube wire inductor," *Proc. 5th IASTED International Symposium on Circuits and Systems*, pp. 171-176, August 23 – 25, 2010, (Maui, Hawaii).

[7] A. Srivastava, Y. Xu, Y. Liu, A. K. Sharma, and C. Mayberry, "CMOS LC voltage-controlled oscillator design using multiwalled carbon nanotube wire inductor," *Proc. IEEE International Symposium on Electronic System Design (ISED)*, December 20-22, 2010, (Bhubaneswar, India).

[8] A. Srivastava, Y. Xu, Y. Liu, A.K. Sharma, and C. Mayberry, ''CMOS LC voltage controlled oscillator design using carbon nanotube wire inductors," ACM Journal on Emerging Technologies in Computing Systems, accept (2011).

APPENDIX C

PERMISSION TO USE COPYRIGHTED MATERIALS

From: Circuits & Systems cs@scirp.org
To: Yang Liu <yliu11@tigers.lsu.edu>
Date: Thu, Oct 27, 2011 at 8:56 PM
Subject: Re: Permission Request
Mailed-by: scirp.org

Dear Dr Yang Liu,

That's OK. Please just indicate the source of your cited figures.

Please feel free to contact me with any problem.

Best Regards,

Tian Huang
CS Editorial Board

Scientific Research Publishing, USA

http://www.scirp.org

Email:cs@scirp.org

-----Original Message-----
From: Yang Liu <yliu11@tigers.lsu.edu>
To: "Circuits & Systems" <cs@scirp.org>
Date: Thu, 27 Oct 2011 14:19:16 -0500
Subject: Permission Request

Dear Editor,

My name is Yang Liu. I am completing a doctoral dissertation at Louisiana State University titled "Phase noise in CMOS phase-locked loop circuits." I would like to request your permission to include Figure 1 to Figure 21 and some content from one of my published works in my dissertation document. The title, volume number and publication date of this publication is as included below:

Y. Liu, A. Srivastava and Y. Xu, “Switchable PLL frequency synthesizer and hot carrier effects,” Journal of Circuits and Systems, Vol. 2, No. 1, pp.45-52, Jan. 2011.

Your immediate response for this request will be highly appreciated as I am in the process of compiling the final document.

Thanks and regards,

Yang Liu

VITA

Yang Liu was born in 1983, in Beijing, China. He received his Bachelor of Science degree in Automation from Beijing Institute of Technology, Beijing, China, in July 2005. He has been enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, since August 2006 to pursue his doctoral studies. During this period, he received his Master of Science degree in Electrical Engineering in Louisiana State University, in May, 2010. His research interests include design and noise analysis of phase-locked loop (PLL) circuits.