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Fabrication of micro bumps for micro scale thermal management

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FABRICATION OF MICRO BUMPS FOR MICRO SCALE THERMAL MANAGEMENT

A Thesis

Submitted to the Graduate Faculty of the Louisiana State University and Agricultural and Mechanical College in partial fulfillment of the requirements for the degree of Master of Science in Mechanical Engineering in

The Department of Mechanical Engineering

by

Ajay A. Kardak
B.E., Visveswaraiah Technological University, India, May 2003
December, 2008
To my parents:

Mr. Ashok Kardak

and

Mrs. Geeta Kardak

For their endless love and support.
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Abstract

Cryopreservation is storage of biological systems at ultra low temperatures for a prolonged duration; such that they can be thawed and restored to the same living state. It is important to understand the behavior of cells when they are subjected to subzero temperatures. Research in this area has shown the occurrence of two main biophysical events; cellular dehydration and intracellular ice formation. Current techniques for characterizing the dehydration in cells as part of a tissue are not adequate for studying intracellular ice formation in tissues. An integrated device consisting of an array of thermal sensors (microthermocouples) and actuators (microthermoelectric coolers) would help to detect intracellular ice formation by measuring and modulating the heat release of individual cells during freezing. This requires a dense wiring layer below the devices which can act as a heat sink in turn affecting the performance of the device. To alleviate this problem fabrication of bump structures was proposed to isolate the dense wiring layer from the array.

Modeling was used to assess the effect of the bumps on the performance of the thermoelectric cooler. Bismuth telluride posts of 10 µm diameter and 20 µm height yielded optimal cooling with a bump radius of 5 µm. A maximum effective change in temperature of 3.47 K was achieved for an applied current of 23.7 mA and Joule’s breakdown was found to occur at 47.7 mA.

To avoid the complexities in the measurements due to the presence of second junction, copper and constantan were chosen as bump material. Electrodeposition along with UV-LIGA microfabrication technique was used to fabricate the bumps. Copper and constantan micro bumps, with mean diameters of 6.5 & 27.76 µm and
heights of 7.81 and 12.04 µm were fabricated with dimensional variation of ±0.5 µm with a 95% confidence interval.

A custom printed circuit board was fabricated on FR4 laminate using lithography and liftoff technique. The mean length and width of the structures were found to be 4151.98 ±1.86 µm and 1003.21 ±0.55 µm, respectively with 95% confidence interval. There is a need for future work to precisely fabricate metal features on FR4 laminate.
1. INTRODUCTION

1.1. Cryopreservation

Cryopreservation refers to storage of cells, tissues and ultimately organs at ultra low temperatures for a prolonged period of time such that they can be thawed and restored to the same living state as they were before storage. Cryopreservation techniques are developed for the preservation of various biological systems such as microorganisms, isolated tissue cells, smaller multicellular organisms and even complex systems such as embryos [1-3] and have become indispensable in the development of modern clinical practices.

Cell water is the essential component of a cell. It is important to understand what happens to this cell water as the cells are subjected to subzero temperatures. Figure 1.1 shows a schematic of a typical cell freezing process. As the cell undergoes freezing, ice is formed in the extracellular space, which causes a chemical imbalance across the cell membrane [4]. During freezing in the presence of extracellular ice biological systems experience either cellular dehydration (water transport) at 'slow' cooling rates or intracellular ice formation (IIF) at 'rapid' cooling rates [2, 5] as shown in Figure 1.1. Both the above mentioned biophysical processes have been shown to be detrimental to the post-thaw viability of the cells [6]. More recently, Pazhayannur and Bischof [7] and Devireddy and Bischof [8] developed two complementary and independent techniques to measure the dynamic water transport response of cells in tissues during freezing. Techniques used to study the water transport and intracellular ice formation are described in the subsequent sections.
1.2. Biophysical Response Detection Technique

1.2.1. Differential Scanning Calorimeter (DSC)

Differential scanning calorimeter (DSC) (Figure 1.2) is an instrument that measures the heat release during a phase change process as a function of time and temperature [9]. The DSC technique has been effectively used to obtain dynamic and quantitative water transport data in cell suspensions during freezing. The method is based on the fact that heat release of a prenucleated sample containing osmotically active cells in media is always greater than the final heat release of an identical sample of osmotically inactive cells in the same media. In DSC as temperature changes at a predefined rate, the heat release and change in enthalpy during a phase change process can be measured by calculating the area under peaks of a heat flow thermogram generated by DSC.
1.2.1.1. Disadvantages of Differential Scanning Calorimeter (DSC)

Although DSC is a vital technique it has some disadvantages:

- DSC is inapplicable to the investigation of Intracellular Ice formation (IIF) in cells;
- DSC cannot be used to study the biophysical response of cells that are subjected to higher cooling rates than 50 °C/min;
- DSC requires a priori knowledge of the initial cell volume, surface area and inactive cell volume;
- The DSC technique cannot detect the presence of dead cells in the initial sample.

As mentioned above IIF cannot be detected using this method because of the lack of any visual aid in the apparatus. Hence DSC as a standalone device cannot completely detect all the biophysical response of the cells when subjected to either heating or cooling protocol.
1.2.2. Cryomicroscopy

Water transport and IIF during freezing have been studied extensively in single spherical cells using cryomicroscopy. Cryomicroscopy is the application of cryogenic temperatures to cellular systems mounted under a light microscope to study the biophysical response of cells to freezing. Molisch first reported the study of living organisms, amoebae, under freezing conditions by placing the whole microscope in a cooled chamber (Molisch 1897). This technique has been refined and modified over the years to allow the study of the dynamic response of a variety of plant and mammalian cells under various freezing conditions [1, 2, 10]. The cryomicroscope as shown in Figure 1.3 (A) has a cryostage fit to a microscope capable of capturing live video and photograph. To obtain water transport and IIF data the sample is mounted on the cryostage and cooled. A predetermined cooling rate can be applied to the cryostage using the controller. Analysis of cellular volumetric response in the presence of extracellular ice can be performed by determining the projected area of each cell at different temperatures during freezing.

Figure 1.3 (A) Overview of Cryomicroscope. (B) Closeup of Cryostage
1.2.2.1. Disadvantages of Cryomicroscopy

Cryomicroscopy can be used to study the two main biophysical events, water transport and IIF for individual cells, but it has some disadvantages that are listed below.

- Cryomicroscopy cannot be used to study the freezing of opaque tissue sections.
- It does not allow the measurement of the volumetric response of a large number of cells.
- In cryomicroscopy two-dimensional area of a cell is extrapolated to three-dimensional volume. This assumption fails while studying irregular or nonspherical cells.

1.3. Motivation

1.3.1. Thermoelectric Cooler (TEC)

One way of acquiring better knowledge of water transport and intracellular ice formation would be to modulate temperature at cellular level. Individually addressable micro thermoelectric coolers can be used to modulate temperatures at the cellular level. Thermoelectric coolers are based on the Peltier effect and use semiconductor materials which are optimized for Seebeck effect. Two different elements, a p-type and an n-type, are employed as a couple to form a simple TEC (Figure 1.4). As shown in Figure 1.4 the bottom ends of p-type and n-type pellets are connected to the positive and negative ends of the voltage source, respectively. The majority charge carriers (holes) in the p-type material are repelled by the positive potential and are attracted by the negative pole; likewise the majority charge carriers (electrons) in the n-type material are repelled by the negative potential and are attracted towards the positive pole of the voltage
supply. In the bottom and top copper interconnects electrons are the charge carriers. When these reach the p-type material, they simply flow through the holes within the crystalline structure. Electrons flow continuously from the negative pole of the voltage supply through the n-type pellet, through the copper interconnect junction, through the p-type pellet and finally to the positive pole of the supply. When a p-n junction is forward biased as shown in Figure 1.4 the majority charge carriers and heat flow in the same direction, which causes heat to be absorbed at the bottom and released at the top. As a first step towards achieving localized control of temperature in cells and tissues, an array of individually addressable micro thermoelectric coolers were modeled and fabricated [11].

![Figure 1.4 Schematic of a typical TEC where n and p type thermoelectric pellets are arranged electrically in series and thermally in parallel.](image)

1.3.2. Thermocouple

A thermocouple in its simplest form would consist of two different metals in a closed circuit and a potential measuring device in series. The operation principle of a thermocouple is described by the Seebeck effect: When two dissimilar materials are
joined together at two junctions and these junctions are maintained at different temperatures, an electromotive force (EMF) exists across the two junctions [12]. As shown in Figure 1.5, A and B are two different metals in contact, forming two separate junctions and an EMF measuring device is in series with metal B. The two junctions are maintained independently at different temperatures. Whenever there is a temperature difference between the junctions, an EMF is produced and measured as \( E_{A,B} \).

![Figure 1.5 Schematic of a thermocouple circuit.](image)

Although two independent and complementary techniques are available to measure the dynamic behavior of cells during freezing, there is no instrument or experimental technique that can measure localized temperature in a tissue matrix during freezing. Models by Kandra and Devireddy [13] suggested that ice formation events in tissue cells can be monitored by tracking the highly localized temperature increase due to the phase change of water to ice or due to the latent heat released when intracellular water turns to ice. During rapid cooling, the temperature drops and the cells either freeze or undergo ice nucleation, as the cooling rate is applied. Freezing of the cells releases latent heat and the consequent transient temperature increase can be measured by a thermocouple array with inter-junction spacing on the order of the cell
size. The formation of ice within cells in a tissue section could be tracked by measuring the temperature increase from individual cell phase change. As a proof of concept for this application, prototype arrays of Type T thermocouples were designed and fabricated [14]. Type T thermocouples were chosen because they offer excellent sensitivity below 0 °C [15], have a stable Seebeck coefficient at low temperatures. Moreover, copper and constantan (copper-nickel) can be more easily electroplated than many other standard alloys used for thermocouples.

1.3.3. Integrated Array of Thermal Sensor and Actuator

An integrated array of thermal sensors and actuators consisting of microthermocouples and microthermoelectric coolers can be used to preserve tissue sections. The microthermocouples and microthermoelectric coolers were specifically designed for use with biological systems [11, 14]. An integrated array is desired to control and modulate temperature at the micro meter (cellular) level. The organization of the proposed device is as shown in Figure 1.6. A set of microthermocouples and microthermoelectric coolers is treated as one unit and the integrated array would consist of 9 (3 x 3) such units.

Figure 1.6 Schematic of an integrated array
1.4. Problem Statement and Approach

The array would have 18 individual devices which would have 36 leads (2 wires per device). As the dimensions of the planar wiring layer at the bottom of the device are comparable to the device and cell dimensions, it acts as a heat sink, so the thermocouples would not record the precise temperature of the biological system. To alleviate this problem the dense wiring layer has to be isolated from the array. This can be achieved by using bump structures. Figure 1.7 shows a schematic of a flip-chip bonded device on a printed circuit board (PCB) with the aid of electrically conductive bumps and adhesive resin. As the bumps ideally would have point contact with the metal bond pads on the PCB, heat loss to the wiring is reduced.

A second generation of the device will have an array of 100 (10 x 10) units of the integrated device to measure and modulate temperature around individual cell. This will provide vital information about the cellular response to local temperature input and this would help to control freezing of individual cells in a tissue sample.

Figure 1.7 Schematic of the packaged device
2. BACKGROUND

2.1. Flip Chip Assembly

2.1.1. Introduction

Flip chip (FC) assembly is the direct electrical connection of face down electronic components onto substrates or circuit boards by means of conductive bumps on the bond pads. Flip chip components are predominantly semiconductor devices; however, components such as filters, sensor arrays, microelectronics and MEMS devices are being used in flip chip form. Flip chip is also called Direct Chip Attach (DCA). It is a more appropriate term as the chip is directly attached to the substrate or circuit board. It is the method of interconnection that distinguishes this method from all others. Flip chip uses direct contact without any additional wires. All other methods like tape automated bonding (TAB), although has the chip face down, wires are used to interconnect the device and circuit board. The idea of direct connection to a substrate or circuit board has many significant benefits while also creating challenges for both assembly and the substrate.

Figure 2.1 describes a typical flip chip assembly. First, the metal pads are formed on the device die or wafer (Figure 2.1 (A)). Bumps are formed on each of these metal pads (Figure 2.1 (B)). As shown in Figure 2.1 (C) the whole device die with bumps is flipped and positioned over the external circuit board such that each bump would face the corresponding metal pad on the circuit. Bumps are mounted on the circuit (Figure 2.1 (D)). In most cases, the bumps are made of solder which is remelted to attach the
bump to the circuit. The remaining space under the device die is filled with an electrically insulating adhesive resin.

Figure 2.1 Overview of the flip chip bonding process (A) Pads are metalized on the surface of the device die. (B) Bumps are fabricated on each pad. (C) Device die is flipped and positioned such that the bumps face the corresponding connectors on the external circuit. (D) Bumps are attached to the circuit. (E) Mounted device is underfilled using electrically insulating adhesive resin.
Flip chip assembly has been widely accepted within microelectronics and MEMS as a technology for maximum miniaturization [16]. Typical applications are cellular devices, GPS navigational systems, and satellite technology. Virtually all computer CPUs around the world use flip chips owing to their great input/output (I/O) flexibility, high performance and small size. Computer components and peripherals, including disk drives, displays, and printers, have adopted flip chip assembly. Braun et al. (2005) have shown that flip chip assembly has potential for high temperature (150 °C) applications in the automotive industry. Flip chip, because of its small size, ruggedness and plethora of other advantages, has found applications in consumer products, communications, smart cards/RFIDs and aerospace industry.

2.1.2. Advantages of Flip Chip Assembly

Flip chip assembly offers a wide range of benefits as listed below:

- **Small size**: As bond wires are eliminated in flip chip the required board area is reduced which in turn reduces the weight of the packaged device.
- **High performance**: As it has direct contact, delaying inductance and capacitance is reduced there by increasing the performance of the whole device.
- **Good I/O flexibility**: Flip chip offers great input/output connection flexibility. As bond wires are eliminated, flip chip connections can use the whole area of the die, accommodating dense connections on a smaller die when compared to any other chip scale packages (CSP’s).
- **Rugged connections**: Flip chip assembled devices have mechanically rugged interconnections. After the final step of underfill, flip chip devices are like solid
blocks of cured epoxy, which can survive rocket liftoff, artillery fire and millions of hours of use in computers and automobiles.

- Low cost: Flip chip offers the lowest cost of interconnection for high volume of production.

### 2.1.3. Current Trends in Flip Chip Technology

With the trends of IC industry to achieve higher performance, reliability and I/O count on ASICs, among the available bonding and assembly techniques, flip chip is the most actively used assembly technique. Flip chip technology has been in use in the electronics industry for over forty years. Supercomputers, workstations, and mainframes have continued to use flip chip for high I/O count and higher performance. Flip chip has found increased applications in portable products that take advantage of the small footprint of flip chip and its light weight and thinness. Products such as PC cards, notebooks, digital cameras and camcorders, PDAs are expected to see increases in flip chip usage over the next few years.

Flip chip was developed for both interconnects in a package and for direct mounting of devices on a substrate [17]. Many Japanese companies such as Hitachi, Fujitsu, Matsushita, NEC, and Oki Electric have already designed products with flip chip-mounted die in a package. As industry infrastructure is not fully developed for direct on-board mounting, the majority of the growth has been in developing flip chip assembly in packages such as ball grid array (BGA) and chip scale packages. Over 90% of the volumes of flip chip applications are low lead count, for watches, vehicle modules, displays and communication modules.
2.2. **Bumps**

2.2.1. **Definition**

Bumps are structures that serve as an electrically conductive spacer between a device die and a substrate or circuit board. Bumps serve several functions in flip chip assembly. In addition to being electrically conductive spacer, bumps also act as a mechanical mounting of the device die to the substrate, provide rigidity, and prevents electrical contact between the die and substrate conductors. Bumps also act as a short lead to relieve mechanical strain between board and substrate.

2.2.2. **Classification** [18]

2.2.2.1. **Fusible Bumps**

Fusible bumps are the most commonly used bump type because the bump material can aid in joining the device die and the substrate. Many fusible types, especially those of lower-melting temperature alloys, provide the joining material for assembly. A few of these are:

- **High-Lead Solder**: High-melting tin-lead (Sn/Pb) solder such as 3/97 is used for this type of bump. This fusible alloy has a reflow temperature of 350 °C and is generally used on ceramic substrates. Flip chip BGAs using high-lead bumps allow the package to be soldered to a board with eutectic solder without disturbing the FC-to-chip-carrier joints. The ceramic substrates, though costlier than organic substrates, offer higher thermal conductivity, better planar surface, low moisture absorption and also act as excellent dielectrics.
• **Stratified Bumps:** These are also built with high-lead content material with the top of the bump being rich in tin. These provide high standoff and favorable fatigue resistance of high-lead bumps while creating stable eutectic solder for joining purposes.

• **Eutectic Sn/Pb:** Eutectic solder is the de facto standard of electronic assembly. Since eutectic temperatures are the natural equilibrium point of an alloy, it is the ideal region for processing. Eutectic solder can be used as the source of joining material for assembly on organic substrates. Eutectic tin-lead solder is readily available in a variety of forms like fine-particle paste. One of the main disadvantages of eutectic solder joints is the eventual fracture when subjected to continual stress.

• **Polymer Bumps, Thermoplastic:** Polymers can either be used as fusible or nonfusible material. Thermoplastics behave like solder. Thermoplastics are polymerized solids, but can be made into conductive pastes by dissolving them in polar solvents and adding conductive particles like silver. Once applied, the solvent can be evaporated to form a dry bump. The bump can be attached to the substrate by heating to softening or melting point.

**2.2.2.2. Nonfusible Bumps**

Nonfusible bumps are only a part of interconnect between the device die and substrate. A joining material is needed to complete the connection. Metals like copper and nickel are used to fabricate nonfusible bumps. Nonfusible bumps help in maintaining minimum height between the die and the substrate, which is a significant feature, as too low standoff may increase the strain in the joint. Materials and their characteristics used to make nonfusible bumps are listed below.
• **Gold**: Gold is a soft and malleable metal, allowing bumps to be shaped easily. Gold was used to bump chips even before the inception of flip chip technology. Tape automated bonding (TAB) process used gold to aluminum connection metallurgy. Pure gold is typically used for bumping chips and can be directly applied on the aluminum pads. Gold bumps are highly compatible with all conductive adhesives.

• **Nickel**: Nickel being very strong, hard and high-melting metal, it has been used extensively in microelectronic assembly. Nickel can be used for both purposes of under bump metallurgy (UBM) and bump itself. In many cases electroplating of nickel is continued until the UBM builds up to a bump. Usually nickel bump is overplated with nobel metals like gold to prevent oxidation.

• **Polymer, Thermoset**: Thermosets are a class of polymers which do not melt once they are set or polymerized. Bumps are usually made with thermoset isotropic conductive adhesive (ICA) material, which are either stenciled or screen printed on the UBM [19]. Once cured, the bumps require an adhesive resin for assembly. Thermoset materials have same thermal conductivity as that of solder and possess reasonable mechanical strength.

### 2.2.3. Bump Fabrication Techniques

Various techniques are employed in bump fabrication, predominant of those being vacuum deposition, electroplating, mechanical or wire bumping technique, and printing or stenciling. Many sub-classifications of these methods are described in the subsequent sections.
2.2.3.1. Vacuum Deposition [18]

In vacuum deposition bumps are always formed on their respective UBM. Many metals and some times even alloys can be deposited using this technique. One commonly deposited alloy is solder (tin-lead). Different compositions of the same alloy can be deposited by varying the deposition time. A mask is used to define the deposition areas which correspond to the metal pads on the substrate. Once the deposition is done the mask can be removed and cleaned as desired. Hicks [20] showed deposition of three layers: 600 Å of chromium being the first, 20000 Å phased chromium and tin followed by 80000 Å of tin by vacuum deposition. This implies stratified bumps of high-lead capped with tin can be produced by this technique.

2.2.3.2. Electroplating

Electroplating is a most common industrial process to deposit metals and a wide range of alloys. Electrodeposition is a process where soluble metal salts are converted back to metal on the surface that needs to be coated. It involves the reduction of metal ions from an aqueous salt solution. The aqueous salt solution is also called electrolyte, commonly referred to as the plating bath. The sample (working electrode) that needs to be coated is immersed into the electrolyte, or bath, and is negatively charged (cathode). A positively charged anode typically a (platinum mesh) completes the circuit. A power source is required to supply the necessary current. The current, in the bath, is carried by the positively charged ions from the anode towards the negatively charged cathode. This movement causes the ions in the bath to migrate toward the electrons present on or near the cathode. Metal ions are removed from the electrolyte by reduction and are deposited on the surface of the sample to be plated as desired. As the deposition
proceeds, metal ions get depleted from the bath. Typically, an electrode of the same metal is used for the positive anode to compensate for the depletion of ions. Electroplating can be done in two ways: Electrolytic, where current is passed through the plating bath, which controls the reaction and acts as a driving force; or Electroless, where a chemical reaction supplies the required energy. Many metals like copper, nickel, constantan (alloy of copper-nickel), bismuth-telluride, gold and solder can be electrodeposited [11, 14, 21-23].

2.2.3.3. Printing/Stenciling

Stencil printing is a low cost approach to forming bumps for flip chip applications. Figure 2.2 describes the wafer bumping process by stencil printing. The first step is to electroless deposit Ni-Au UBM on Al pads. The second step is to deposit solder paste by stencil printing as shown in Figure 2.2. Next is to reflow the solder paste to form solder bumps on the wafer. The final step is to clean the wafer with DI water [24]. Solder bumps have been fabricated via stencil printing method on 4, 5, 6 and 8 inch wafers 200 µm pitch with the bump height standard deviation less than 3% [24]. Kay et al. [12] demonstrated consistent printing of ICA bumps with a 90 µm pitch and uniform height of 50 µm. Reflowed solder bumps on a 6 inch wafer with 150 µm pitch and 65 µm height have been fabricated by using the stencil printing method [25].

2.2.3.4. Mechanical (Wire Bumping)

Mechanical bumping is a chemical free technique. Generally gold bumps are formed using a wire bonding machine [26]. This method has certain advantages. No UBM is required, the process is completely mechanical, and no chemicals are involved,
practical for single die. Typically bumps formed by this method use modified wire bonding processes, where the wire is snapped off after the ball is initially connected to the device die forming a conical shape at the top [27]. A process called coining is followed to flatten the tail and to create a flat round top on the bump.

![Figure 2.2 Wafer bumping process by stencil printing [24]](image)

2.2.4. Literature Review

Wafer bumping is the heart of flip chip technology. A wide variety of bumps, with different metals and alloys have been fabricated. Table 2.1 gives a brief overview of bumps that have been fabricated employing different techniques and materials with their key feature dimensions.
Table 2.1 Literature review of bumps fabricated employing different techniques and material

<table>
<thead>
<tr>
<th>Reference</th>
<th>Material and fabrication process</th>
<th>Feature size (µm)</th>
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</thead>
<tbody>
<tr>
<td>[28]</td>
<td>Electroplated Nickel with gold top</td>
<td>Diameter</td>
</tr>
<tr>
<td></td>
<td>Electroplated Solder on copper UBM</td>
<td>400</td>
</tr>
<tr>
<td>[23]</td>
<td>Solder free bumps were electroplated using pure-tin (Sn), tin-bismuth (80wt%Sn:20wt%Bi), tin-copper (99.3wt%Sn:0.7wt%Cu), tin-silver (96.5wt%Sn:3.5wt%Ag), tin-silver-copper (93.8wt%Sn:3.5wt%Ag:0.7wt%Cu)</td>
<td>200</td>
</tr>
<tr>
<td>[21]</td>
<td>Stencil printing of solder bumps on copper stud</td>
<td>150</td>
</tr>
<tr>
<td>[19]</td>
<td>Stencil printing of cylindrical conductive polymer (H20E-PFC-LC, JM7000.imp) bumps</td>
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</tr>
<tr>
<td>[29]</td>
<td>Electroplated solder bumps on nickel stud</td>
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<td>[30]</td>
<td>Electroplated copper column based solder bumps</td>
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<td></td>
<td>70, 65</td>
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<td>[31]</td>
<td>Electroless plating of nickel on Al pads</td>
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<td>[32]</td>
<td>Electroplated tin capped copper column bumps</td>
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<td>[33]</td>
<td>Electroplated cylindrical indium solder bumps</td>
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<td>Electroplated copper column bumps</td>
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<td>[35]</td>
<td>Silver paste bumps with Ni/Au cap on Al pads</td>
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<td>[36]</td>
<td>Electroplated Cu and Sn/Ag double bump</td>
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</tr>
<tr>
<td>[37]</td>
<td>Sea-of-leads (SoL) complaint solder bumps were electroplated</td>
<td>55</td>
</tr>
<tr>
<td>[38]</td>
<td>Reflowed solder bumps (Square) on Ni pedestal</td>
<td>50x50</td>
</tr>
</tbody>
</table>
From Table 2.1 it can be observed that, bumps of different size and shape, diameter ranging from 40 µm to 400 µm have been reported. The most common fabrication technique employed was electrodeposition, as this technique is a low cost method for fabricating high quality metal and alloys. As the functions of the micro devices have been remarkably enhanced, the number of pads needed for interconnection on a device die has been increased. It was necessary to fabricate bumps of smaller dimensions (<40 µm) and finer pitch. An effort has been made to fabricate micro bumps with finer pitch to allow for modular design of integrated sensors and actuators.
3. Thermal System Modeling

3.1. Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z(T)$</td>
<td>Dimensionless figure of merit</td>
<td></td>
</tr>
<tr>
<td>$\alpha(T)$</td>
<td>Temperature dependent Seebeck coefficient</td>
<td>$VK^{-1}$</td>
</tr>
<tr>
<td>$K(T)$</td>
<td>Temperature dependent thermal conductivity</td>
<td>$W , \mu m^{-1} K^{-1}$</td>
</tr>
<tr>
<td>$\sigma(T)$</td>
<td>Temperature dependent electrical conductivity</td>
<td>$\Omega^{-1} \mu m^{-1}$</td>
</tr>
<tr>
<td>$T$</td>
<td>Absolute temperature of the system</td>
<td>$K$</td>
</tr>
<tr>
<td>$Q$</td>
<td>Heat flow rate at the cold junction</td>
<td>$W$</td>
</tr>
<tr>
<td>$T_c$</td>
<td>Cold junction temperature</td>
<td>$K$</td>
</tr>
<tr>
<td>$T_h$</td>
<td>Hot junction temperature</td>
<td>$K$</td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>Ambient temperature</td>
<td>$K$</td>
</tr>
<tr>
<td>$I$</td>
<td>Current through the thermo-elements</td>
<td>$A$</td>
</tr>
<tr>
<td>$R$</td>
<td>Electrical resistance of the thermo-elements</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$V$</td>
<td>Voltage across the thermo-elements</td>
<td>$V$</td>
</tr>
<tr>
<td>$Q_h$</td>
<td>Heat rejection of the µTEC</td>
<td>$W$</td>
</tr>
<tr>
<td>$Q_c$</td>
<td>Cooling capacity of the µTEC</td>
<td>$W$</td>
</tr>
<tr>
<td>$A$</td>
<td>Cross-sectional area of the thermo-elements</td>
<td>$\mu m^2$</td>
</tr>
<tr>
<td>$h$</td>
<td>Height of the thermo-elements</td>
<td>$\mu m$</td>
</tr>
<tr>
<td>$L$</td>
<td>Length of the thermo-elements</td>
<td>$\mu m$</td>
</tr>
<tr>
<td>$W$</td>
<td>Width of the thermo-elements</td>
<td>$\mu m$</td>
</tr>
</tbody>
</table>
3.2. Design Theory

The cooling performance of the Thermo-electric cooler (TEC) materials can be determined by a dimensionless factor called figure of merit, $Z(T)$. $Z(T)$ is defined by the following relation [39]:

$$Z(T) = \frac{\alpha(T)^2 \sigma(T)}{K(T)} T$$  \hspace{1cm} (1.1)
Where $\alpha(T)$, $\sigma(T)$ and $K(T)$ are temperature dependent material properties of the thermoelectric material. Among the various TEC materials, bismuth telluride has the best performance ($Z(T)$) [40] and is stable at room temperature. These temperature dependent properties were obtained by curve fitting the standard curves and can be represented as follows [11]:

$$\alpha(T) = -0.001T^2 + 0.937T + 29.684$$  \hspace{1cm} (1.2)

$$K(T) = 0.0004T^2 - 0.231T + 53.21$$  \hspace{1cm} (1.3)

$$\sigma(T) = \frac{1}{4.3516T - 279.9}$$  \hspace{1cm} (1.4)

In order to set the framework of the numerical methods used, some of the basic conventional thermoelectric equations are reviewed. The heat balance at the cold junction of the thermoelectric cooler is given by

$$Q = \alpha(T)IT_c - I^2 \frac{R(T)}{2} - K(T)(T_h - T_c)$$  \hspace{1cm} (1.5)

Where $\alpha(T)IT_c$ represents the Peltier cooling effect, $I^2 \frac{R(T)}{2}$ represents Joule heating due to the resistance of the thermoelectric element, $K(T)(T_h - T_c)$ represents the amount of heat flowing from the hot to the cold junction.

Prior attempts have been made to mathematically model the thermoelectric device performance, assuming that the material properties are being invariant with temperature [41-46]. Later dimensionless entropy equations were derived that formed a closed form expression for the TE system [10-12]. These equations were later used to analyze the optimum design of thermoelectric cooler [47-51]. However, the above mentioned design methods disregard the effect of the contact resistances. Although reasonable for macro TEC (>100 µm), as the size of the TE elements scale down, the
effect of contact resistances become increasingly important and is essential to accurately modeling the performance of μTEC [42]. The effect of electrical contact resistance on the performance of μTECs was studied by Semeniouk, V [52]. Models accounting for both the contact resistances [53, 54] have been reported, but are not applicable when the temperature of the object to be controlled (passive load) is comparable to the size of the μTEC. More recently Prabhakar et al. [55] modeled a single stage μTEC specifically for bio-applications. In all of the above models the μTEC was connected to the external circuit by an inter-metallic planar wiring layer, which was an integrated part of the device die. As a modular system of integrated sensor and actuator with an intermediate bump layer is desired, it is essential to study the effect of bumps on the performance of the μTEC. A performance analysis of the integrated cooling cell, a single stage μTEC and bumps were performed, using a lumped parameter model.

3.3. Lumped Parameter Model

The lumped parameter model development followed the approach of Prabhakar [11], based on a set of rate equations describing one-dimensional thermal dynamics through all the intermediate metal and ceramic end layers. Adiabatic boundary conditions were applied to four vertical side surfaces of the control volume. Figure 3.1 shows that there is symmetry in the single stage μTEC, indicating the adequacy of considering only a single TEC element sandwiched between two insulating end layers (Figure 3.2). The rest of the area between the substrate was assumed to be vacuum which allowed the representation of periodic boundary conditions. Any heat flow between the μTEC and the ambient surroundings in the direction perpendicular to the
line symmetry was ignored and only heat transfer along the line of symmetry which accounted for the cooling capacity was considered.

![Diagram of TEC](image)

**Figure 3.1** Schematic of a single stage TEC showing only heat transfer along the line of symmetry which accounts for the cooling capacity.

The problem formulation required a few assumptions: (1) presumption of constant heat load $Q = 0$; (2) joule heating of the interconnect was neglected (assumed to be negligible when compared with that of TEC element); (3) treatment of the heat sink as a node at constant temperature; (4) The cell to be subjected to temperature modulation by the μTEC was simulated as a heat generation input in its frozen state, ice, so the uppermost layer in the model was represented by ice.
The above mentioned assumptions have been validated by Prabakar et al. [55]. The model also accounted for the temperature dependence of the thermoelectric parameters ($\alpha$, k, $\sigma$). Initially the model was solved by setting all of the TCE material variables at 300 K. This newly obtained temperature distribution was then used to obtain new values of the variables $\alpha$, k, $\sigma$ at each level yielding a new temperature distribution.

The contact resistances are a result of impurities, variations in the crystal size and orientation and defects at the interface, which are created in the fabrication
process. When a semiconductor is grown on top of a metal (or vice versa) there is often no gap at the interface. But the different lattice parameters of the materials allow strain between the layers, which may cause the dislocation of atoms and the formation of defects [53]. Variation in the stoichiometry of the thermoelectric compounds, as well as diffusion of the metal into the semiconductor, can also occur. These surface features affect the transport of heat and electricity through the interfaces. Both resistances cause a reduction of the device performance. Thermal and electrical contact resistances are present at the metal and thermoelectric interfaces, and thermal contact resistances are present at the metal and insulator interfaces of the μTEC [56]. The effect of thermal contact resistance can be represented as discontinuity of temperature at the interface, and the electrical contact resistance increases the total electrical resistance of the device. Experimental investigations were done on the thermal contact resistance between gold (Au) coating and ceramic substrates (Al₂O₃) and found that the values ranged from 10⁻⁷ to 10⁻⁸ (Km²/W) [57]. Hmina [58] experimentally found the thermal contact resistance values for copper-glass and copper-alumina (Al₂O₃), which were of the order of 10⁻⁷ (Km²/W) with an uncertainty of about 30%. Contacts of gold-ceramic and gold-silicon dioxide formed by evaporation had resistances estimated on the order of 1 - 2x10⁻⁷ (Km²/W)[59]. Based on these reported values a thermal contact resistance of 10⁻⁷ (Km²/W) was assumed. Experiments have to be done in order to exactly determine the value of thermal contact resistance present at the interface of copper-bismuth telluride (metal/semiconductor), to accurately model the performance.

In macroscopic thermoelectric devices, specific electrical contact resistance between the semiconductor and metal electrodes has been reported to typically be
between $10^{-8}$ to $10^{-9}$ $\Omega m^2$ [60]. Specific electrical contact resistance values ranging from $10^{-5}$ to $10^{-11}$ $\Omega m^2$ have been found experimentally [26-31]. Electrical contact resistance under well controlled laboratory conditions between silicon-platinum and silicon-aluminum has been reported to be $5 \times 10^{-12}$ $\Omega m^2$ and $2 \times 10^{-11}$ $\Omega m^2$ respectively [61]. Although Si-metal is not a type of electrical contact found in the µTEC, it can be considered as a good indication that the specific electrical contact resistance of the Bismuth telluride-metal contact can be less than or equal to $2 \times 10^{-11}$ $\Omega m^2$ since the electrical resistivity of Si ($10^{-3}$ $\Omega m$) is higher than that of the thermoelectric elements. Based on this the specific electrical contact resistance of $2 \times 10^{-11}$ $\Omega m^2$ was assumed.

A first law analysis of heat transfer from the cold junction to the hot junction of the µTEC, leads to a set of modified energy balanced equations (Eq 1.6 – 1.15):

$$Q + K_1(T_{amb} - T_c) - K_2(T_{t1} - T_c) = 0$$  \hspace{1cm} (1.6)

$$K_2(T_{t1} - T_c) - K_{R1}(T_{t1} - T_{b1}) = 0$$  \hspace{1cm} (1.7)

$$K_{R1}(T_{t1} - T_{b1}) - K_3(T_{tcj} - T_{b1}) = 0$$  \hspace{1cm} (1.8)

$$K_3(T_{tcj} - T_{b1}) - K_{R2}(T_{tcj} - T_{bcj}) = 0$$  \hspace{1cm} (1.9)

$$I \alpha_1 T_{bcj} - \frac{1}{2} \rho (R + rce) - K_4(T_{thj} - T_{bcj}) - K_5(T_{tcj} - T_{bcj}) = 0$$  \hspace{1cm} (1.10)

$$I \alpha_2 T_{thj} + \frac{1}{2} \rho (R + rce) - K_4(T_{thj} - T_{bcj}) - K_5(T_{thj} - T_{bth}) = 0$$  \hspace{1cm} (1.11)

$$K_{R3}(T_{thj} - T_{bth}) - K_5(T_{b} - T_{bth}) = 0$$  \hspace{1cm} (1.12)

$$K_5(T_{b} - T_{bth}) - K_6(T_{th} - T_{b}) = 0$$  \hspace{1cm} (1.13)

$$K_6(T_{th} - T_{b}) - K_{R4}(T_{th} - T_{bth}) = 0$$  \hspace{1cm} (1.14)

$$K_{R4}(T_{th} - T_{bth}) - K_7(T_{bth} - T_{amb}) = 0$$  \hspace{1cm} (1.15)
Where $K_{R1}$, $K_{R2}$, $K_{R3}$, and $K_{R4}$ are given by \( K_{Ri} = \frac{A_i}{rct_i} \) and $rct_i$ represents thermal contact resistance at the interface of two different materials. An exact treatment of the coexistence of the thermal and electrical contact resistance requires the detailed knowledge of where the heat is generated due to the contact resistances and whether the heat is transferred across the interface. Equations (1.10) and (1.11) imply that the heat due to electrical contact resistance is generated in the thermoelectric elements and is equally distributed to the cold and the hot sides. Equations (1.7), (1.9), (1.11) and (1.14) imply that the heat due to thermal contact resistance is generated at the interface of the top insulator - top copper interconnect, top copper interconnect - thermoelectric material (TE), TE - copper bump and copper pad - bottom insulator respectively and flows toward the cold junction. Thermal contact resistance was neglected at the interface of copper bump and copper pad as an ideal point contact (minimal circular area of 0.5 µm diameter) was considered. Initial dimensions of the proposed device were chosen from Prabhakar et al. [55].

3.4. Results and Discussions

The effect of varying the following device parameters on the performance of μTEC was studied:

- μTEC leg element dimensions
- Bump radius
- Height of the metal interconnects and pads
- Electrical and thermal contact resistance
- Operational current limitations
The maximum temperature gradient was experienced in the µTEC element region; making the TEC leg dimensions an important design parameter. Initially the nominal device dimensions, which were well within the fabrication and application limitations, were used to understand the influence of the µTEC dimensional parameters (Table 3.1).

Table 3.1 Initial device dimensions for a single µTEC leg element

<table>
<thead>
<tr>
<th></th>
<th>Length (µm)</th>
<th>Width (µm)</th>
<th>Height (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ice (Cell)</td>
<td>15</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>Top ceramic plate (Alumina)</td>
<td>15</td>
<td>14</td>
<td>5</td>
</tr>
<tr>
<td>Top copper interconnect</td>
<td>15</td>
<td>12</td>
<td>unknown</td>
</tr>
<tr>
<td>Bottom copper pad</td>
<td>15</td>
<td>12</td>
<td>unknown</td>
</tr>
<tr>
<td>TEC leg element (Bi-Te)</td>
<td>unknown</td>
<td>unknown</td>
<td>unknown</td>
</tr>
<tr>
<td>Bump (copper)</td>
<td>unknown</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

After establishing baseline performance, the required design parameters were varied and analyzed parametrically. The hot junction temperature, \( T_h \), was maintained at 300 K for all further studies. Figure 3.3 gives the effective change in temperature, \( \Delta T \) (\( T_{bh} - T_c \)), as a function of applied current at zero external heat load (\( Q = 0 \)), for three different conditions: without bumps, with bumps under ideal conditions, and with bumps and non-ideal effects like electrical and thermal contact resistance. At higher values of the operating current there was a marked difference in the device performance for different µTEC geometries. However the inset in Figure 3.3 shows that for the expected operating range of 0 – 5 mA this effect was almost negligible.
Figure 3.3 Influence of bump and non-ideal effects like electrical and thermal contact resistance on the effective temperature change ($T_{bh} - T_c$) at zero external heat load ($Q = 0$)

Table 3.2 Maximum effective change in temperature ($\Delta T$, K) values for different µTEC geometry, at 5 mA

<table>
<thead>
<tr>
<th></th>
<th>Maximum $\Delta T$ (K)</th>
<th>% Difference in Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without bump</td>
<td>1.4265</td>
<td></td>
</tr>
<tr>
<td>With bump</td>
<td>1.386</td>
<td>2.83</td>
</tr>
<tr>
<td>With bump and non-ideal effects</td>
<td>1.334</td>
<td>6.48</td>
</tr>
</tbody>
</table>
Introduction of bumps and non-ideal effects produced estimated 2.83% and 6.48% differences in the effective change in temperature, respectively, when compared to a µTEC without bumps (Table 3.2). This was considered negligible when compared to the cell temperature. Figure 3.4 shows the influence of different µTEC leg element height on the performance. Due to large heat leakage through the air gap between the two ceramic end plates the increase in the height of the µTEC leg element increases the heat load at the cold junction, leading to a small junction temperature decrease. This implies that there is an inverse proportionality between the height of the leg element and effective change in temperature (K). In order to achieve a better temperature drop, the µTEC leg element height should be as small as possible. However, the smallest achievable leg height is limited by the ability to plate bismuth telluride uniformly in recess. It was reported that the most uniform deposition occurred at the minimum height of 20 µm [11]. So the height of the µTEC leg element was fixed at 20 µm. Further analysis of the µTEC was done with this fixed height. Increasing the diameter of the µTEC element increases the conductance which causes the heat leakage load to decrease, so the junction temperature increases (Figure 3.5). In order to achieve a larger effective temperature drop the µTEC element diameter should be as large as possible. However due to the proposed end application of modulating cell temperature there is a design constraint on the maximum diameter of the µTEC element. The cells were assumed to have a mean diameter of 30 µm, a value that corresponds to the most commonly used cells (fibroblasts) in tissue engineering applications [62]. This implies that the total contact cross-sectional area of each individual µTEC, including the two TE
elements and the space between them should be a maximum of 30-50 µm. The diameter of each element was restricted to a maximum of 10 µm.

---

**Figure 3.4** Influence of the µTEC leg element height at zero external heat load

**Figure 3.5** Influence of the µTEC leg element diameter at zero external heat load
After fixing the dimensions of the µTEC leg elements (height 20µm, diameter 10µm) it was also essential to explore the effect of the metal bump radius and interconnect height on the µTEC system performance. To establish its influence under the non-ideal conditions, like electrical and thermal contact resistances were studied. From inset of Figure 3.6 it can be inferred that the temperature drop increased as the radius of the bump decreased. However the smallest achievable bump dimension was limited by the ability to plate the bump with a diameter less than that of the TE element, so the radius of the bump was fixed at 5 µm. It was observed (Figure 3.7) that the temperature drop increased as the height of the copper interconnects decreased. However, the minimum height of the top copper interconnect should be such that it allowed for a proper passage of current through the two TEC elements. To do so it
should be at least 1/10 of the TE element leg height [63]. So the height of interconnect was selected to be 2-3 µm. It was also observed (Figure 3.8) that the temperature drop decreased as the height of the bottom copper pad decreased. However, the minimum height of the bottom copper pad was chosen to be 0.5 µm because of the ability to deposit copper film with good surface finish.

Figure 3.9 represents the temperature profile along the length of the µTEC for different applied current. The region in yellow represents the presence of contact resistances at the interface of different materials. These contact resistances act as heat generators at the interface which can be inferred from the steep temperature rise at the interface. It was observed that the effective change in temperature ($\Delta T_{\text{max}} = T_{bh} - T_c = 3.44$ K at 23.7 mA) was always less than the temperature drop across the TE element ($\Delta T_{te} = T_{bcj} - T_{thj} = 10.6$ K at 23.7mA), which was evident because of the presence of contact resistances at different interface [53].

![Figure 3.7 Influence of the height of the top copper interconnect at Q = 0](image-url)
**Figure 3.8** Influence of the height of the bottom copper pad at Q = 0

**Table 3.3** The dimensions of the proposed µTEC device

<table>
<thead>
<tr>
<th>Component</th>
<th>Length (µm)</th>
<th>Width (µm)</th>
<th>Height (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ice (Cell)</td>
<td>15</td>
<td>15</td>
<td>3</td>
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<td>Top copper interconnect</td>
<td>15</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>Bottom copper pad</td>
<td>15</td>
<td>12</td>
<td>0.5</td>
</tr>
<tr>
<td>TEC leg element (Bi-Te)</td>
<td>10</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>Bump (copper)</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distance between the TEC legs</td>
<td>10</td>
<td></td>
<td>10 [11]</td>
</tr>
</tbody>
</table>
Figure 3.9 Temperature profile along the length of the µTEC for different applied current (0 – 35 mA). Highlighted regions represent contact resistance present at the interface.

The dimensions of the µTEC were optimized using lumped parameter model and are shown in Table 3.3. It was predicted that a maximum effective change in temperature of 3.47 K occurred at an applied current of 23.7 mA (Figure 3.10) and Joules breakdown was found to occur at 47.7 mA, for the optimized dimensions.

3.5. Conclusions

A lumped parameter model was developed and numerical simulations were carried out to investigate the influence of critical parameters related to integrated
biological cell and the single stage µTEC system under steady state conditions. The non-ideal effects such as electrical and thermal contact resistance were included. The effects of TE leg element dimensions and height of top and bottom copper layers were also studied. The diameter of the TE leg element was constrained to 10 µm because of the size of the biological cell to be cooled. The height was limited to 20 µm as it was possible to uniformly plate bismuth telluride. It was also shown that smaller copper interconnect and pad height was beneficial for achieving a better effective temperature drop. A maximum effective change in temperature of 3.47 K was achieved for an applied current of 23.7 mA and Joules breakdown was found to occur at 47.7 mA, for optimized dimensions of the µTEC.

![Graph showing the variation of effective change in temperature with applied current for the optimized dimensions of µTEC](image)

**Figure 3.10** Variation of effective change in temperature with applied current for the optimized dimensions of µTEC
4. Fabrication of Bumps

4.1. Introduction

The prototype array of micro bumps were fabricated using UV lithography-based microfabrication technique and electroplating. This method gives high flexibility of adjusting the geometry, material composition and scalability. The following sections outline briefly the background, fabrication details, electroplating of copper and constantan bumps, and material and dimensional characterization.

4.2. Background

Few groups have fabricated copper bumps using UV lithography and electroplating on silicon substrates. Cylindrical copper bumps have been reported, but hemispherical shaped copper bumps have not been fabricated previously. Hemispherical shaped bumps are important as the heat loss from the device die could be reduced. Constantan (copper-nickel) bumps have not been fabricated previously. Ueno et al. [34] electroplated copper column bumps on printed wire boards with diameters of 75 µm, heights of 50 µm and a pitch of 200 µm. Tomita et al. [32] successfully fabricated tin-capped copper column bumps with a height of 5 µm that were spaced 100 µm apart for 3D LSI chip integration. Yamada et al. [3] fabricated copper column-based solder bumps by electroplating of various sizes, with diameters of 65, 85, 120 µm, height of 70 µm and a pitch of 300 µm for a CCD micro-camera visual inspection system. Son et al. [4] electroplated Cu (60 µm)/ Sn/Ag (20 µm) double bump with a diameter of 60 µm and a pitch of 100 µm.
4.3. Fabrication Outline

The fabrication of bumps was done through a UV lithography-based microfabrication technique. Figure 4.1 gives an overview of the steps in the microfabrication sequence.

![Fabrication Outline Diagram]

Figure 4.1 Overview of the microfabrication steps. (1) Silicon wafer base. (2) E-beam deposit titanium and copper. (3) Spin AZ 4620 resist. (4) Expose and develop the resist. (5) Deposit copper in the recess to form the bump. (6) Remove the resist.

The microfabrication was performed on a silicon wafer. The first step was to electron beam (e-beam) evaporate a 0.01 µm thick titanium adhesion layer and a 0.05 µm thick copper plating base, to facilitate electrodeposition in future steps. A 20 µm
thick layer of AZ 4620 (AZ Electronic Materials, Somerville, NJ) resist was spin coated and baked on the e-beam deposited sample. A UV exposure was made and the resist was developed. Copper was electrodeposited (Kinetic region) in the patterned recess until it reached the top surface of the resist. Over plating of copper was done so as to have diffusion controlled electroplating for the hemispherical bump formation. The remaining resist was completely removed and the measurements were done. Same procedure as described above was used to fabricate constantan bumps except that the plating bath had a copper-nickel solution.

4.4. Electrodeposition

4.4.1. Introduction

Constantan (copper-nickel) and copper bumps were chosen as the bump materials for the device because Type-T (copper-constantan) thermocouples were chosen as the thermal sensors due to excellent sensitivity below 0 °C (ASTM 1970), and stable Seebeck coefficients at low temperatures. Copper and constantan (copper-nickel) were more easily electroplated than any other standard alloys like chromel, alumel, nicrosil, nisil used for thermocouple. The next few sections give a brief background on the electrodeposition of copper and constantan; electrochemical factors considered in fabrication and describe experiments done to obtain the bumps.

4.4.2. Background

For a particular electrodeposition cell setup (bath composition, cell and electrode geometry, as well as other factors) the relationship between the voltage and the current of the system can be shown by a polarization curve. This curve gives useful data about
an electrochemical system, especially in terms of alloy deposition. Figure 4.2 is an example of a copper-nickel polarization curve. When a voltage is applied between the anode and cathode, the measured current density is given by the combined curve in the figure. The real benefit of studying the polarization curve in alloy deposition is being able to separate the individual curves of the elements in the alloy to determine their plating characteristics.

Figure 4.2 Representative polarization curve for copper and nickel alloy deposition. [14]

In the example curve there are copper and nickel curves as well as a curve for hydrogen evolution, a side reaction occurring at higher over-potentials that decreases efficiency. The relative amount of a single component element deposited in an alloy is based on the relative proportion of the total current density for that element. Knowing
the trend of individual component polarization curves can aid in predicting deposition composition for alloys.

The rate of material deposited is based on the current efficiency and Faraday’s law (Eq. 1.1)

$$It = nF \left[ \frac{m}{sM} \right]$$

(1.16)

Where, \(I\) is the applied current, \(t\) is the time length of deposition, \(n\) is the number of electrons in the reaction, \(s\) is the stoichiometric coefficient in the balanced reduction equation, \(M\) is the molecular weight, \(F\) is Faraday’s constant (96,485 Coulombs/mole) and \(m\) is the mass reacted. The actual rate is generally smaller because not all of the applied current goes toward depositing the metal; the efficiency is typically less than 100%.

As shown in Figure 4.2, each partial current density has its own polarization curve, the sum of which gives a combined, overall polarization curve for the system. The relative amount of a single component element deposited in an alloy is based on the relative proportion of the total current density curve coming from the curve for that element. Knowing the trend of individual component curves can aid in predicting deposition composition for alloys.

In this project, a specific composition of two metal species was required, and it was important to pay attention to what current was being used to electrodeposit, and also which section of the curve was in use. From the figure, there is a thermodynamically-controlled reversible potential at the start of the curve, a kinetically controlled upward sloping region, and a flat mass transport-controlled region.
Generally, regions are mixed, such that the curve is not governed just by mass transport or just by kinetics.

At equilibrium, no current is applied, and the reaction is at its reversible potential along the x-axis of the graph. This reversible potential is based on the standard potential, which is a constant for a particular oxidation or reduction of an ion, modified by thermodynamic solution factors. Electrons will normally try to go to the most favorable, lowest energy, state, and remain there. For example, if iron is placed into a solution of \( \text{CuSO}_4 \), the copper will replace the iron on the surface, because it is a more favorable energy state for the electrons. Applying a current will help to move a reaction out of the unfavorable range and allow reactions that normally would not happen to take place.

Once a current or voltage is applied, the relationship between the current and voltage is governed by the rate of electrochemical charge transfer. For electrodeposition onto a substrate, this reaction is governed by the Butler-Volmer equation for a cathodic process (Eq. (1.2))

\[
i_c = i_o e^{\frac{-\beta \eta F \eta}{RT}} \tag{1.17}
\]

Where, \( i_o \) is the exchange current density, \( \beta \) is the reaction rate, \( R \) is the gas constant, \( T \) is the temperature, \( \eta \) is the overpotential. Overpotential is the voltage deviation from equilibrium or the reversible potential. The exchange current is the back and forth exchange of charge carriers going on in the system even during equilibrium. Deposition in this zone is known as the kinetic region and current rises exponentially with an increase in over-potential.
When the current is high enough (depending on the solution concentration, mixing, and geometry), mass transport dominates (Figure 4.2). The zero slope in the partial current curve during mass transport indicates that although the potential in the reaction may be increased, the current at which the species react and the rate of deposition remain the same. This is called the limiting current, and it occurs because mass transport is limiting the reaction. In the plating cell, more current simply increases the amount of hydrogen evolution, and not the amount of species deposited (efficiency goes down). The limiting current is affected by mixing of the solution, rotating the working electrode, and species concentration in the solution.

At lower currents, in the kinetic region, the surface concentration of ions is approximately equal to the bulk concentration. At higher currents, the deposition rate is more rapid, and the ions are not replaced quickly enough on the surface. This creates the mass transport limitation, where the surface concentration is not equal to the bulk ion concentration.

The diffusion layer is the distance from the electrode, generally several micrometers size, where the local ion concentration is smaller than the bulk concentration. Within this layer, there are three main modes of mass transport: diffusion-based transport governed by species concentration, convection-based transport governed by solution velocity, and migration-based transport governed by the electric field. In electrochemical cells, migration can often be neglected, and the diffusion layer can be simplified into a linear Nernst diffusion layer near the electrode, where diffusion is assumed to play the main role, and the remaining space where
convection is dominant. The limiting current can then be approximated by Equation (1.3).

\[
\frac{i_{lim}}{nF} = D \frac{C^b}{\delta_N}
\]  

(1.18)

Where, \(i_{lim}\) is the limiting current, \(D\) is the diffusion coefficient for the solution, \(C_b\) is the bulk ion concentration and \(\delta_N\) is the Nernst diffusion layer distance. This equation assumes that the surface concentration, \(C_s\) is 0. Equation (1.3) reveals that a smaller diffusion layer gives an increased limiting current, which means there is an increased concentration slope near the surface. In electrodeposition of microstructures, this is important because the Nernst diffusion layer is approximately equal to the depth of the recess during deposition.

4.4.3. Electrodeposition in Recesses

Plating in recesses has concerns about mass transport limitations and pH increase at the surface. It has been reported that pH increases at the surface with time and could negatively affect the growth of microstructures [64]. For microstructures, nickel was kept in great excess of the copper, leaving copper as mass transport controlled. Cygan [14] fabricated copper-nickel posts in 3 and 5 µm diameter recesses with 20 µm depth. The solution used was a modified version of Panda’s solution that enabled kinetic control of both copper and nickel deposition. A pulse plating scheme along with mild agitation was used to give a relaxation time to bring the pH back down and allow any hydrogen gas formed during electrodeposition to escape from the surface of the electrode [14, 64].
4.4.4. Electrodeposition of Bumps

Bumps are generally formed by chronoamperometry. Chronoamperometry is an electrochemical technique in which the potential of the working electrode is stepped up and the resulting current accruing at the electrode, caused by the potential step was monitored as a function of time. While plating on an array of recesses, the surfaces of the solid electrodes are usually inhomogeneous in a physical sense because of the presence of a number of crystal faces with different electrochemical characteristics and are often inhomogeneous in a chemical sense, partly covered with oxides or absorbed electro-inactive molecules and ions [65]. Such a situation can arise when arrays of electrodes are fabricated by microelectronic methods, or when the electrode is a composite material based on conducting particles, such as copper, in an insulating layer, such as a photoresist. Figure 4.3 shows an overview of the bump formation process during electroplating into recesses. At the beginning, the electrodeposition was done in kinetic region where the ions tend to follow the electric field along the path of least resistance. This implies, more electric field lines come from the side of the anode into the active region. This gives rise to the concave profile at the top of the deposit (Figure 4.3 (A, B)). When the deposition of the metal reaches the top of the resist the current is ramped up to near its limiting value. At short time scales, when the diffusion layer thickness is small compared to the size of the active region, each spot or region generates its own planar diffusion field (Figure 4.3 (D)). This allows for more deposition at the center of the recess Figure 4.3 (E). As shown in Figure 4.3 (F) with time as the diffusion layer expands and the thickness of the layer is large with respect to the size of the metal recess but small when compared to the distance between the two adjacent
electrode recesses, steady-state diffusion occurs at each active spot, depending on its shape. At longer time scales, the individual linear diffusion is augmented by a radial component. This forms a spherical diffusion field Figure 4.3 (F, G), which leads to uniform growth of the plating species on all sides rendering the bump its shape.
Figure 4.3 Overview of the bumping process. (A) Electroplating starts in the kinetic region with field lines bending from the distant anode to the micro cathode area. (B) Intermediate stage during plating through the recess. (C) Shows a profile when the top of the resist is reached. (D) Potential at the cathode or working electrode is stepped up leading to the evolution of planar diffusion field. (E) Plating at the center of the profile. (F) At an intermediate stage where bump formation begins and the transition of the shape of the diffusion field to spherical. (G), (H) Formation of uniform spherical diffusion field with more uniform plating on all sides. (I), (J) and (K) At longer time scales, the individual diffusion fields begin to extend, and merge into a single larger field and the individual single active areas are no longer distinguishable.

At still longer time scales, when the diffusion layer is much thicker than the distances between the active regions, the separated diffusion fields merge into a single larger field and have an area equal to the geometric area of the entire array, even including that of electrically insulating region present between the active regions and plating occurs merging the individually distinguishable bumps (Figure 4.3 (I, J, K)). Thus, the individual active regions are no longer distinguishable. All of the above
mentioned behavior and their transitions have been analyzed analytically and experimentally for arrays of electrodes [8-14].

4.5. Micro-Bump Fabrication

4.5.1. Wafer Preparation

The microfabrication was performed on a 4” diameter single side polished silicon wafer (1 – 20 Ω - cm). A 0.01 µm titanium adhesion layer and a 0.05 µm copper plating base were e-beam (Model BJD-1800 E-Beam Evaporator, Temescal, Wilmington, MA) evaporated onto the surface of the silicon wafer. The wafer was cleaned using acetone, isopropyl alcohol (IPA), and rinsed in DI water to remove any oxides or organic residue. The wafer was then dehydration baked at 95 °C on a hot plate for 5 minutes to promote adhesion of the resist with the substrate.

4.5.2. Spin Coating and Prebaking of the Resist

AZ 4620 resist was spin coated at 2000 rpm for 5 seconds to get a nominal thickness of 20 µm. After spin coating, the edge bead was removed with a glass plate. The sample was given a 10 minute relaxation time before being soft baked in a convention oven (M326 Mechanical Convection Oven, Blue M Electric, Watertown, Wisconsin) for 10 minutes at 85 °C. The sample was again baked on a hot plate at 115 °C for 60 seconds. The sample was baked on a glass holder on the hotplate such that there was an air gap between the middle underside of the wafer and the hotplate, and the top was covered [66]. The high temperature bake was experimentally found to improve aspect ratio, but also reduced exposure sensitivity, so it was kept short [14]. The air gap prevented the sudden heating of the base of the resist, which caused
thermal stress, and the cover helped to maintain proper and uniform temperature over the resist surface. After baking, the sample was allowed to cool for at least 20 minutes before exposure.

4.5.3. UV Exposure and Resist Development

A UV exposure was performed under high vacuum contact on a Quintel UL 7000-OBS Aligner and Exposure station (Quintel Corp., Morgan Hill, CA) with a dose of 600 mJ/cm² at 365 nm wavelength. The sample was developed for 5 minutes in AZ 400K developer (AZ Electronic Materials, Somerville, NJ), diluted 4:1 with DI water, rinsed with DI water, and dried by blowing nitrogen gas (Figure 4.4). Developing was done in Branson ultrasonic cleaner (Branson 2510R-DTH, Branson Ultrasonics Corporation, Danbury, CT 06813) bath.

4.5.4. Electroplating Experiments

This section includes the details of the electroplating jig, jig accessories and necessary plating parameters like over-plating current and time involved in electroplating of copper and constantan bumps.

![Figure 4.4](image)

Figure 4.4 (A) 5 µm diameter recess after exposure and development; (B) 3 µm diameter recess after exposure and development.
The primary design of the plating jig was borrowed from Adam Cygan at the Department of Mechanical Engineering, LSU. The electroplating jig (Figure 4.5) consists of the bottom and top cover. The bottom of the jig has a stainless steel disk which is connected to a copper wire to pass current. The top cover of the jig had O-rings to prevent the solution leakage into the contact surface. Prior to deposition, the patterned sample was placed in a vacuum chamber (Figure 4.6) and 5-10 mL of DI water was placed over the patterns. A vacuum pump was used to depressurize and remove air bubbles over the patterned areas leaving the sample ready for deposition. The depressurized sample was placed on the steel disk and was connected to the steel disk by copper conducting tape. The top and bottom parts of the jig (Figure 4.7) were held together with six nylon screws. The whole assembly was immersed in the plating solution for electrodeposition. A platinum coated titanium mesh counter electrode was used in the experiments, along with a mechanical stirrer to provide agitation. A horizontal substrate orientation was used to allow the escape of any hydrogen gas formed during deposition.

Figure 4.5 Electroplating jig.
Figure 4.6 Vacuum chamber used to depressurize the samples.

Figure 4.7 Apparatus for micro-bump deposition.
4.5.4.1. Copper Electrodeposition

A galvanostatic electrodeposition scheme without pulsing was used to fabricate the copper bumps. Copper bumps of different heights were fabricated on 2 base structures of 5 and 3 µm diameters respectively. The composition of the solution used for plating is as shown in Table 4.1. Copper was electrodeposited in the patterned recess until the top surface of the resist, under kinetic control, at 7 mA/cm² for 1 hour and 15 minutes.

Table 4.1 Copper plating solution components (Chomnawang, 2002).

<table>
<thead>
<tr>
<th>Solution Component</th>
<th>Composition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper Sulphate</td>
<td>1.0 M</td>
</tr>
<tr>
<td>Sulfuric Acid</td>
<td>100 mL/L</td>
</tr>
</tbody>
</table>

Over-plating was done at 300 mA/cm² so as to have diffusion controlled electroplating for the bump formation. Over-plating was done for 3 different plating times 5, 10 and 15 minutes. Figure 4.8 and Figure 4.9 show SEM micrographs of copper bumps electroplated on 5 and 3 µm diameter base structures for different over-plating times.

Figure 4.8 SEM micrograph of copper bump electroplated on 5 µm diameter base structure for different over-plating times. (A) 15 minutes (B) 10 minutes (C) 5 minutes
Figure 4.9 SEM micrograph of copper bump electroplated on 3 µm diameter base structure for different over-plating times. (A) 15 minutes (B) 10 minutes (C) 5 minutes

The diameter and the height of the bumps were measured using a Measurescope (MM-22, Nikon Corp., Kawasaki, Japan) and non-contact profilometer (Nanovea ST400, Micro Photonics Inc., Allentown, PA) respectively. The measured values were represented by the mean value and with the error bars representing the 95% confidence interval. Figure 4.10 shows the variation of measured bump diameter for 3 different over-plating times on 5 and 3 µm diameter base structures. The measured mean heights of the copper bumps for different plating parameters are shown in Figure 4.11. The measured mean diameter and height of the copper bumps and their difference is shown in Table 4.2. The dimensional variation of the copper bumps was found to be ±0.52 µm with a confidence interval of 95%. As the over-plating time increased the difference between the measured mean diameter and height of copper bumps respectively, on 5 and 3 µm diameter base structures decreased suggesting that at the initial stage of over-plating, the area exposed to the plating solution does have an effect on the bump diameter and height. However as the over-plating time was increased this effect was found to be minimal.
Figure 4.10 Measured copper bump diameter variation for three different over-plating times (5, 10 and 15 minutes).

Figure 4.11 Measured copper bump height variation for three different over-plating times (5, 10 and 15 minutes).
Table 4.2 Measured mean diameter of the copper bumps for 3 different plating times on two base structures of 5 and 3 µm diameter

<table>
<thead>
<tr>
<th>Over-plating time (minutes)</th>
<th>5 µm diameter base structure</th>
<th>3 µm diameter base structure</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Diameter (µm)</td>
<td>Height (µm)</td>
<td>Diameter (µm)</td>
</tr>
<tr>
<td>5</td>
<td>10.226</td>
<td>8.4933</td>
<td>6.5451</td>
</tr>
<tr>
<td>10</td>
<td>20.3119</td>
<td>10.258</td>
<td>18.0776</td>
</tr>
<tr>
<td>15</td>
<td>30.1574</td>
<td>12.694</td>
<td>29.5554</td>
</tr>
</tbody>
</table>

Table 4.3 Dimensional variation of copper bumps with 95% confidence interval

<table>
<thead>
<tr>
<th>Over-plating time (minutes)</th>
<th>5 µm diameter base structure</th>
<th>3 µm diameter base structure</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Diameter (µm)</td>
<td>Height (µm)</td>
</tr>
<tr>
<td>5</td>
<td>0.52</td>
<td>0.24</td>
</tr>
<tr>
<td>10</td>
<td>0.52</td>
<td>0.22</td>
</tr>
<tr>
<td>15</td>
<td>0.26</td>
<td>0.24</td>
</tr>
</tbody>
</table>

4.5.4.2. Constantan (Copper-Nickel) Deposition

The sample was patterned and developed in the sample way as for copper bumps. For electrodeposition, the plating setup used was the same as for the copper bumps, using constantan plating solution. A galvanostatic electrodeposition scheme with pulse plating scheme was used to fabricate the constantan bumps [14]. Constantan bumps were fabricated on 2 base structures of 5 and 3 µm diameters respectively. The composition of the solution used for plating is as shown in Table 4.4. Constantan was electrodeposited in the patterned recess until the top surface of the resist, under kinetic control, at 15 mA/cm² with a 0.25 duty cycle and 10 seconds on time was used for a total plating on-time of 20 minutes.
Table 4.4 Constantan plating solution components [14]

<table>
<thead>
<tr>
<th>Solution Component</th>
<th>Composition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nickel Sulfate</td>
<td>1.0 M</td>
</tr>
<tr>
<td>Copper Sulfate</td>
<td>0.5 M</td>
</tr>
<tr>
<td>Sodium Citrate</td>
<td>1.0 M</td>
</tr>
<tr>
<td>Ammonium Hydroxide</td>
<td>74 mL/L</td>
</tr>
</tbody>
</table>

When over-plating was done at 1 A/cm² with the same duty cycle as that for plating in recess for a total on time of 10 minutes, an oxidized and highly uneven deposit was formed (Figure 4.12). To alleviate this effect, the current density and on time during each cycle was reduced. Over-plating was done under diffusion control at 0.75 A/cm² with 0.25 duty cycle and 5 seconds on time for a total on time of 10 minutes. The same was rinsed in DI water and blown dry with nitrogen gas.

The diameter and the height of the constantan bumps were measured using a Measurescope (MM-22, Nikon Corp., Kawasaki, Japan) and non-contact profilometer (Nanovea ST400, Micro Photonics Inc., Allentown, PA) respectively. The resist was dissolved in acetone and cleaned in DI water and blown dry with nitrogen gas. SEM images were taken to examine the structures. Unfortunately the sample was mishandled which led to the breakage of the base structures. The measurement of diameter and height of the bumps were made for all the 10 samples present on the same substrate and are represented by the mean and the error bars indicate 95% confidence interval. The measured mean diameter of the constantan bump on 5 and 3 µm diameter base structures were found to be 28.45 and 27.76 µm respectively and the height to be 12.43 and 12.04 µm respectively, on the corresponding base structures.
Figure 4.12 Constantan bump formation with oxide and highly uneven surface at high current density with 0.25 duty cycle for 10 seconds on-time and a total plating on-time of 10 minutes.

Figure 4.13 SEM image of constantan (copper-nickel) bumps. (A) 3 µm diameter base structure. (B) 5 µm diameter base structure.
Figure 4.14 Measured constantan bump diameter variation for a total over-plating times of 10 minutes on 5 and 3 µm diameter base structures.

Figure 4.15 Measured constantan bump diameter variation for a total over-plating times of 10 minutes on 5 and 3 µm diameter base structures.
Table 4.5 Measured mean dimensions and variations with 95% confidence interval of constantan bumps on 5 and 3 µm diameter base structures for a total over-plating on time of 10 minutes

<table>
<thead>
<tr>
<th></th>
<th>5 µm diameter base structure</th>
<th>3 µm diameter base structure</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Diameter (µm)</td>
<td>Height (µm)</td>
</tr>
<tr>
<td>Mean</td>
<td>28.45</td>
<td>12.43</td>
</tr>
<tr>
<td>Variation</td>
<td>0.51</td>
<td>0.26</td>
</tr>
</tbody>
</table>

Figure 4.16 Energy dispersive spectrometric analysis of constantan bump

The dimensional variation of the constantan bumps was found to be ±0.51 µm with a confidence interval of 95%. The difference in the mean values of the diameter and height of the bumps on both of the base structures was 0.69 and 0.39 µm respectively, which was similar to the trend for the copper bumps. Energy dispersive spectrometric analysis (EDXRF) of constantan bump was done to confirm the presence of copper and nickel (Figure 4.16). However, due to various fabrication constraints at CAMD, LSU and time limitations involved, the fabrication of constantan bumps with
diameter of the order of few micrometers have not yet been explored as part of this study.

4.6. Conclusions

It was shown that successful production of micro bumps of copper and constantan is feasible by means of electrodeposition techniques in combination with LIGA technology. Copper and constantan micro bumps with mean diameters of 6.5 and 27.76 µm were fabricated showing the possible use of these bumps in the application of fine pitch requirement. Although galvanostatic plating with out pulse plating scheme was used to fabricate copper bumps, further studies are needed to employ reverse pulse plating to improve the surface morphology and form compact electrodeposit [67]. Further studies with reduction of total over-plating on time to form smaller constantan bumps of the order few micrometers are needed.
5. Printed Circuit Board

5.1. Introduction

A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive traces. Alternative names are printed wiring board (PWB), and etched wiring board. A PCB populated with electronic components is a printed circuit assembly (PCA), also known as a printed circuit board assembly (PCBA). PCBs are rugged, inexpensive, and can be highly reliable. PCBs require much more layout effort and higher initial cost than either wire-wrapped or point-to-point constructed circuits using bread boards, but are much cheaper and faster for high-volume production. Prior to the advent of the PCB, electrical interconnections between components were made in a point-to-point fashion. This was very time consuming and highly error prone. PCB have offered a way to make ordered interconnections between components while radically reducing the potential for error by allowing faithful reproduction of the circuit using a combination of lithographic and etching methods. Much of the electronic industry’s PCB design, assembly, and quality control needs are set by standards that have been published by the IPC organization.

5.2. Classification

PCB substrates are usually called laminates. These PCB laminates are created in two primary forms: single-clad and double-clad laminates. They are also produced in a number of different thicknesses to facilitate different customer requirements. When used in the manufacture of multilayer circuits, the laminates are commonly referred to as core material.
5.2.1. Single-clad Laminates

Single-clad laminates have copper on one side and are used either for the manufacture of single-sided circuits or for the manufacture of multilayer circuits as an inner layer.

5.2.2. Double-clad Laminates

Double-clad laminates are essentially identical to single-clad laminates in description and use except that copper is laminated on both sides of the structure.

5.3. Generic Process Overview of Single Sided PCB

Figure 5.1 shows the overview of the fabrication process for single-clad FR-4 Printed Circuit Boards. First the laminate or substrate is cleaned for any impurities present (Figure 5.1(A)). The metal layer, commonly copper, is either deposited on the laminate (Figure 5.1(B)) by vacuum methods or metal foil is hot pressed on the laminate with the help of adhesive resin in between the metal foil and laminate. Negative tone resist is coated on the entire surface of the metal clad laminate and baked either on hot plate or convection oven (Figure 5.1(C)). The resist coated laminate is exposed to either to X-rays and UV light and developed in the corresponding developer to form patterns to expose the metal to be etched (Figure 5.1(D)). The exposure is done using a photo definable mask made of soda lime on most cases to define the desired pattern on the laminate. The patterned laminate is immersed in a metal etching solution and the exposed metal is etched leaving the metal under the resist (Figure 5.1(E)). The remaining resist is stripped to leave the metal under it (Figure 5.1(F)). This is the most generic method employed to produce industry standard PCBs.
Figure 5.1 Overview of the PCB fabrication process. (A) Substrate or laminate cleaning. (B) Metal is deposited on the substrate. (C) Negative tone photoresist is spin coated on the metal clad laminate. (D) Exposure and development of the resist. (E) Etching of the exposed metal. (F) Stripping of the left-over resist.

This technique cannot be used to fabricate fine pitch micro traces of copper on PCB because of (A) the lateral etching of the copper would yield non-straight edges on the traces giving rise to parasitic resistance; (b) Processing time needed for negative resists is very high when compared to positive resists. These could be overcome by using a liftoff technique as any kind of fine metal pattern and high quality pattern can be fabricated without any crack or grain defects [68]. It has also been shown that liftoff techniques can be used to pattern any difficult-to-etch metals and metal oxides [69]. Liftoff processes requires only one optimization step for resist development when compared to that of generic process.
5.4. PCB Fabrication Overview

The fabrication of the custom PCB was done through a UV lithography based microfabrication technique. Figure 5.2 shows an overview of the microfabrication sequence. The microfabrication was performed on a 4 inch diameter FR-4 substrate. FR-4 is Epoxy/glass fabric which has high flex and impact strength, an excellent electrical insulator, and is highly flame retardant. Based on the above said properties FR-4 substrate was chosen to fabricate the custom PCB.

A 2 µm thick Lift of resist (LOR 20B, MicroChem Crop., Newton, MA) was spin coated on the sample and baked (Figure 5.2 (B)). A 10 µm thick AZ 4620 resist was spin coated and baked on the coated sample (Figure 5.2 (C)). UV exposure was made
and the resists were developed. A flat exposure under UV light was done on the patterned sample (Figure 5.2 (D)). 0.01 µm thick Titanium and a 0.5 µm thick Copper layer were e-beam evaporated on the resist coated samples (Figure 5.2 (E)). Then the liftoff was done by rinsing the metal deposited sample in MF319 developer (Rohm and Hass Electronic Material LLC, Marlborough, MA) (Figure 5.2 (F)).

5.5. UV Photomask Design

Photomasks are used to have desired pattern on a resist coated substrate. Photo mask was designed to fabricate PCB test structures on FR4 laminate. Figure 5.3 and Figure 5.4 shows an overview of the PCB test mask and close up of the center pads respectively.

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Figure 5.3 Overview of the PCB test mask
5.6. Experimental Details

5.6.1. Sample Preparation

FR4 (Insulectro, Londonderry, NH) laminate, 2mm thick and 18”x24” board was cut into 4” diameter circular pieces using a band saw. As these work pieces were too thick to fit on to the UV exposure machine’s jig, they were milled to a thickness of 1.1mm by conventional milling machine at the Mechanical Engineering (LSU) machine shop. The samples were warped after conventional milling due the presence of residual stress developed during milling. The samples were flattened by placing them under a weight of 3 kg in convection oven at 150 °C for 5 hrs and were allowed to cool to room-
temperature. The last 100 µm was milled using a fly cutting machine at CAMD. The milled surface was then lapped to fit onto the jig of the UV exposure machine.

5.6.2. Spin Coating and Prebaking of the Resist

A 2 µm thick LOR 20B resist was spin coated at 2800 rpm for 30 seconds on the laminate. The sample was then soft baked on a hot plate for 5 minutes at 150 °C. The sample was allowed to cool to room temperature for about 20 minutes. A 10 µm thick layer of AZ 4620 was spin coated over the LOR at 2000 rpm for 15 seconds. The sample was given a 10 minute relaxation time before being soft baked in a convention oven (M326 Mechanical Convection Oven, Blue M Electric, Watertown, Wisconsin) for 10 minutes at 85 °C. The sample was again baked on a hot plate at 115 °C for 60 seconds. The sample was baked on a glass holder on the hotplate such that there was an air gap between the middle underside of the wafer and the hotplate, and the top was covered [66]. The sample was allowed to cool to room temperature for at least 20 minutes.

5.6.3. UV Exposure and Resist Development

A UV exposure was performed under high vacuum contact on a Quintel UL 7000-OBS Aligner and Exposure station (Quintel Corp., Morgan Hill, CA) with a dose of 600 mJ/cm² at 365 nm wavelength. The sample was developed for 4 minutes and 30 seconds in AZ 400K developer (AZ Electronic Materials, Somerville, NJ), diluted 4:1 with DI water, rinsed with DI water, and dried by blowing nitrogen gas. Figure 5.5 shows a close up view of the center pads and the big pads after exposure and development. Any residual resist was removed by oxygen plasma etching for 3 minutes.
Figure 5.6 shows the SEM image of undercut caused by rapid etching of the LOR resist when compared to AZ 4620.

Figure 5.5 Close up view of center pads and the big pads after exposure and development

Figure 5.6 SEM micrograph of undercut under AZ 4620 on PCB substrate
5.6.4. Flat Exposure and Metal Deposition

The developed sample was then flood exposed under UV light. 0.01 µm thick Titanium and a 0.5 µm thick Copper layer were e-beam evaporated on the resist coated samples (Figure 5.7).

![Figure 5.7 Titanium and Copper clad FR4 laminate](image)

5.6.5. Liftoff Process

Liftoff of copper was done by immersing copper clad laminate in AZ 400 K developer (AZ Electronic Materials, Somerville, NJ) for 1 hour 20 minutes with little agitation. Figure 5.8 shows the progression of the liftoff process at different time intervals. It was inferred that the process was slow at the beginning as the area of contact between the resist and the developer was less. However, with increased time the area of contact increased, which lead to a clear liftoff. After 1 hour 20 minutes, the sample was washed in DI water and blown dry with nitrogen gas. Figure 5.9 shows the micrographs of the center pads, big pads and wire structures after liftoff process.
Figure 5.8 Progression of copper liftoff process at different time (t) intervals. (A) At the beginning i.e., t = 0 minutes. (B) At t = 5 minutes. (C) At t = 30 minutes. (D) At t = 45 minutes. (E) At t = 1 hour. (F) At t = 1 hour 20 minutes.

Figure 5.9 Optical micrographs of PCB. (circles indicates the defects) (A) and (B) Center pads, (C) Big pads (4150x1000 µm) (D) wire structures (2x2000 µm)
The edges were not very well-defined and the metal layer did not adhere to the substrate as indicated with the circles on Figure 5.9. The bigger pads showed consistent dimensions and good adhesion with the substrate, but had some irregular edges. The dimensions of the bigger pads were measured and are as shown in Table 5.1. The mean length and width of the pads were found to be 4151.98 ±1.86 µm and 1003.21 ±0.55 µm respectively. This variation from the designed nominal value can be attributed to some sources of error during photolithography explained in the subsequent sections.

5.7. Possible Solutions

5.7.1. Residual Resist on the Mask

The uneven edges formed were because of the residual resist remaining at the edges of features on the photomask. Figure 5.10 shows the residual resist present at the edges of various features on the photo mask. The presence of this resist would hinder the precise UV exposure of resist and render the features with uneven edges. This could have been avoided by cleaning the photomask with acetone after every exposure.

<table>
<thead>
<tr>
<th></th>
<th>Nominal designed value (µm)</th>
<th>Measured mean value (µm)</th>
<th>95% confidence interval (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Length</strong></td>
<td>4150</td>
<td>4151.98</td>
<td>1.86</td>
</tr>
<tr>
<td><strong>Width</strong></td>
<td>1000</td>
<td>1001.21</td>
<td>0.55</td>
</tr>
</tbody>
</table>
Figure 5.10 Micrographs of the photomask with residual resist at the corner of the features (A) Distant view of the center pads (B) Close up view of (12x12 µm) center pads (C) and (D) Left edge and left bottom edge of the big pad (E) and (F) Connecting wire and pads
5.7.2. Adhesion of Metal on FR4

Figure 5.9 shows the lack of adhesion between the metal and FR4 substrate. The reason for this is not known yet. It has been shown that the adhesion between FR4 and copper can be increased by introducing a layer of liquid crystal polymer (LCP) [70]. As LCP offers a good combination of physical and chemical properties and are not affected by physicochemical changes, they make a good choice as substrate material too.

5.8. Conclusions

The fabrication of the PCB was not very conclusive. Precise definition of structures was on FR4 laminate was not very successful. The results indicate a variation in the dimensions and lack of adhesion between the FR4 laminate and copper. The mean length and width of the bigger pads were found to be 4151.98 ±1.86 µm and 1003.21 ±0.55 µm respectively. The dimensional variation can be attributed to the residual resist on the photo mask, but the reason for lack adhesion is not known yet. The fabrication process can be improved upon. Cleaning of the mask with acetone and then rinsing with IPA and DI water, after exposure can yield higher quality patterned features. LCP can be attached to the FR4 laminate with an adhesive (Araldite) to improve the adhesion between the polymer and metal layer.
6. Conclusions and Future Work

6.1. Thermal System Modeling

6.1.1. Conclusions

To determine the effect of bumps on the performance of the single stage μTEC, a lumped parameter model was developed and numerical simulations were carried out under steady state conditions. The non-ideal effects such as electrical and thermal contact resistance were included. The effects of TE leg element dimensions and height of top and bottom copper layers were also studied. The diameter of the TE leg element was constrained to 10 µm because of the size of the biological cell to be cooled. The height was limited to 20 µm as it was possible to uniformly plate bismuth telluride. It was also shown that smaller copper interconnects and pad heights were beneficial for achieving a better effective temperature drop. A maximum effective change in temperature of 3.47 K was achieved for an applied current of 23.7 mA and Joules breakdown was found to occur at 47.7 mA, for optimized dimensions of the μTEC.

6.1.2. Future Work

Finite element analysis of the μTEC along with the micro thermocouple should be carried out in future to evaluate the performance on each of these devices in the presence of other. The Joule heating of interconnect and the heat loss to the surrounding polymer should be accounted for precise evaluation of the performance. The effect of different cells could also be modeled, along with several cells to study the performance of the integrated array with random cell position.
6.2. Fabrication of bumps

6.2.1. Conclusions

It was shown that copper and constantan bumps can be produced by means of electrodeposition techniques in combination with LIGA technology. The bumps were fabricated on 2 base structures of diameter 5 and 3 µm. Smallest copper and constantan micro bumps with mean diameter of 6.5 and 27.76 µm and height of 7.81 and 12.04 µm were fabricated showing the possible use of these bumps in the application of modular design of packaging with fine pitch requirement. The dimensional variation was found to be ±0.5 µm with 95% confidence interval.

6.2.2. Future Work

Although galvanostatic plating without pulse plating scheme was used to fabricate copper bumps, reverse pulse plating can be used to improve the surface morphology and form compact electrodeposit. Further studies with reduction of total over-plating on time to form smaller constantan bumps of the order few micrometers are needed. Triton X-100 additive can be added to the copper-nickel plating solution to reduce the sticking of hydrogen bubble on the surface of the deposit by changing their surface tension.

6.3. Fabrication of PCB

6.3.1. Conclusions

The fabrication of PCB was not very conclusive. Precise definition of structures was on FR4 laminate was not very successful. The results indicate a variation in the
dimensions and lack of adhesion between the FR4 laminate and copper. The mean length and width of the bigger pads were found to be 4151.98 ±1.86 µm and 1003.21 ±0.55 µm respectively. The dimensional variation can be attributed to the residual resist on the photo mask, but the reason for lack adhesion is not known yet. The results did indicate that the liftoff technique can be used to produce PCBs with feature sizes of the order of few micrometer and tighter tolerances.

6.3.2. Future Work

The fabrication process can be improved upon. Cleaning of the mask with acetone and then rinsing with IPA and DI water, after exposure can yield high quality patterned features. LCP can be attached to the FR4 laminate with an adhesive (Araldite) to improve the adhesion between the polymer and metal layer. Actual PCB for the integrated array should be possible with improved liftoff technique.
References


Appendix A: Photomask Used in Microfabrication of Bumps

Figure A1 Photo mask layout used to fabricate copper and constantan bumps

See Figure A2

Figure A2 Detailed view of the center of the photo mask
Appendix B: Snapshots of PCB
VITA

Ajay Kardak was born in Gwalior, India, in June 1981. Two months later, his family moved to Bangalore, India. He received the degree of Bachelor of Engineering in Mechanical Engineering from M. S. Ramaiah Institute of Technology (affiliated to Visvesvaraya Technological University), Bangalore, India, in June 2003. He joined the prestigious Indian Institute of Science (IISc), Bangalore, India, in August 2003. To further his knowledge in the field of science and technology, he enrolled for the graduate program in the Department of Mechanical Engineering at Louisiana State University, Baton Rouge, Louisiana in Fall 2005. Since then he has been working as a member of bioengineering and micro systems engineering team. He expects to receive the degree of Master of Science in Mechanical Engineering at the December 2008 commencement.